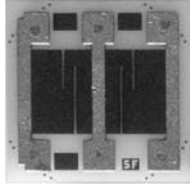


Thin Film Center-Tapped Resistor Divider Network



Product may not be to scale

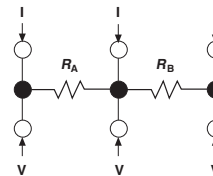
The CTT series resistor chips offer a combination of low shunt capacitance and excellent stability. The CTT offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature.

The CTTs six bonding pads allows the user increased layout flexibility. The CTTs tantalum nitride resistor material offers excellent resistance to high moisture environments.

The CTTs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTTs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

FEATURES

- Wire bondable
- Center tap feature
- Chip size: 0.030" x 0.030"
- Case: 0303
- Resistance range R_T : 10 Ω to 35 k Ω
- Alumina substrate, low shunt capacitance: < 0.2 pF
- Resistor material: Tantalum nitride
- Moisture resistant
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

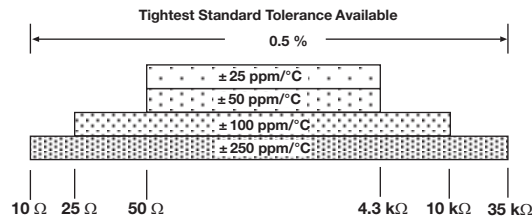


APPLICATIONS

The CTT center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, tracking, low shunt capacitance and better frequency response are necessary.

Vishay EFI measures low-value resistors by the four-wire kelvin technique.

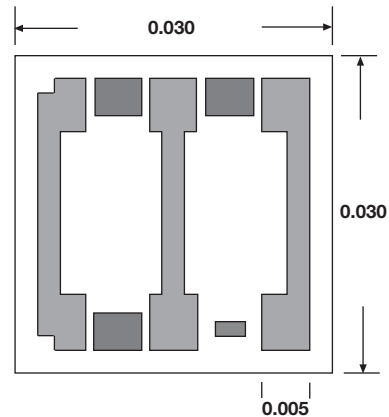
TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	VALUE	UNIT
Total Resistance Range	10 to 35K	Ω
Standard Tolerances	± 0.5	%
TCR	$\pm 25, \pm 50, \pm 100, \pm 250$	ppm/ $^{\circ}$ C



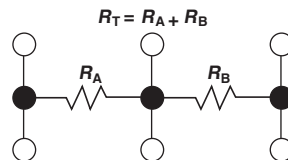
STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	VALUE	UNIT
TCR Tracking Between Halves (R_A/R_B) ⁽¹⁾	± 2	ppm/ $^{\circ}$ C
Center Tap Ratio, R_A/R_B : Tolerance	1 ± 1	%
Noise, MIL-STD-202, Method 308	- 35 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. $\Delta R/R$	%
Stability, 1000 h, + 125 $^{\circ}$ C, 62 mW	± 0.25 max. $\Delta R/R$	%
Operating Temperature Range	- 55 to + 125	$^{\circ}$ C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 max. $\Delta R/R$	%
High Temperature Exposure, + 150 $^{\circ}$ C, 100 h	± 0.2 max. $\Delta R/R$	%
Insulation Resistance	10^{12} min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at 70 $^{\circ}$ C (derated to zero at + 150 $^{\circ}$ C)	0.125 max.	W
5 x Rated Power Short-Time Overload, + 25 $^{\circ}$ C, 5 s	± 0.25 max. $\Delta R/R$	%

Note

⁽¹⁾ 10 ppm/ $^{\circ}$ C for $R < 100$

DIMENSIONS in inches


STANDARD CONFIGURATION
 *Six locations. All pads 0.005" x 0.005"

SCHEMATIC


MECHANICAL SPECIFICATIONS	
PARAMETER	VALUE
Chip Size	0.030" x 0.030" ± 0.002" (0.762 mm x 0.762 mm ± 0.050 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	99.6 % alumina
Resistor Material	Tantalum nitride
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm)
Number of Pads	6
Pad Material	25 kÅ minimum gold (Al optional)
Backing	None

Options: Alphanumeric part marking, up to six characters.

GLOBAL PART NUMBER INFORMATION																
Global Part Number: CTT5000KFKGNHWS																
Global Part Number Description: CTT 5K 10 % RT 1 % ± 100 ppm/°C ± 10 ppm/°C Au None H WS																
C	T	T	5	0	0	0	0	K	F	K	K	G	N	H	W	S
MODEL	RESISTANCE (R TOTAL)	RESISTANCE MULTIPLIER CODE	TOL. CODE (%)	RATIO TOL. (%)	TCR (ppm/°C)	TCR TRACK (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE						
CTT	First 4 digits are significant figures of resistance	B = 0.01 A = 0.1 0 = 1 1 = 10	D = 0.5 F = 1.0 G = 2.0 J = 5.0 K = 10.0	F = 1.0 G = 2.0 U = User N = No	E = ± 25 C = ± 50 K = ± 100 M = ± 250	G = ± 2 J = ± 5 K = ± 10 N = No	G = Au A = Al	G = Au N = None	H = Class H K = Class K	WS = Waffle pack 100 min., 1 mult						



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