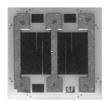
**GREEN** 

(5-2008)





# Thin Film Center-Tapped Resistor Divider Network



Product may not be to scale

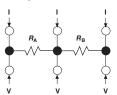
The CTT series resistor chips offer a combination of low shunt capacitance and excellent stability. The CTT offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature.

The CTTs six bonding pads allows the user increased layout flexibility. The CTTs tantalum nitride resistor material offers excellent resistance to high moisture environments.

The CTTs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTTs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

#### **FEATURES**

- Wire bondable
- · Center tap feature
- Chip size: 0.030" x 0.030"
- Case: 0303
- Resistance range  $R_T$ : 10  $\Omega$  to 35 k $\Omega$
- Alumina substrate, low shunt capacitance: < 0.2 pF</li>
- · Resistor material: Tantalum nitride
- Moisture resistant
- Material categorization: For definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

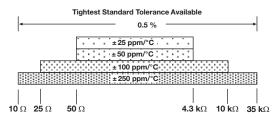


### **APPLICATIONS**

The CTT center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, tracking, low shunt capacitance and better frequency response are necessary.

Vishay EFI measures low-value resistors by the four-wire kelvin technique.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES					
PARAMETER	VALUE	UNIT			
Total Resistance Range	10 to 35K	Ω			
Standard Tolerances	± 0.5	%			
TCR	± 25, ± 50, ± 100, ± 250	ppm/°C			



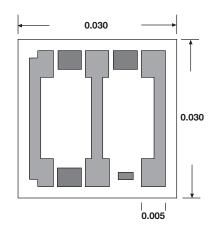
STANDARD ELECTRICAL SPECIFICATIONS	VALUE	LINUT
PARAMETER	VALUE	UNIT
TCR Tracking Between Halves $(R_A/R_B)^{(1)}$	± 2	ppm/°C
Center Tap Ratio, R <sub>A</sub> /R <sub>B</sub> : Tolerance	1 ± 1	%
Noise, MIL-STD-202, Method 308	- 35 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. ΔR/R	%
Stability, 1000 h, + 125 °C, 62 mW	± 0.25 max. ∆R/R	%
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 max. ΔR/R	%
High Temperature Exposure, + 150 °C, 100 h	± 0.2 max. ΔR/R	%
Insulation Resistance	10 <sup>12</sup> min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at 70 °C (derated to zero at + 150 °C)	0.125 max.	W
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 max. Δ <i>R/R</i>	%

### Note

(1) 10 ppm/°C for R < 100

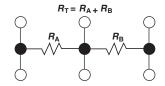


## **DIMENSIONS** in inches



**STANDARD CONFIGURATION** \*Six locations. All pads 0.005" x 0.005"

## **SCHEMATIC**



MECHANICAL SPECIFICATIONS					
PARAMETER	VALUE				
Chip Size	0.030" x 0.030" ± 0.002" (0.762 mm x 0.762 mm ± 0.050 mm)				
Chip Thickness 0.010" ± 0.002" (0.254 mm ± 0.05 mm)					
Chip Substrate Material	99.6 % alumina				
Resistor Material	Tantalum nitride				
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm)				
Number of Pads	6				
Pad Material	25 kÅ minimum gold (Al optional)				
Backing	None				

Options: Alphanumeric part marking, up to six characters.

GLOB	AL PART N	UMBER INI	ORMAT	TION						
Global F	Global Part Number: CTT50000KFKKGNHWS									
Global F	Global Part Number Description: CTT 5K 10 % RT 1 % ± 100 ppm/°C ± 10 ppm/°C Au None H WS									
С	C T T 5 0 0 0 K F K K G N H W S									
							<u> </u>			
MODEL	RESISTANCE (R TOTAL)	RESISTANCE MULTIPLIER CODE	TOL. CODE (%)	RATIO TOL. (%)	TCR (ppm/°C)	TCR TRACK (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
СТТ	First 4 digits are significant	<b>B</b> = 0.01 <b>A</b> = 0.1 <b>0</b> = 1	<b>D</b> = 0.5 <b>F</b> = 1.0 <b>G</b> = 2.0		$E = \pm 25$ $C = \pm 50$ $K = \pm 100$		<b>G</b> = Au <b>A</b> = Al	<b>G</b> = Au <b>N</b> = None	<b>K</b> =	100 min.,
	figures of resistance	<b>1</b> = 10	<b>J</b> = 5.0 <b>K</b> = 10.0	N = No	$M = \pm 250$	<b>N</b> = No			Class K	1 mult



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