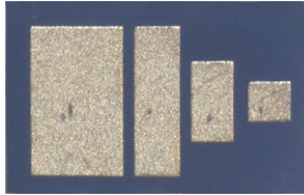


## Thin Film Binary MOS Capacitors



Product may not be to scale

The CBA MOS capacitor chips each contain four different capacitors in binary increments allowing the user many choices in value selection. Two versions of CBA capacitors are available: one with a total capacitance of 3.75 pF and one with a total capacitance of 15 pF.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CBAs are 100 % electrically tested and visually inspected to MIL-STD-883.

### FEATURES

- Wire bondable
- User value selection
- Four capacitors with common connection
- Capacitance range: 0.25 pF to 15 pF in binary increments
- Dielectric: Silicon dioxide
- Chip size: 0.019" x 0.030"
- Substrate: Silicon with gold backing
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
**GREEN**  
(5-2008)

### APPLICATIONS

Vishay EFI CBA binary MOS multi-value capacitor chips are designed for hybrid packages in which microwave circuits are to be trimmed. This is done on the CBA chips by selecting the bonding pad for the required capacitance and wire-bonding by conventional techniques.

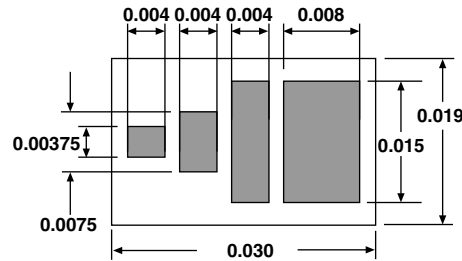
### WV (DC) VALUES AND TOLERANCES

CAPACITOR MODEL	CBA 3.75 pF	CBA 15 pF	UNIT
Case Size	0203	0203	
Total Capacitance	3.75	15	pF
Capacitance Values	0.25, 0.50, 1.0, 2.0	1.0, 2.0, 4.0, 8.0	pF
Tolerance	± 25	± 10	%
DC Working Voltage	100	30	V

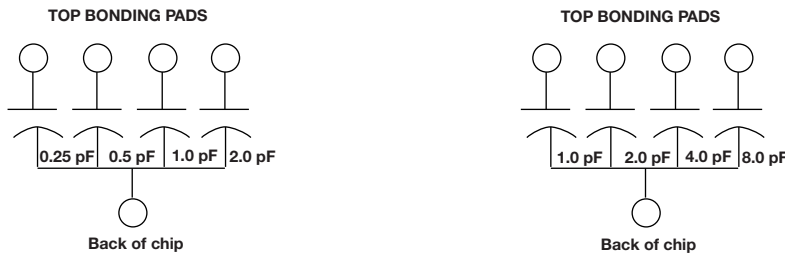
### STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	VALUE	UNIT
Capacitance Range	0.25 to 15	pF
Maximum Working Voltage	100	V
Peak Voltage at + 25 °C	1.5 x working voltage	
Dissipation Factor, 1 kHz, 1 V <sub>RMS</sub> , + 25 °C	0.1 max. MOS	%
Q at 1 mHz, 50 mV <sub>RMS</sub> , + 25 °C	1000 min.	
TCC, - 55 °C to + 150 °C	+ 15 ± 25	ppm/°C
Insulation Resistance at Working Voltage, + 25 °C	10 <sup>9</sup> min.	Ω
Operating Temperature Range	- 55 to + 150	°C
Thermal Shock	± 0.25 + 0.25 pF max. ΔC/C	%
Moisture Resistance, MIL-STD-202, Method 106	± 1.0 + 0.25 pF max. ΔC/C	%
Short Time Overload, + 25 °C, 5 s; 1.5 x Working Voltage	± 0.25 + 0.25 pF max. ΔC/C	%
High Temperature Exposure: 100 h at + 150 °C Ambient	± 0.25 + 0.25 pF max.	%
Life, MIL-STD-202, Method 108, Condition D, + 125 °C Ambient, 1000 h at Working Voltage	± 2.0 + 0.25 pF max. ΔC/C	%

**CONFIGURATIONS** in inches



**SCHEMATIC**



MECHANICAL SPECIFICATIONS	
PARAMETER	VALUE
Chip Size	0.019" x 0.030" ± 0.002" (0.48 mm x 0.75 mm ± 0.05 mm)
Chip Thickness	0.010" ± 0.003" (0.25 mm ± 0.08 mm)
Chip Substrate Material	Semiconductor silicon
Dielectric	Silicon dioxide (MOS)
Bonding Pads	10 kÅ minimum aluminum
Backing	3 kÅ minimum gold

GLOBAL PART NUMBER INFORMATION						
Global Part Number: <b>CBA3750CMAHWS</b>						
Global Part Number Description: <b>CBA 3.75 pF 20 % Al H WS</b>						
<b>C</b>	<b>B</b>	<b>A</b>	<b>3</b>	<b>7</b>	<b>5</b>	<b>0</b>
<b>C</b>	<b>M</b>	<b>A</b>	<b>H</b>	<b>W</b>	<b>S</b>	
MODEL	CAPACITANCE (pF)	CAPACITANCE MULTIPLIER CODE	TOLERANCE CODE	TERMINATION	VISUAL CLASS	PACKAGING CODE
<b>CBA</b>	First 4 digits are significant figures of capacitance	<b>C</b> = 0.001 <b>B</b> = 0.01	<b>K</b> = 10 % <b>M</b> = 20 % <b>L</b> = 25 %	<b>G</b> = Au <b>A</b> = Al	<b>H</b> = Class H <b>K</b> = Class K	<b>WS</b> = Waffle pack 100 min., 1 mult



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