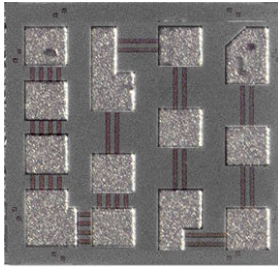


## Wire Bondable Thin Film Multi-Tap Resistor Arrays



Product may not be to scale

The MTR multi-tap resistors, available in two formats, offer eleven taps allowing the user to select specified increments a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTRs are 100 % electrically tested and visually inspected to MIL-STD-883.

### FEATURES

- Wire bondable
- Selectable values by wire bonding
- Chip size: 0.030" x 0.030"
- Case: 0303
- Standard resistance range: 100 Ω to 24 kΩ or 800 Ω to 240 kΩ
- Resistor material:  
Tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Ideally suited for hybrid prototyping
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### APPLICATIONS

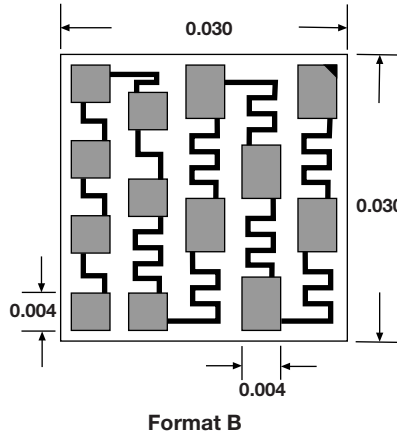
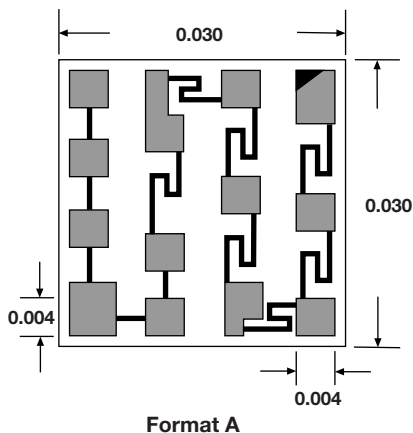
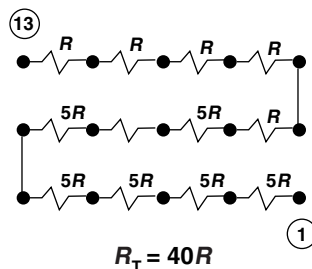
The MTR series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES			
PARAMETER		VALUE	UNIT
Total Resistance Range	Format A Format B	100, 200, 400, 800, 2.4K, 8K, 24K 800, 2.4K, 8K, 24K, 80K, 160K, 240K	Ω
7 Resistors Between Pads 1 and 8 5 Resistors Between Pads 8 and 13		Each 12.5 % of total resistance Each 2.5 % of total resistance	
Standard Tolerances		± 10, ± 20 of total resistance of all 12 resistors	%
TCR		± 100	ppm/°C

#### Example:

When the total resistance value is 8 kΩ, the resistors between pads 8 and 13 are 200 Ω each, and the resistors between pads 1 and 8 are 1 kΩ each.

STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	VALUE	UNIT
TCR Tracking Between Elements	± 5	ppm/°C
Noise, MIL-STD-202, Method 308	-30 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. ΔR/R	%
Stability, 1000 h, +125 °C, 125 mW	± 0.5 max. ΔR/R	%
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 max. ΔR/R	%
High Temperature Exposure +150 °C, 100 h	± 0.5 max. ΔR/R	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10 <sup>12</sup> min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at +70 °C (Derated to Zero at +175 °C)	0.250, total R	W
5 x Rated Power Short-Time Overload, +25 °C, 5 s	± 0.25 max. ΔR/R	%

**DIMENSIONS** in inches

**SCHEMATIC**


MECHANICAL SPECIFICATIONS	
PARAMETER	
Chip Size	0.030" x 0.030" ± 0.003" (0.762 mm x 0.762 mm ± 0.076 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO <sub>2</sub>
Resistor Material	Tantalum nitride, self-passivating
Bonding Pads	0.004" x 0.004" (0.10 mm x 0.10 mm)
Number of Top Pads	13
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

GLOBAL PART NUMBER INFORMATION									
Global Part Number: <b>MTR24001KAKANHWS</b>									
Global Part Number Description: <b>MTR 24K 10 %, format A, 100 ppm/°C, Al pads, no back metal, class H, WS</b>									
<div style="display: flex; justify-content: space-around; font-weight: bold; font-size: 1.2em;"> <span>M</span> <span>T</span> <span>R</span> <span>2</span> <span>4</span> <span>0</span> <span>0</span> <span>1</span> <span>K</span> <span>A</span> <span>K</span> <span>A</span> <span>N</span> <span>H</span> <span>W</span> <span>S</span> </div>									
MODEL	RESISTANCE	RESISTANCE MULTIPLIER CODE	TOL. CODE (%)	FORMAT	TCR (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
<b>MTR</b>	First 4 digits are significant figures of resistance	A = 0.1 0 = 1 1 = 10 2 = 100	J = 5.0 K = 10 M = 20 L = 25	A = form A B = form B	K = ± 100 M = ± 250 R = 0/- 250	G = gold A = aluminum	G = gold N = none	H = class H K = class K	<b>WS</b> = waffle pack 100 min, 1 mult
Historical Part Number: <b>WMTR05024001K</b> (will continue to be accepted)									



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