Cost-effective High Volume Interconnect Substrate Solutions

Introduction

The evolving requirements for high density interconnects has driven Vishay EFI Technology to offer a high volume manufacturing capability to answer our customers needs for cost effective solutions. A dedicated manufacturing cell with the ability to produce in excess of 10 million square inches of circuits per year has been added to Vishay EFI's existing diverse capability. EFI Technologys increasing portfolio of capabilities offers the designer a wide flexibility for meeting the demands of todays markets. Applications in the markets of wireless and fiber optic telecommunication, CATV, medical and military systems are readily solved using EFI Technologys array of design features. This design guide outlines the available toolkit for designing cost-effective volume interconnect solutions. It should be noted that a Vishay EFI Technology sales engineer should work closely with the designer to ensure the most cost-effective solution.

Overview of Technology

Vishay EFI Technology offers a wide array of features for integration into the designers interconnect. Plated through substrate vias offer a low cost approach to obtain signal or ground connections in specific locations within a circuit. Solid copper filled vias offer a lower inductance ground path than plated vias and prevent backside connection materials from contaminating the circuit surface. A wide range of resistor values offer flexibility to integrate more functionality into the interconnect, minimizing discrete part count. Thick film crossunders offer increased density and minimize wirebonding at higher assembly. Several solder stops are available and offer flexibility in assembly methods. In all, the designer can create a concise, densely packed interconnect solution offering a high performance cost-effective package for high volume applications.

Using the Guide

This guide is created as a supplement to the other guides offered by Vishay EFI Technology. The focus of this guide is to outline the standard parameters available for high volume manufacturing. It is intended to complement the information available in the single subject brochures in EFIs complete Design Guide. For the purposes of this guide, high volume is defined as continuous production within Vishay EFIs workcell over an interval of several months. As always, consult your local Vishay EFI Technology sales engineer for a review of your application and its relationship to this guide.

Substrates

As with most designs, initial layout activity begins with a selection of substrate and thickness. In general, higher frequency applications require thinner substrates both for performance and size considerations. Vishay EFI Technologys high volume manufacturing uses alumina as the substrate medium of choice in processing. Alternate materials are under consideration and can be reviewed with your local sales engineer. Table 1 outlines some important properties of alumina and the options available to the designer.

Table 1 - Substrate Properties

Substrate		
Metal	Alumina (A12O3)	99.5 % or 99.6 % purity
Surface Finish	As-Fired	5 µ" CLA
Camber	0.005 in/in	0.002 in/in available
Thickness	15, 20, 25, 27, 40 Mils	± 10 %
Wafer Size	3.75" x 4.50" 3.25" x 4.00" usable area	Other sizes available
Finished Circuit Dimension		
Laser Scribed	± 5 Mils	0.250 minimum dimension
Diced	± 2 Mils	3.0/0.3

TECH NOTE

Cost-effective High Volume Interconnect Substrate Solutions

Resistors

After choosing a substrate material and laying out the conductor pattern, the designer may choose to enhance the functionality of the circuit by adding resistors. Tasks such as voltage division, power termination and current regulation are achieved using precision thin film resistors. Resistors are patterned in thin film using a photoresist and etching process to define the outline of the resistor followed by laser trimming if needed, to precisely control the value of the resistor. Because the resistor material is of consistent thickness, laser trimmed resistors will track each other over temperature variations adding to the performance of the circuit. Another added feature to resistor values is the incorporation of ladder resistors. Generally a design containing low value resistors for termination and high value resistors for power sensing creates a dilemma for choosing a sheet resistance. Ladder resistors alleviate the high resistor value problem by creating an efficient serpentine style layout with enhanced trimming capabilities. By trimming groups of rungs from the ladder, very high values (greater than 100K) can be achieved with a nominal sheet resistance. For more detailed information, including serpentine resistor requirements, resistor power handling and ladder resistors, consult EFI Technologys separate resistor guide and a EFI sales engineer. Table 4 outlines some specifics related to resistors.

Conductor Features

Innovations in photoresist patterning have allowed Vishay EFI Technology to offer fine line features (< 2 mils) or high volume assemblies. Although a thorough design eview is necessary to incorporate features under 0.002, any applications can benefit from the improvements by incorporating inductors, couplers and low value capacitors.

Spiral Inductors

High quality inductors offer the designer the option of integrating increased functionality with no additional cost to manufacture. Circular or rectangular spiral inductors using low loss metallization can create inductor structures with high Q (50 min at 10 MHz) further reducing discrete parts. An additional feature is a thick film connection (addressed later in this guide) to the center of the inductor eliminating bonding and increasing reliability.

Other Fine Line Features

Couplers require all facets of the environment be considered for applicability. Operating frequency, substrate thickness, substrate material, metal thickness, linewidths, spacings and interconnects are all elements determining a couplers performance. Consult your EFI Technology sales engineer for assistance in integrating couplers into designs.

Table 2 - Standard Metalization

-A- Side		
TaN	500, 100	Other sheet resistives available
Ti	1500 A ± 250 A	Adhesion layer if no resistors
Ti/Pd	1500 A ± 250 A	Alloy
Cu	3 - 10 Micron	Overall range
Ni	1 - 3 Micron (electroplated)	Electroless Ni available
Au	1 - 3 Micron	
-B- Side		
Ti	1500 A ± 250 A	
Ti/Pd	1500 A ± 250 A	
Cu	3 - 10 Micron	Overall range
Ni	1 - 3 Micron (electroplated)	Electroless Ni available
Au	1 - 3 Micron	

Minimum Line Width	2.0 mils	1.5 mils available
Minimum Gap	2.0 mils	1.5 mils available
Pullback from substrate edge	2.0 mils	Minimum
Sheet resistance	2.0 mΩ	Typical only, metal thickness will determine final value

Intergrated Capacitors

This type of capacitor permits the designer to realize a planar capacitor up to two picofarads in value using closely spaced fingers. A number of published articles referenced in EFIs guide to thin film capacitors detail closed form design equations for this type of capacitor as a function of width, spacing, number of fingers, and length. Commercially available microwave simulation tools provide accurate library models for interdigitated capacitor analysis.

Plated Via Holes

Plated via holes offer the designer a proven, high reliability method of introducing signal or ground plane connections at strategic points within a circuit. Plated via holes are available in a range of sizes based upon the substrate thickness. Refer to Table 5 for design parameters of plated via holes. EFI's unique process technology permits high aspect ratio vias with superb mechanical integrity.

Cost-effective High Volume Interconnect Substrate Solutions

Filled Vias

Vishay EFI Technology has taken its high quality, reliable gold filled via process and adapted it for use in high volume manufacturing using solid copper as the filling material. Features such as planar surface for die mounting directly on the via, wire bondable solid vias, low inductance, low resistance ground paths and isolating circuit attachment material from the circuit area are typical improvements. In addition, solid copper offers a superior thermal path for heat transfer from active die and a method for I/O in CSP applications. Also available are solid copper slots (see table 7) for improved heat transfer over a larger area. Consult table 6 for parameters related to filled vias.

Conductivity

Vishay EFI Technology also offers selective high conductivity traces to optimize the performance of your circuit for specific criteria. Mostly used in high current applications where resistive losses to active die are undesirable, this technology is also applicable to filter structures where high Q and performance are critical. Consult EFI Technologys design guide for high conductivity traces for further information.

Thick Film Interconnects

For high volume applications, reducing bond count is a significant cost advantage for both manufacturing and reliability. Integrated spiral inductors, DC routings and other interconnects require additional space be allocated for wire bond connections. Vishay EFI Technology has introduced a thick film interconnect capability with a proven thick film to thin film interface eliminating the need for wire bonds in these areas. This allows circuit density to increase offering more value in the same package size. Similar in application to EFI Technologys air bridges, the base level thick film circuit is passivated, allowing thin film patterns to cross it, thus increasing circuit density. General trace routing can also be done on the thick and thin film layers. An MIC sales engineer will gladly assist in incorporating interconnects into your design.

Table 3 - Solder Mask & Insulator Parameters

Vacred solder mask	
Thickness	3.0 mils
Maximum temperature	260 °C, 60 seconds 280 °C, 20 seconds
Minimum feature width	10.0 mils
Minimum gap	10.0 mils
Minimum conductor overlap onto ceramic or pullback	3.0 mils
Minimum freestanding soder dam	10.0 x 20.0 mils
Distance to circuit edge	5.0 mils Minimum
Application side	-A- or -B- or both

Ni Oxide solder stop		
Length	15.0 mils	Minimum
Width	2.0 mils	
Distance to circuit edge	Full conductor width + 6 mils	Minimum
Application side	-A- or -B- or both	

Metal System

Vishays EFI Technologys volume manufacturing relies primarily on a consistent proven metal system. Resistors, as previously stated, are created with a layer of Tantalum nitride deposited on the substrate surface. Base conductor layers consist of sputtered Titanium and Palladium fol owed by plated Copper, Nickel and Gold. These plated met ls allow some variation for specific applications such as conductivity (thicker copper) or solderability (thinner gold). Other metal systems have selected availability based on circuit design and volume. See Table 2 for a review of metallization thicknesses.

Solder Stop

Two options exist for this feature, allowing the designer to incorporate varying levels of passivation to a circuit. First, a nickel oxide layer may be patterned within the confines of the circuit. The oxide creates a solder barrier prohibiting solder spread. The second option consists of adding a glass material to the surface of the ceramic and patterning this material. The overlay that results creates not only a solder stop, but a passivation to the circuit. This allows low bond height if necessary, without a chance for contact with the circuit area crossed by the bond. Table 3 contains the design parameters for this feature.

Cost-effective High Volume Interconnect Substrate Solutions

Table 4 - Resistors Parameter

Parameter	Value - inches (µm)	
Resistor Material	TaN	Alternative materials available
Sheet Resistance	50, 100 Ω	Alternative values available
Reistor Style	Type - 1	Resistor inboard of conductor
Resistor Tolerance	± 1 - 20 % trimmed	Lower values require a higher % tolerance
Minimum etched resistors	0.004 x 0.004 (100 x 100)	Ladder resistors available at 1.2 mils
Minimum probe pad dimension	0.008 x 0.008 (200 x 200)	
Conductor/ Resistor overlap	0.002 (50) (minimum)	per side Perpendicular to current flow including termination block widths
	0.003 (75) per end	Parallel to current flow (on resistor mask)
Layout Dimensions		
Standard resistor	80 % of value	Based on L/W x R_{sheet}
Serpentine resistor	120 % of value including kerf	Based on 1.3 mil laser kerf
Trim style	Plunge/ Serpentine/ Scan	Consult factory for ladder resistors

Table 5 - Plated Via Hole Parameters

Parameter		
Resistor Material	± 3 mils (± 75 µm)	
Sheet Resistance	100	
Reistor Style	± 2 mils (± 50 µm)	From a fixed datum
Resistor Tolerance -	-A- face: -B- face:	Via diameter + 10 mils Via diameter + 14 mils

Substrate Height	Plated Via Diameter	Via spacing edge to edge	Via spacing edge to circuit edge
0.015" (0.375 µm)	0.012" - 0.100" (0.300 µm - 2.5 µm)	0.020" (0.5 µm)	0.020" (0.5 µm)
0.015" (0.375 µm)	0.012" - 0.100" (0.300 µm - 2.5 µm)	0.020" (0.5 µm)	0.020" (0.5 µm)
0.015" (0.375 µm)	0.012" - 0.100" (0.30 µm - 2.5 µm)	0.020" (0.5 µm)	0.020" (0.5 µm)

Table 6 - Filled Via Parameters

Parameter		
Thermal Conductivity	393 W/M °C	Thermal conductivity of pure CU
Maximum via count per square inch	100	1200 per herman
Locational Tolerance	± 2 mils (± 50 µm)	From a fixed datum
Minimum capture pad diameter	-A- face: -B- face:	Via diameter + 10 mils Via diameter + 14 mils

Substrate Height	Plated Via Diameter	Via spacing edge to edge	Via spacing edge to circuit edge
0.015" (0.375 µm)	0.012" - 0.018" (0.300 µm - 0.450 µm)	0.020" (0.500 µm)	0.020" (0.500 µm)
0.020" (0.500 µm)	0.016" - 0.024" (0.400 µm - 0.600 µm)	0.020" (0.500 µm)	0.020" (0.500 µm)
0.025" (0.625 µm)	0.020" - 0.030" (0.500 µm - 0.750 µm)	0.020" (0.500 µm)	0.020" (0.500 µm)

Table 7 - Solid Copper Slot Parameters

Substrate Height	Slot size	Spacing edge to edge of nearest via	Slots spacing to circuit edge or additional slot
0.020" (0.500 µm)	0.016" - 0.032" (0.400 µm - 0.800 µm)	0.020" (0.500 µm)	0.060" (1.500 µm)
0.025" (0.625 µm)	0.020" - 0.040" (0.500 µm - 1.000 µm)	0.020" (0.500 µm)	0.060" (1.500 µm)

Table 8 - Thick Film Crossunder Design Parameters

Material	DuPont	
Resistivity	5 mΩ	Typical
Thickness	0.001"	Typical
Minimum Width	0.005"	
Minimum Length	0.030"	
Minimum Spacing	0.060"	Edge to Edge
Interconnect Length	0.010"	Minimum
Crossunder Patterns	Allowed	

Cost-effective High Volume Interconnect Substrate Solutions

Glaze (Crossunder Passivation, GL)

Material	DuPont	
Thickness	0.002"	Typical, 2 levels applied
Minimum Width	0.017"	Centered over XUN
Minimum Length	0.018"	Centered over XUN
Thin Film Overlap	0.002"	Minimum

Thin Film Over Glaze

Direction	Perpendicular to XUN	Parallel allowed, review required
Minimum Width	0.003"	
Minimum Spacing	0.004" (100 µm)	
Minimum distance to edge of glaze	0.005" (150 µm)	

Summary

Vishays EFI Technology has the capability and flexibility to meet the requirements of today's commercial markets. Our high volume, high throughput manufacturing facility is capable of meeting the requirements of virtually all volume commercial and military applications, cost effectively.

The innovations used result in extremely high yielding, high performance interconnects. Using conveyorized "touchless" systems as a manufacturing platform reduces the defect rate, thus allowing for significant cost reductions.