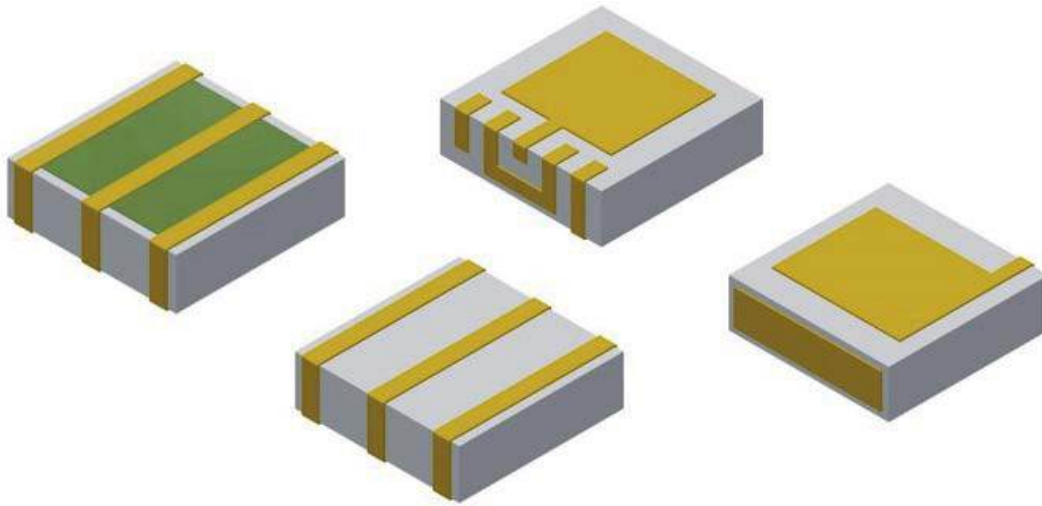


Side Wall Patterning - Custom Substrate



CAPABILITIES

- Conductor patterning on 4 surfaces
- Wire-bondable or solderable metalizations
- Allows attachment to side wall of substrate
- Tight dimensional tolerances

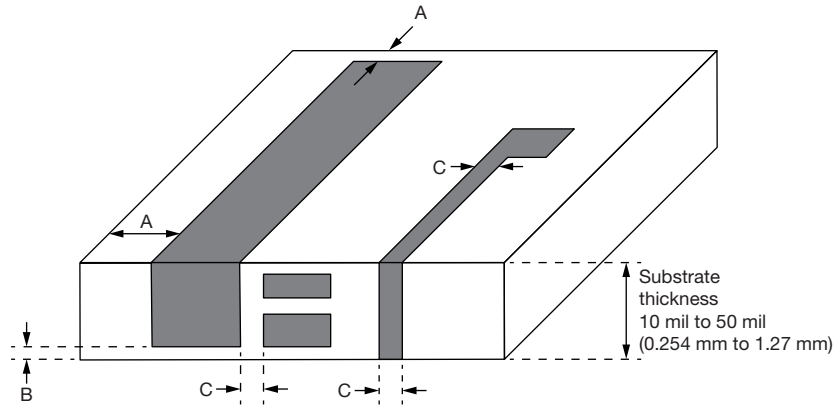
APPLICATIONS

- Electro-mechanical or electro-optical applications that require an interface between the electric circuit and an element such as a mirror, lens, fiber, etc.
- High frequency circuits such as RF application, and high bit rate transceivers (TOSA / ROSA) that benefit by replacing wire bonds with side-patterned traces
- Applications that require a high degree of miniaturization

DESIGN SPECIFICATIONS AND RULES

- Substrate materials: alumina or AlN. Sidewall patterning can be deposited on plates ranging between 10 mils and 50 mils. Polished plates are preferred due to their tighter thickness tolerance.
- Metalization: TiW / Au, TiW / Ni / Au or TiW / Pd / Au as well as resistor and AuSn metalization available.
- Lines and gaps: lines and gaps down to 0.003" (75 microns) can be patterned on the component sidewalls.
- Pullback from bottom edge: traces designed to reach the bottom edge of the sidewall will require a ± 2 mil tolerance. Positive tolerance represents a gap from the bottom edge; negative tolerance represents metal wrapping around edge to the rear surface.
- Geometric tolerances down to ± 1 mil ($\pm 25 \mu\text{m}$) can be maintained on sidewall geometries. Tolerances between metal on diced edges of the ceramic tile down to ± 2 mil.
- Connectivity: side wall patterns can be isolated (standalone), connected to front side only (half wrap) or connected to both front and rear sides (full wrap).
- Component with sidewall patterning can have integrated resistors or AuSn solder pads embedded on the front or rear surfaces. These capabilities are not allowed on the sidewall itself.

| DESIGN SPECIFICATIONS | |
|---------------------------------------|--|
| Plate Thickness | 0.010" to 0.050" |
| Minimum Gap | 0.003" |
| Dimensional Tolerance | ± 0.001 " |
| Metal Pattern to Diced Edge Tolerance | ≥ 0.002 " |
| Metal Systems | TiW / Au / Au plate or TiW / Pd / Au |
| | TiW / Au / Ni plate / Au plate |
| | TaN / TiW / Au or NiCr / TiW / Au |
| | 80 / 20 AuSn pads available, consult factory |

SIDE WALL PATTERNING DESIGN RULES


| A | B | C |
|--|--|---|
| Best alignment of metal to diced edges $\pm 0.002'' (\pm 50 \mu\text{m})$ | Metal pullback from bottom edge Typical: $0.002'' \pm 0.002'' (50 \mu\text{m} \pm 50 \mu\text{m})$ or $0'' \pm 0.002'' (0 \mu\text{m} \pm 50 \mu\text{m})$ Negative values wrap to rear side. | Line or gap $0.003'' (75 \mu\text{m})$ min. Typical tolerance: $\pm 0.002'' (\pm 50 \mu\text{m})$ Tight tolerance to $\pm 0.001'' (\pm 25 \mu\text{m})$ allowed in some cases |

CONTACT INFORMATION

 For design assistance, contact: efi@vishay.com
GLOBAL PART NUMBER INFORMATION

Global Part Numbering example: SDWP20xxxx-00Q

| | | | | | | | | | | | | | |
|-------|---|---|---|---------------------------------|---|--|--|--|--|-------------------|---|---|---|
| S | D | W | P | 2 | 0 | | | | | - | 0 | 0 | Q |
| Model | | | | Sequential: assigned by factory | | | | | | Internal revision | | | |



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