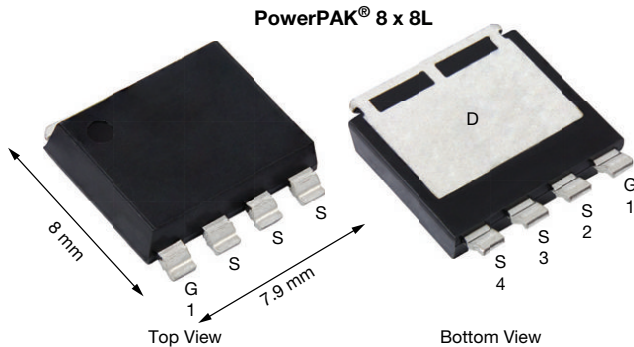


N-Channel 40 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00052
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00074
Q_g typ. (nC)	99
I_D (A) ^a	608
Configuration	Single

FEATURES

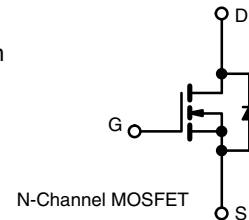
- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device
- Very low $R_{DS} \times Q_g$ figure of merit (FOM)
- 50 % smaller footprint than D²PAK (TO-263)
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- OR-ing
- Motor drive control
- Battery management



ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SIJH400E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	+20, -16	V
Continuous drain current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	608
		$T_C = 70$ °C	509
		$T_A = 25$ °C	57 ^b
		$T_A = 70$ °C	47 ^b
Pulsed drain current ($t = 100$ μ s)	I_{DM}	800	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	350
		$T_A = 25$ °C	3 ^b
Single pulse avalanche current	I_{AS}	82	mJ
Single pulse avalanche energy	E_{AS}	338	
Maximum power dissipation	P_D	$T_C = 25$ °C	385
		$T_C = 70$ °C	269
		$T_A = 25$ °C	3.3 ^b
		$T_A = 70$ °C	2.3 ^b
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	36	45	°C/W
Maximum junction-to-case (drain)				

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



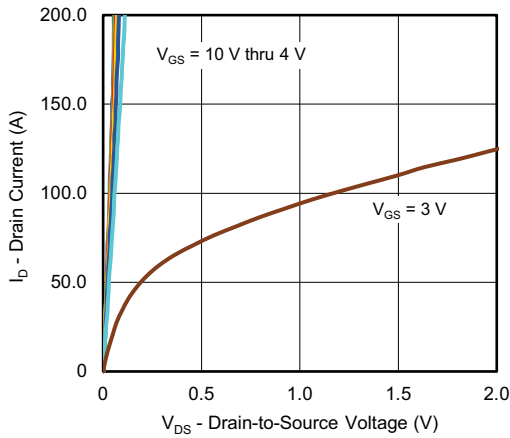
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	24	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-7.8	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1	-	2.4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00041	0.00052	Ω
		V _{GS} = 4.5 V, I _D = 20 A	-	0.00058	0.00074	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 75 A	-	290	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	15 050	-	pF
Output capacitance	C _{oss}		-	3115	-	
Reverse transfer capacitance	C _{rss}		-	240	-	
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 20 A	-	220	330	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 20 A	-	99	148	
Gate-source charge	Q _{gs}		-	50	-	
Gate-drain charge	Q _{gd}		-	12	-	
Gate resistance	R _g	f = 1 MHz	0.2	1.1	2.2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	22	45	ns
Rise time	t _r		-	15	30	
Turn-off delay time	t _{d(off)}		-	90	180	
Fall time	t _f		-	16	35	
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	80	160	
Rise time	t _r		-	125	250	
Turn-off delay time	t _{d(off)}		-	95	190	
Fall time	t _f		-	80	160	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	350	A
Pulse diode forward current	I _{SM}		-	-	800	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.7	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	75	150	ns
Body diode reverse recovery charge	Q _{rr}		-	155	310	nC
Reverse recovery fall time	t _a		-	46	-	ns
Reverse recovery rise time	t _b		-	29	-	

Notes

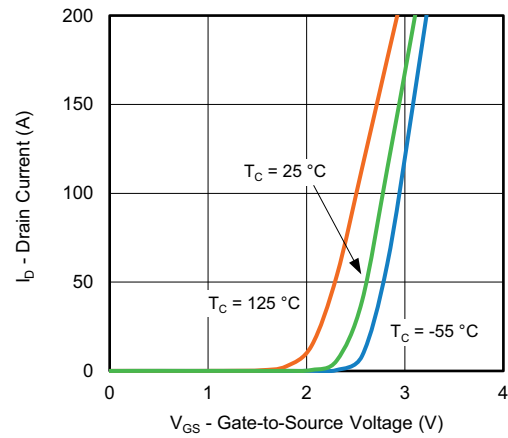
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

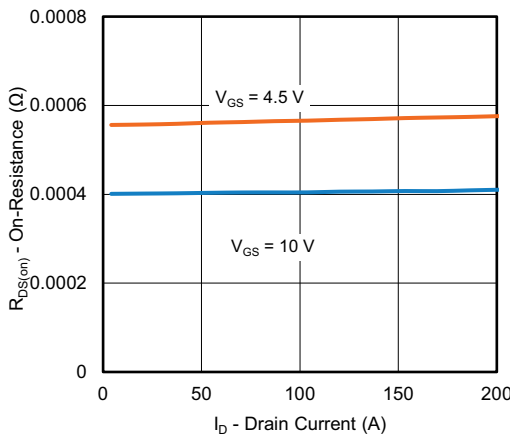
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



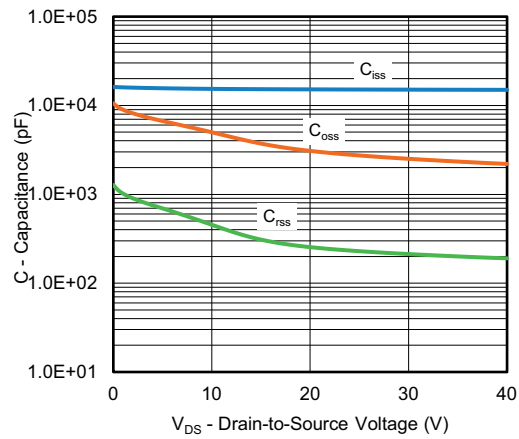
Output Characteristics



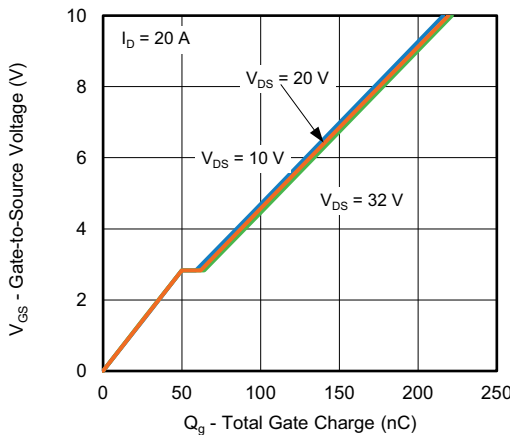
Transfer Characteristics



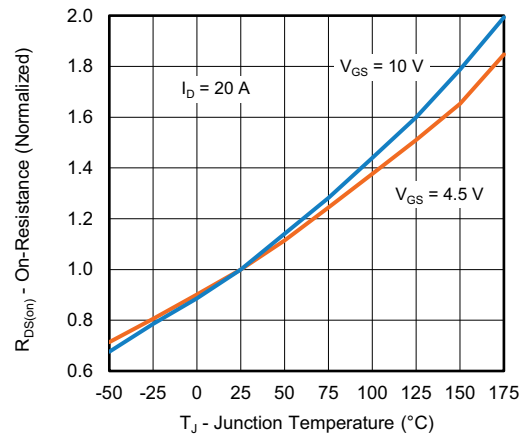
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



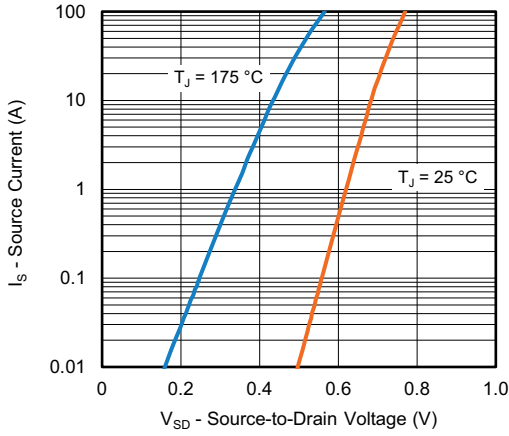
Gate Charge



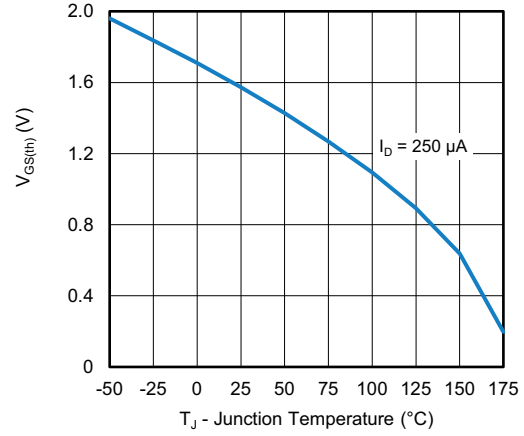
On-Resistance vs. Junction Temperature



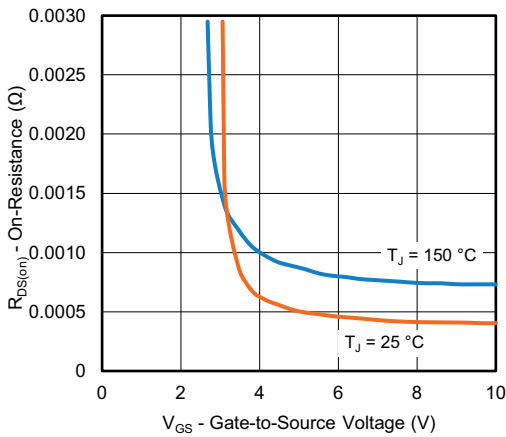
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



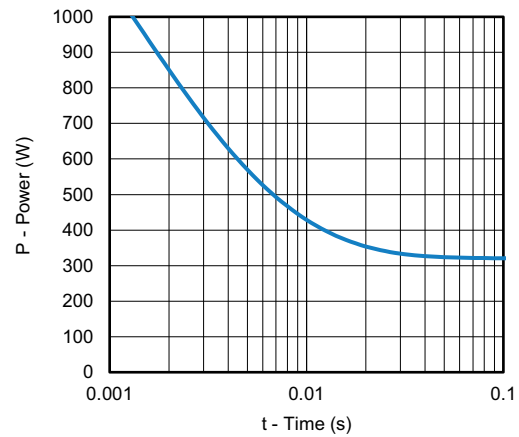
Source-Drain Diode Forward Voltage



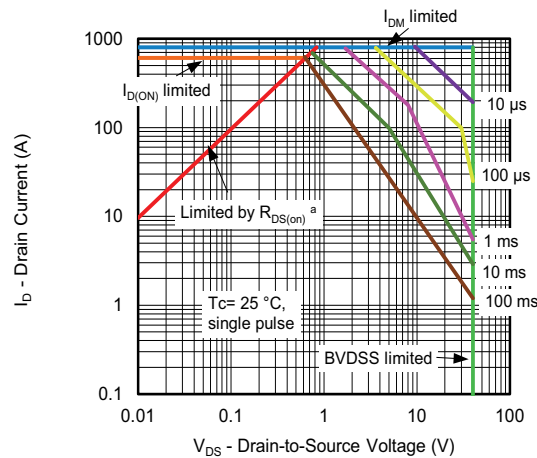
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



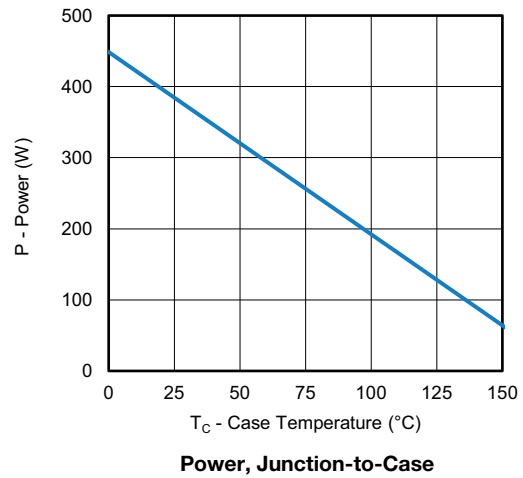
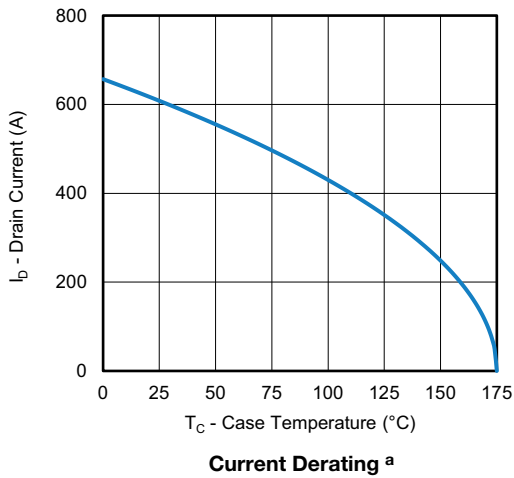
Safe Operating Area, Junction-to-Case

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

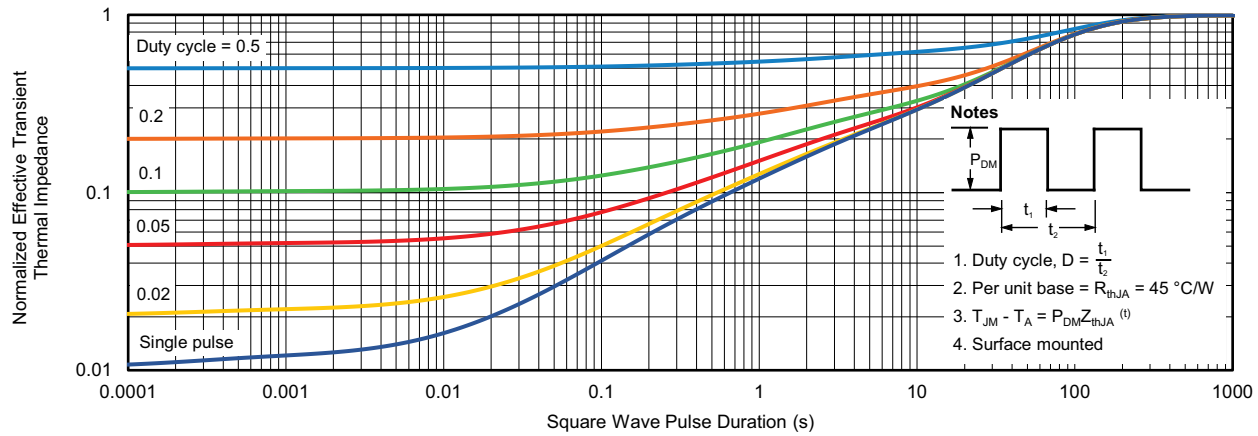


Note

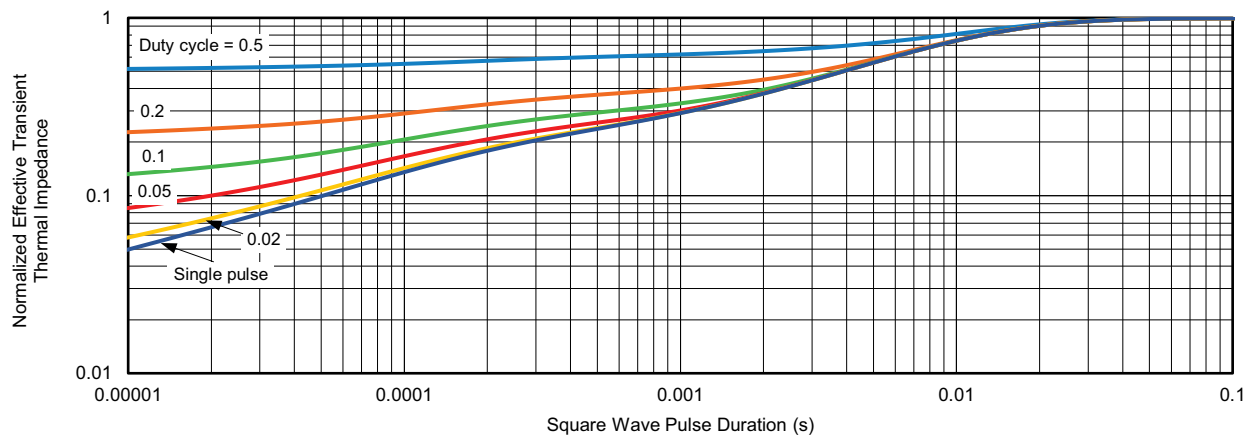
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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