18 V, 60 A, 0.6 mΩ $R_{DS(on)}$ Hot-Swap eFuse Switch

DESCRIPTION

The SiC32311 is a programmable hot swap e-fuse for high current applications such as servers, data storage, and communication products. It contains a high-side MOSFET and other control circuitry that enables it to work as stand-alone device, or to be controlled by a hot-swap controller. The SiC32311 drives up to 60 A of continuous current per device.

The SiC32311 limits the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop.

The device offers many features to simplify system designs. It provides an integrated solution for monitoring output current and die temperature, eliminating the need for an external current sensing shunt resistor, power MOSFET, and thermal sensing device.

The SiC32311 detects the power FET gate, source, and drain short conditions, in addition to feedback to the controller. SiC32311 can be operated in parallel for higher current applications. The SiC32311 is available in a PowerPAK MLP32-55.

FEATURES

- 4.5 V to 18 V operating input range
- 25 V guaranteed maximum input tolerance
- 2.3 ms moderate OCP blanking time
- Maximum 60 A output current
- Integrated switch with lower $R_{DS(on)}$ of 0.6 mΩ
- Built-in MOSFET driver
- Integrated current sensing with sense output
- Separate current sensing output used to program over-current value
- Built-in soft start and insertion delay
- Output short-circuit protection
- Over-temperature protection
- Built-in fuse health diagnostics
- Fault status report
- Parallel operation for higher current applications
- Analog temperature report
- Available in a PowerPAK MLP32-55 package

APPLICATIONS

- Hot swap
- PC cards
- Disk drives
- Servers
- Networking

TYPICAL APPLICATION CIRCUIT

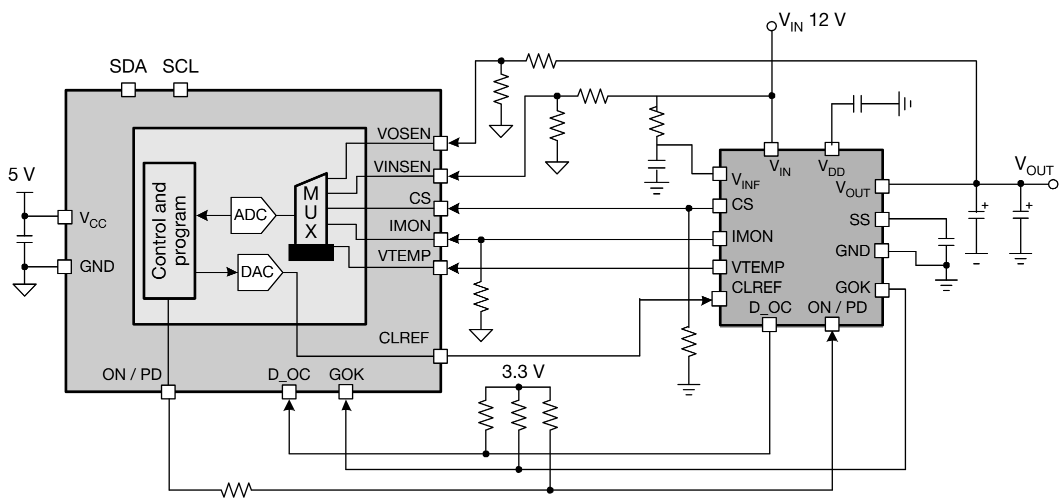


Fig. 1 - Typical Application Circuit

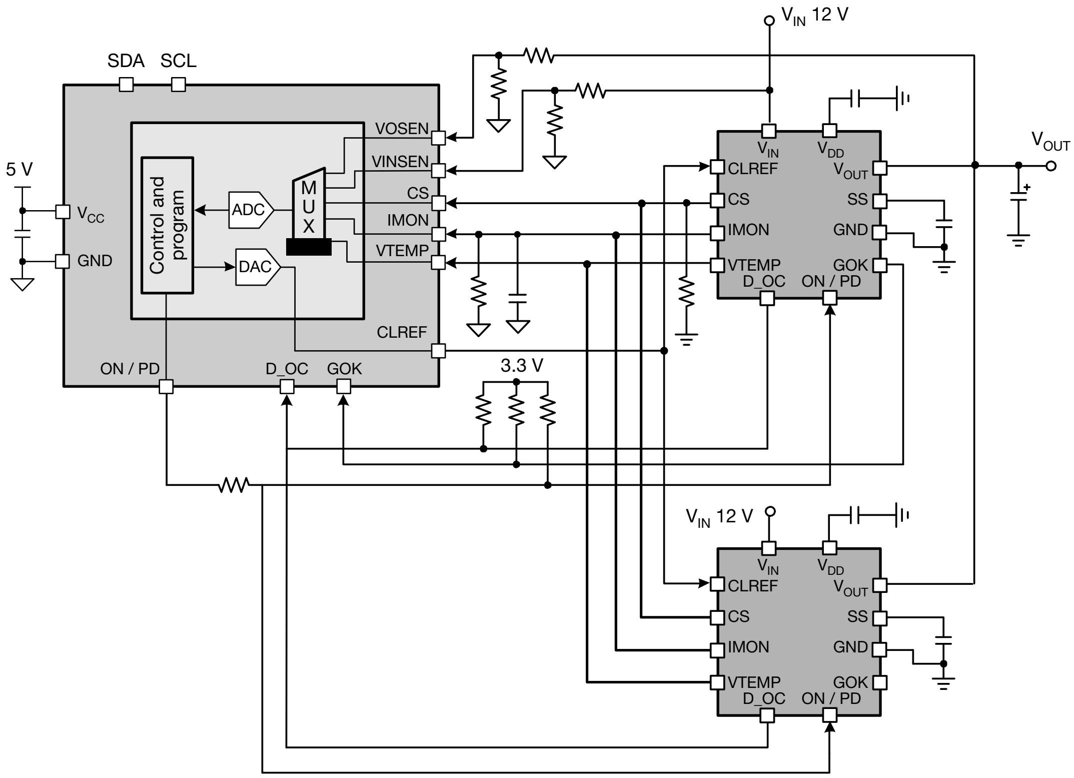


Fig. 2 - SiC32311 Typical Application Diagram

PINOUT CONFIGURATION

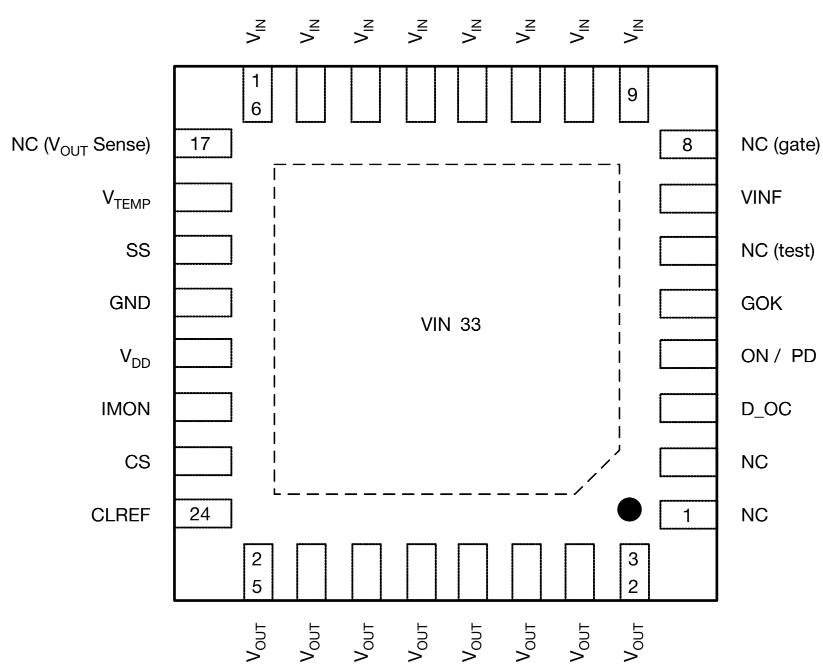
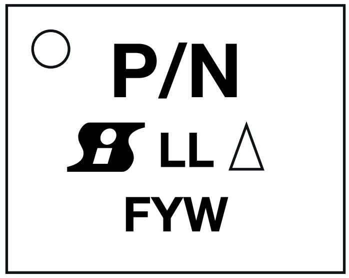


Fig. 3 - Pins Out Configuration (Top View)

ORDERING INFORMATION				
PART NUMBER	PACKAGE	FAULT RESPONSE	ALERT PINS	MARKING CODE
SiC32311CD-T5E3	PowerPAK MLP32-55	Switch off, and latch upon fault event	GOK, D_OC	SiC32311
SiC32311EVB	Reference board			

PIN DESCRIPTION		
PIN	NAME	FUNCTION
1, 2	NC	May connect to GND, V_{OUT}, or left floating
3	D_OC	Digital output of over-current indication. D_OC is an open-drain output. When the voltage on CS is higher than 83 % x VCLREF, D_OC logic is pulled low. This pin has an internal 2 MΩ pull-down resistor to artificially pull low in case the external pull-up resistor is missing
4	ON / PD	Power FET on / off control or OUT voltage pull-down mode control. Drive ON / PD higher than 1.4 V to turn on the power FET after setting ON / PD equal to 1.1 V for 2 ms will cause the controller to recognize a V_{OUT} discharge request. The power FET will begin to discharge with a 500 Ω internal resistor. Drive ON / PD below 0.8 V to open the power FET. A 1 MΩ resistor connects ON / PD to GND just in case it is floating when power input is under UVLO threshold.
5	GOK	If a fault is detected, GOK will pull low, and the switch is turn off. If the fault is caused by an OVER-CURRENT event, OVER-TEMPERATURE event or OVER-POWER event, then the GOK will latch. Other faults monitored which do not cause a latch unless the 200 ms soft-start timer expires are DRAIN-SHORT short, GATE-SOURCE short, GATE-DRAIN short, and SOFT-START FAIL. The OVER-CURRENT event will cause a GOK latch immediately if the current is greater than 100 A or if the CS voltage is greater than the CLREF voltage for 2.3 ms. Power or ON / PD cycling is required if the GOK latches. FET health is monitored at startup via DRAIN / GATE / SOURCE short detection but does not latch GOK unless 200 ms timer expires. This pin has an internal 2 MΩ pull-down resistor to artificially pull the signal low in case the external pull-up resistor is missing
6	NC (TEST)	Do not connect to this pin; leave floating
7	V_{INF}	This pin is an optional filtered V_{IN} pin. Connect an appropriate RC filter to filter noise on V_{IN}
8	NC (Gate)	Leave floating or connect a 33 nF capacitor to GND if load could oscillate at greater than 4 kHz at initial power on with single configuration circuit design
9 to 16	V_{IN}	System input power supply. The SiC32311 operates from a +4.5 V to +16 V input rail.
17	NC (V_{OUT} Sense)	V_{OUT} Sense pin. Connect to V_{OUT} or leave floating
18	V_{TEMP}	Junction temperature sense output. The output temperature equals 200 mV + 10 mV/°C x T_J
19	SS	The SS pin is the ramping control for soft-start ramping rate. An internal fixed current source charges an external capacitor in linear fashion. The V_{OUT} voltage soft-starts at a rate that tracks the soft-start capacitor. If soft-start has not completed within 200ms, a fault is declared. In the event that the soft- start ramp is too fast and causes in-rush current to charge V_{OUT} with too much current, the CLREF reference will override (slow down) the soft-start ramp rate. The ramping voltage on the SS pin will equal 10 % of the V_{OUT} voltage during ramping
20	GND	Signal ground
21	V_{DD}	Internal 5 V LDO output. Place a 1 µF decoupling capacitor close to V_{DD} and GND
22	I_{MON}	Current monitor output. The output current is proportional to the current flowing through the power device. The I_{MON}/I_{OUT} gain is 10 µA/A with 5 µA off set
23	CS	Current sense output. CS requires an external resistor. The V_{CS} voltage is compared with CLREF to determine the current limit
24	CLREF	Current limit reference voltage input. An internal 10 µA current is sourced from this pin to an external resistor. During soft-start, this current is further internally limited such that the developed external voltage is not more than 100 mV when V_{OUT} is less than 3.25 V, 150mV when V_{OUT} is between 3.25 V and 40% of VIN, 500 mV (approximately) when V_{OUT} is between 40 % and 80 % of V_{IN}. When V_{OUT} is 80 % of V_{IN} or higher, the CLREF voltage is set by external resistor. The max settable voltage on this pin is 1.6 V. This pin can be manually controlled / driven by an external DAC that can overdrive 10 µA.
25 to 32	V_{OUT}	Output voltage controlled by the IC. OUT is connected to the source of the integrated MOSFET
33	V_{IN}	Input of hot swap power switch

MARKING CODE



Format:

- Line 1: part number
- Line 2: Siliconix logo, lot code, and ESD logo
- Line 3: factory code, year code, work week code

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Input voltage	V_{IN}, V_{INF}	-0.3	+25	V
Output voltage (DC)	V_{OUT}	-0.3	+25	V
Output negative voltage (10 µs)		-3	-	V
Output negative voltage (500 µs)		-1	-	V
Internal 5 V LDO output	V_{DD}	-0.3	-0.3 to +6	V
All other pins		-0.3	-0.3 to V_{DD} + 0.3	V
Operating junction temperature range	T_J	-40	+150	°C
Lead temperature	T_{SLD}	-	260	°C
Storage temperature	T_{STG}	-65	+150	°C
Pin 17 ''V_{OUT} Sense'' voltage range		Internally limited		
Pin 8, gate voltage range (V_{GATE} - V_{OUT})		-20	20	V
Maximum continuous switch current		-	60	A
Electronstatic discharge, human body model (per EIA/JESD22-A114)	ESD_{HBM}	-	2	kV
Electronstatic discharge, charge device model (per EIA/JESD22-A115)	ESD_{CDM}	-	1.5	kV
Maximum latch-up current limit (per JESD78 class II)	I_{LU}	-	100	mA
Moisture sensitivity level	MSL	Level 1		
Storage	T_{STG}	-55	+125	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage (V_{IN})	4.5	-	18	V
Maximum continuous output current	-	-	60	A
Maximum peak output current	-	-	80	A
V_{DD} output capacitance range	2.2	-	10	µF
CLREF voltage range	0.2	-	1.6	V
Operation junction temperature	-40	-	+125	°C

THERMAL CHARACTERISTICS			
THERMAL PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
Thermal resistance, junction to ambient	$R_{\theta JA}$	17	°C/W
Thermal resistance, junction to case, V_{OUT} lead	$R_{\theta JCL}$	1.9	°C/W
Thermal resistance, junction to case, center of exposed pad	$R_{\theta JCB}$	1	°C/W

Note

- Thermal resistances are obtained by measurement with part mounted on evaluation board

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS V_{IN} = V_{INF} = 12 V, ON / PD = 3.3 V, CVINF = 0.1 μF, CVDSS = 4 μF, CVTEMP = 0.1 μF, RVTEMP = 1 kΩ, CSS = 100 nF, MIN. / MAX. LIMITS ARE OVER THE JUNCTION TEMPERATURE RANGE OF -40 °C TO +125 °C UNLESS SPECIFIED OTHERWISE, TYP. VALUES AT T_A = 25 °C	LIMITS MIN.	TYP.	MAX.	UNIT
Supplies Current						
Quiescent current	I_Q	V_{ONPD} = 3 V, no load	-	3.15	-	mA
		Fault latch off	-	6.5	-	μA
		V_{ONPD} = 0 V	-	6.15	-	mA
V_{DD} Regulator and UVLO						
Regulator output voltage	V_{VDD}	I_{VDD} = 0 mA, V_{INF} = 6 V	-5%	5	5%	V
V_{DD} current limit			40	70	-	mA
V_{DD} drop out voltage		V_{INF} = V_{IN} = 4.5 V, I = 20 mA	-	140	210	mV
V_{IN} Under Voltage and Over Voltage Protections						
V_{IN} under voltage lockout threshold rising	V_{VIN_THR}		-	4.2	-	V
V_{IN} under-voltage lockout hysteresis	V_{VIN_THF}		70	105	-	mV
ON / PD						
Internal current source	I_{ON_PD}		3.8	4.2	4.6	μA
FET on insertion delay time	t_{ON_DLY}	**Note:** 1 ms timer begins after ON_PD pin transitions above 1.4 V	-	1	-	ms
FET on high-level input voltage	V_{ON_Hi}		1.25	1.35	1.45	V
FET on-state hysteresis	V_{ON_Hyst}		-	0.1	-	V
Switch off discharge upper threshold	V_{PD_Hi}	**Note:** ON / PD must be held continuously between the value of 0.8 V and 1.2 V for 80 μs before command to discharge is recognized. Discharging will commence 2 ms after command is recognized	-	1.2	-	V
Switch off discharge lower threshold	V_{PD_Lo}		-	0.8	-	V
PD mode pull-down resistor	R_{PL_DN}	Internal resistor from V_{OUT} to ground through PD controlled functionality	-	625	-	Ω
PD mode pull-down delay time	$t_{PL\_DN\_DLY}$	**Note:** This 2.08 ms is the summation of the 80 μs recognition time and 2 ms delay time	-	2.05	-	ms
ON / PD pull-down resistor	R_{PL_ONPD}	Discharge resistor on ON / PD pin activated while V_{IN} not ready	-	1	-	MΩ
Soft-Start						
Pull-up current	I_{SS}	T_J = 25 °C	4.5	5.2	6	μA
Gain to V_{OUT}	AVSS	30 %	8.6	10.4	12.2	V/V
		60 %	9.35	10.3	11.25	V/V
		90 %	9.6	10.3	11	V/V
SS pulldown voltage	VOL_SS	0.1 mA into pin during ON delay	-	6.7	-	mV
GOK Output						
Output low current capability	I_{GOK_ACTIVE}	V_{GOK} = 0.2 V	20	30	45	mA
GOK off-state leakage current	I_{GOK_LKG}	V_{GOK} = 5 V **Note:** There is an intentional internal 2 MΩ pull down resistor	-	2.7	-	μA

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS $V_{IN} = V_{INF}$ = 12 V, ON / PD = 3.3 V, CVINF = 0.1 μF, CVDSS = 4.7 μF, CVTEMP = 0.1 μF, RVTEMP = 1 kΩ, CSS = 100 nF, T_J = 25 °C	LIMITS			UNIT
			MIN.	TYP.	MAX.	
I_{MON}						
Sense gain			-	10	-	μA/A
Pre-bias offset current			-	5	-	μA
I_{MON} accuracy (1)	I_{MON_ACC}	0.5 A ≤ I_{OUT} ≤ 3 A	I_{OUT} - 0.5	-	I_{OUT} + 0.5	A
		I_{OUT} = 5 A	-4.5	-	+4.5	%
		I_{OUT} = 10 A	-3	-	+3	%
		I_{OUT} = 50 A	-3	-	+3	%
Over-current threshold for D_OC signal pulling down	V_{DOC_TH}		83	87	90	%
Short - Circuit Protection						
Short-circuit current trip point	I_{SC}		-	100	-	A
Response time (1)	t_{SC}		-	200	-	ns
CLREF						
Internal current source	I_{CLREF}		9.5	10	10.6	μA
Internal max. current limit clamp at various V_{OUT} levels	V_{CLREF_CLMP}	V_{OUT} < 40 % V_{IN} (relevant for shorted output during startup)	80	100	125	mV
		3.25 V < V_{OUT} < 40 % V_{IN}	120	150	185	mV
		40 % V_{IN} or 3.25 V whichever is higher < V_{OUT} < 80 % V_{IN}	435	500	555	mV
		V_{OUT} > 80 % V_{IN}	1.45	1.6	1.7	V
Over-current blanking time	$t_{CL\_REG\_OC}$	During normal operation	1.8	2.3	3.3	ms
CLREF current source clamp voltage			-	1.6	-	V

Notes

(1) Guaranteed by design and characterization
(2) Typical limits are established by characterization and are not production tested
(3) Min. and Max. Parameters are not 100% production tested

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS V_{IN} = 12 V, V_{DD}, = 5.0 V, T_J = 25 °C, unless otherwise noted	LIMITS MIN. (3)	 TYP. (2)	 MAX. (3)	UNIT
D_OC Output						
D_OC pull down current	I_{DOC_ACTIVE}	V_{DOC} = 0.1 V	-	10	-	mA
D_OC off-state leakage current	I_{DOC_LKG}	**Note:** There is an intentional internal 2 MΩ pull down resistor	-	2.7	-	µA
D_OC flag response time (1)		Load current cross from 80 % to 90 % in 1 µs, both rise and fall of VSC	-	1	5	µs
VTEMP						
Sense Gain		Sense range 0 °C to 140 °C	-	10	-	mV / °C
Sense Offset			410	450	490	mV
Pull down current			-	50	-	µA
Thermal Shutdown						
Thermal shutdown temperature	T_{THDN}	GOK pulls low	-	140	-	°C
Power MOSFET						
On resistance	$R_{DS(on)}$		-	0.6	0.8	mΩ
		T_J = 85 °C	-	0.7	-	mΩ
FET Health Diagnostic (Fault Detection)						
FET VDS short threshold	V_{SCTH_DS}	Startup postponed if $V_{OUT} > V_{SCTH\_DS}$ anytime after postponed **(Note: this is a non-latching fault)**	-	80	-	%
FET VDS short release threshold. (short flag removed threshold)	V_{DS_OK}	Startup resumed if $V_{OUT} < V_{DS\_OK}$ anytime after postponed	-	70	-	%
FET gate to drain short threshold	V_{SCTH_DG}	Startup postponed if V_G is less than V_{SCDG_TH} at $V_{ON} > V_{ON\_HI}$ transition. It will resume once it is below V_{DG_OK} **(Note: this is a non-latching fault)**	-	2.2	-	V
FET gate to drain short OK threshold	V_{DG_OK}	Startup resumed if $V_G < V_{DG\_OK}$ anytime after postponed	-	2	-	V
VG low threshold	V_{G_TH}	Restart / latch if $V_{GD} < V_{G\_TH}$ after t_{SS_MAX}. During normal operation, it will be a flag and triggers restart / latch	-	7	-	V
V_{OUT} low threshold	V_{OUTL_TH}		-	90	-	%
FET maximum gate fault timer	t_{gf_max}	After ON / PD goes high, if V_{GS} remains low for longer than 200 ms **(Note: this fault causes GOK to latch)**	-	200	-	ms
Maximum soft-start time	t_{SS_MAX}	After ON / PD goes high, if V_{OUT} < 90 % V_{IN} within 200 ms, or if V_{GS} remains less than 1.5 V below internal charge pump voltage (indication of fuse not fully on) within 200 ms **(Note: this fault causes GOK to latch)**	-	200	-	ms

Notes

(1) Guaranteed by design and characterization

(2) Typical limits are established by characterization and are not production tested

(3) Min. and Max. Parameters are not 100% production tested

FUNCTIONAL BLOCK DIAGRAM

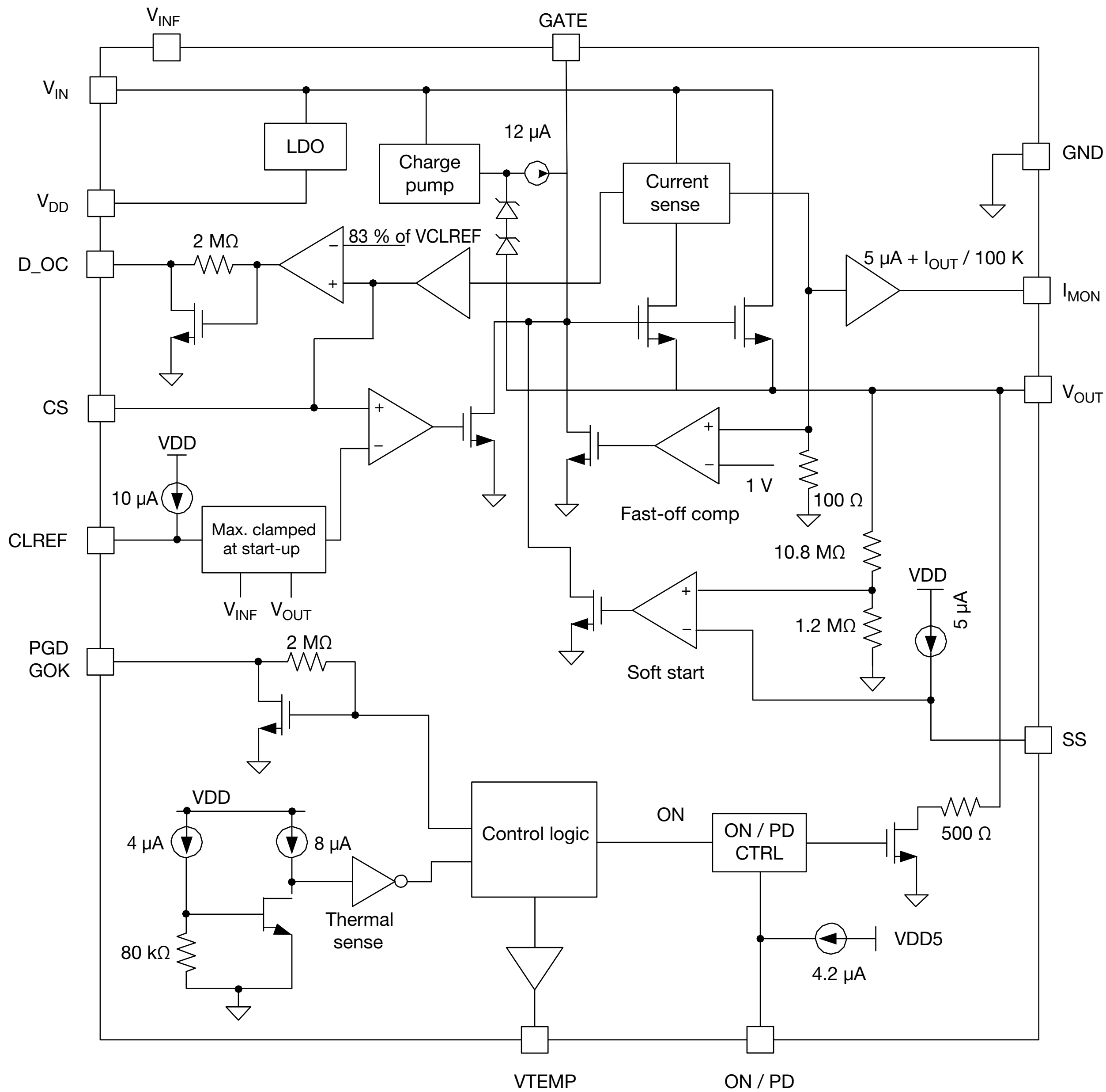


Fig. 4 - Functional Block Diagram

TYPICAL CHARACTERISTICS (Test conditions: V_{IN} = 12 V, C_{SS} = 220 nF, RCS = 2 kΩ, RCLREF = 120 kΩ, RCS = 2 kΩ, RIMON = 2 kΩ, T_A = 25 °C, unless otherwise specified)

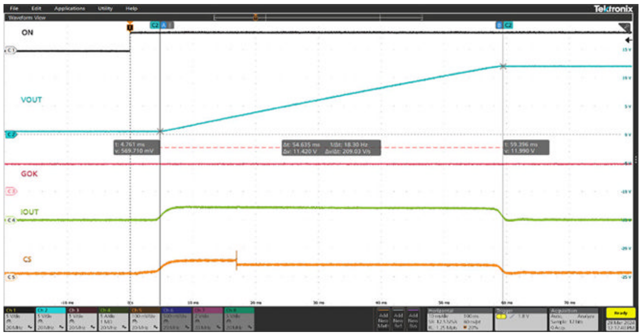


Fig. 5 - Start Up by EN (I_{OUT} = 0 A, C_{OUT} = 10mF)

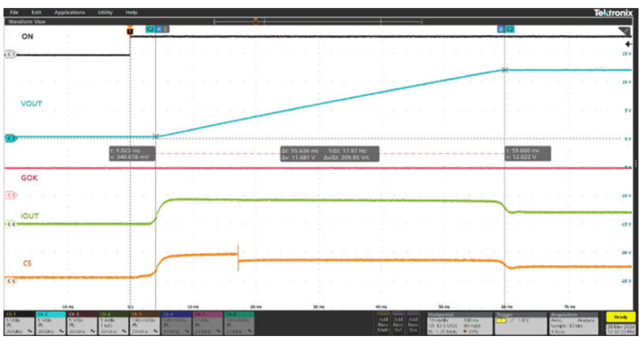


Fig. 6 - Start Up by EN (I_{OUT} = 2 A, C_{OUT} = 10mF)

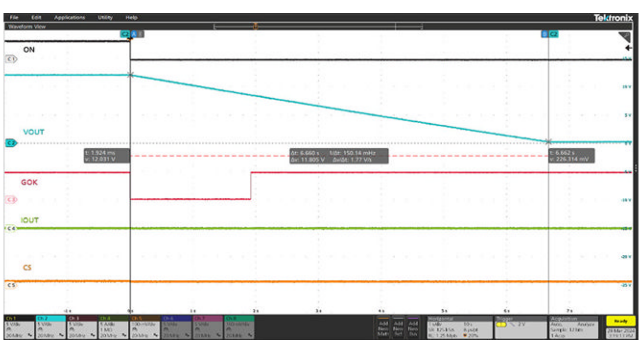


Fig. 7 - Shut Down by EN (I_{OUT} = 0 A, C_{OUT} = 10 mF)

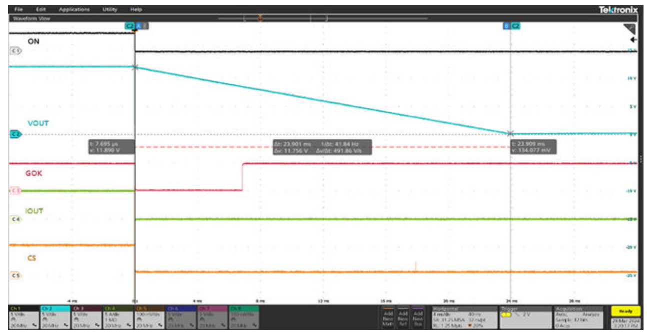


Fig. 8 - Shut Down by EN (I_{OUT} = 2 A, C_{OUT} = 10 mF)

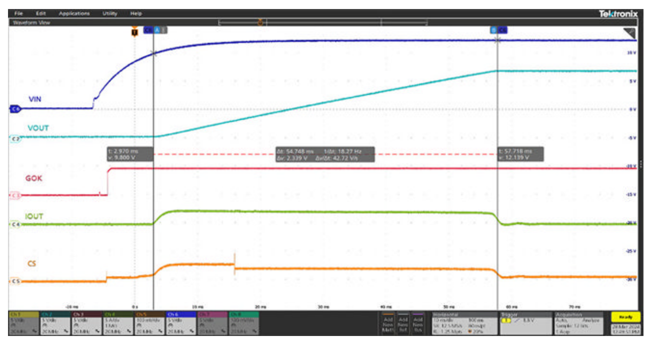


Fig. 9 - Start Up by V_{IN} (I_{OUT} = 0 A, C_{OUT} = 10 mF)

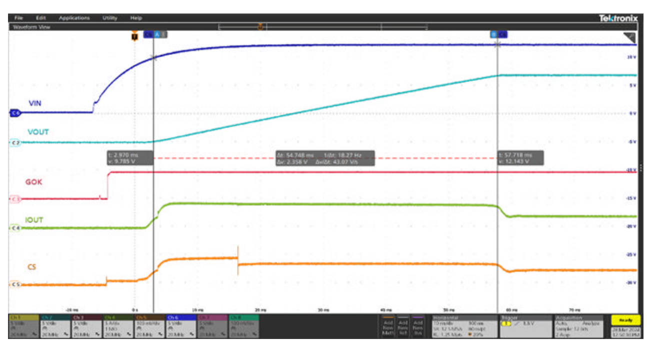


Fig. 10 - Start Up by V_{IN} (I_{OUT} = 2 A, C_{OUT} = 10 mF)

TYPICAL CHARACTERISTICS (Test conditions: V_{IN} = 12 V, C_{SS} = 220 nF, RCS = 2 kΩ, RCLREF = 120 kΩ, RCS = 2 kΩ, RIMON = 2 kΩ, T_A = 25 °C, unless otherwise specified)

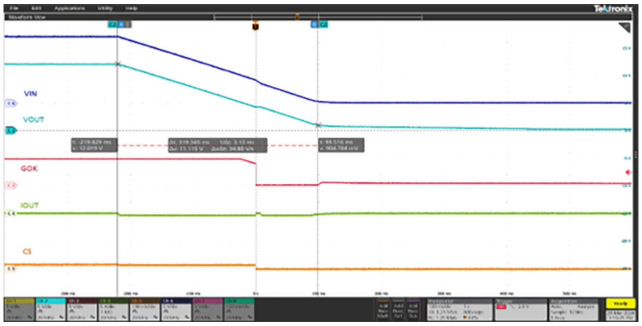


Fig. 11 - Shut Down by V_{IN} (I_{OUT} = 0 A)

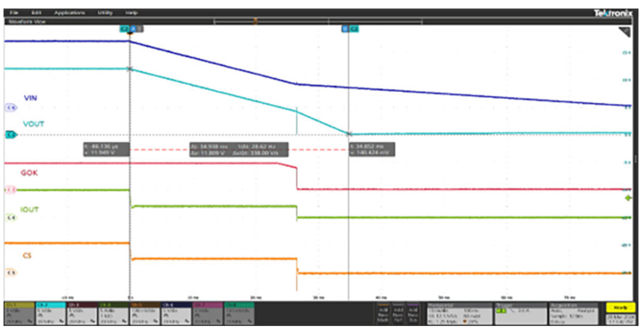


Fig. 12 - Shut Down by V_{IN} (I_{OUT} = 5 A)

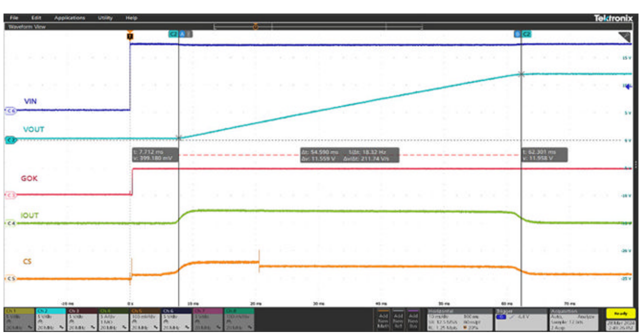


Fig. 13 - Start Up by Hot Plug V_{IN} (I_{OUT} = 0 A, C_{OUT} = 10 mF)

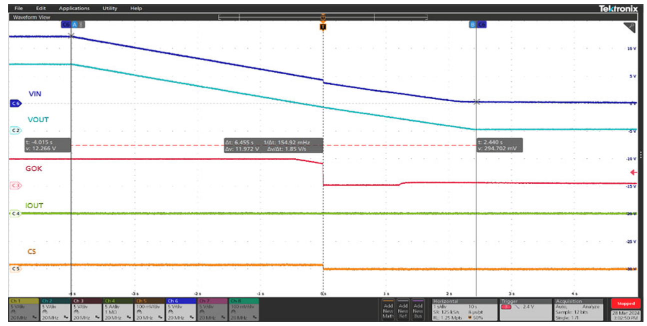


Fig. 14 - Shut Down by V_{IN} (I_{OUT} = 0 A)

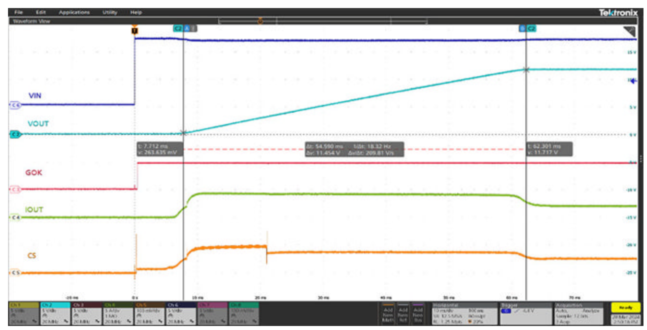


Fig. 15 - Start Up by Hot Plug V_{IN} (I_{OUT} = 2 A)

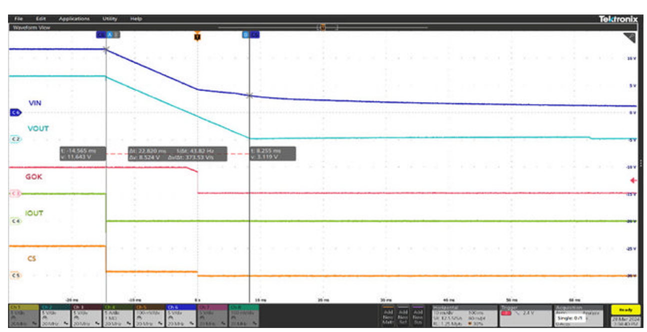


Fig. 16 - Shut Down by V_{IN} (I_{OUT} = 5 A)

TYPICAL CHARACTERISTICS (Test conditions: V_{IN} = 12 V, C_{SS} = 220 nF, RCS = 2 kΩ, RCLREF = 120 kΩ, RCS = 2 kΩ, RIMON = 2 kΩ, T_A = 25 °C, unless otherwise specified)

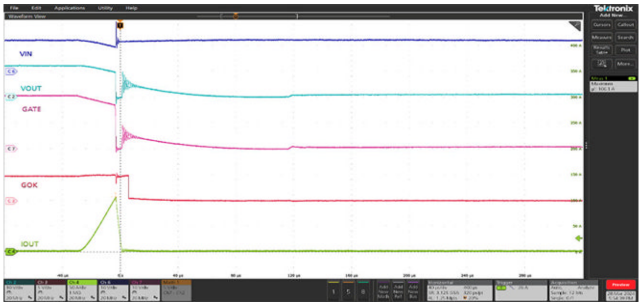


Fig. 17 - V_{OUT} Short Circuit During Normal Operation (I_{OUT} Measured Before C_{OUT})

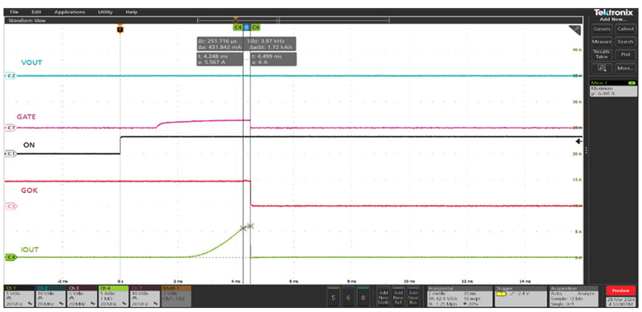


Fig. 18 - Start Up by EN with V_{OUT} Short (I_{OUT} Measured Before C_{OUT})

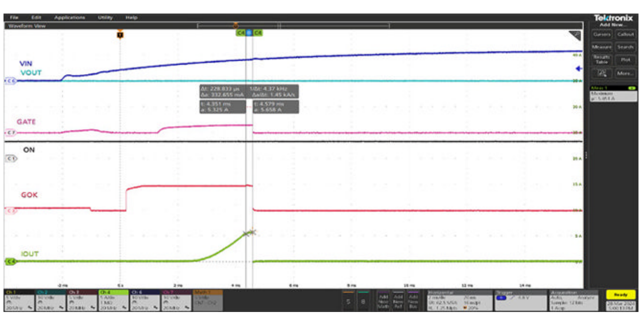


Fig. 19 - Start Up by V_{IN} with V_{OUT} Short (I_{OUT} measured before C_{OUT})

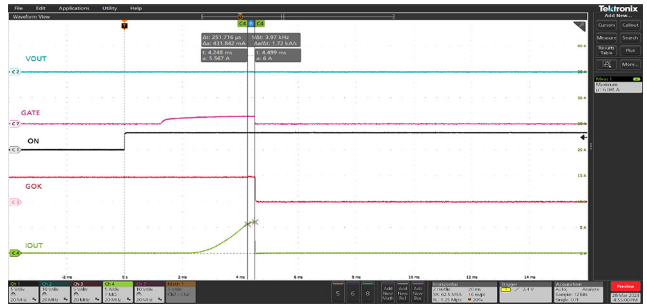


Fig. 20 - Start Up by Hot Plug V_{IN} with V_{OUT} Short (I_{OUT} Measured Before C_{OUT})

Fig. 21 - D_OC Assertion for Over Current During Normal Operation (I_{LIM} = 60 A)

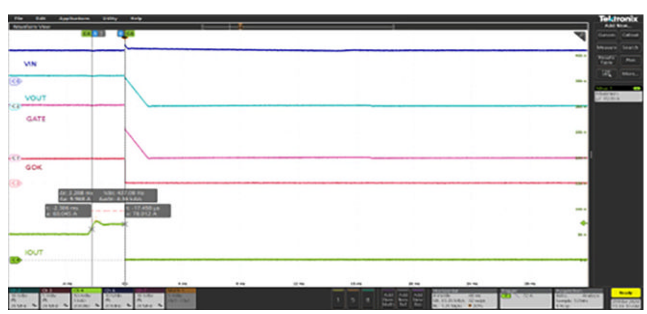


Fig. 22 - D_OC Desertion from Over Current During Normal Operation (I_{LIM} = 60 A)

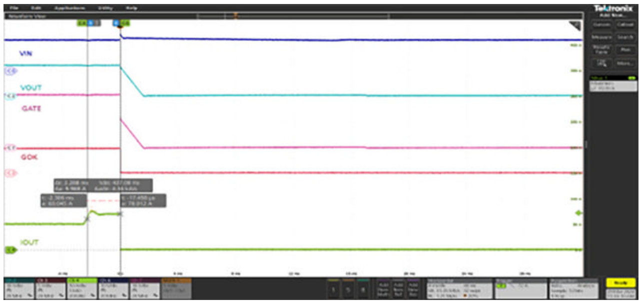


Fig. 23 - Over Current Protection Switch Off after 2.3 ms Blanking During Normal Operation

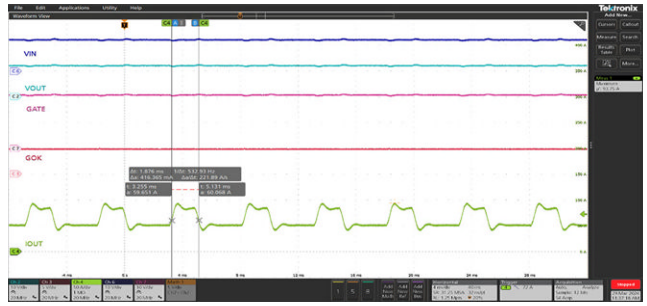


Fig. 24 - 2.3 ms Over Current Blanking During Normal Operation

DETAILED OPERATIONAL DESCRIPTION

The SiC32311 integrates at 60 A high-side MOSFET with $R_{DS(on)}$ of 0.6 mΩ, which is suited for multi-fuse hot-swap applications. The parts can work as stand-alone devices or be controlled by a hot-swap controller for multi-fuse operation.

The SiC32311 limits the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop. It provides an integrated solution for monitoring the output current and the die temperature, eliminating the need for an external current-sensing power resistor, power MOSFET, and thermal sensing device. Also, it provides monitored current and temperature information feedback to the processor or controller. The SiC32311 limits the internal MOSFET current by controlling the gate voltage through the current limit reference input and soft start ramp.

Power-Up Sequence

For hot-swap applications, the input of the SiC32311 can experience a voltage spike or transient during the hot-plug procedure. This is caused by the parasitic inductance of the input trace and the input capacitor. A fixed 1 ms insertion delay stabilizes the input voltage.

If the SiC32311 is controlled by a front-end hot- swap controller, there will be a time-on delay before ON / PD can turn on the power FET. This stabilizes the input voltage when GOK becomes high.

As shown in Fig. 25, the input voltage rises immediately. The power FET GATE voltage should always be pulled low during the V_{IN} plug-in with high dV/dt. The internal LDO output V_{DD} ramps up along with the input voltage. If the SiC32311 co-operates with the hot-swap controller, the V_{DD} output can be used to power up the hot-swap controller.

The power FET remains off until the ON / PD signal is pulled high. When the ON / PD signal becomes high and the 1 ms insertion delay time ends, the power FET is charged up by the internal 12 µA charge pump under the supervision of the soft-start control loop and the CLREF current limiting loop, which itself is a function of the V_{OUT}/V_{IN} voltage ratio, or alternately, the DAC output of a controller.

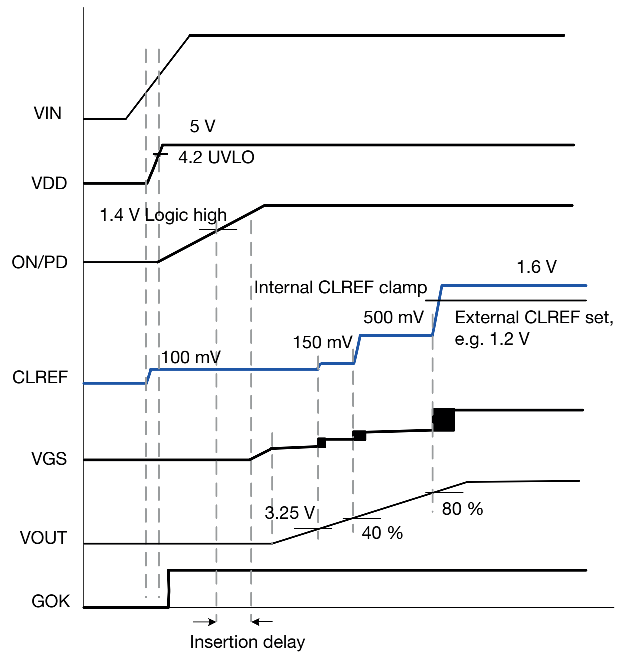


Fig. 25 - Start-Up Sequences Between SiC32311 and Front-End Controller

If the SiC32311 works as stand-alone devices (see Fig. 26), an external capacitor C_{ON} can be connected from ON / PD to ground for an automatic start-up. The internal 4.2 µA current source charges the capacitor when V_{DD} is higher than UVLO. Also, ON / PD can be pulled up externally to the V_{DD} voltage. An internal 10 µA CLREF current source determines the current limit level through a resistor to ground.

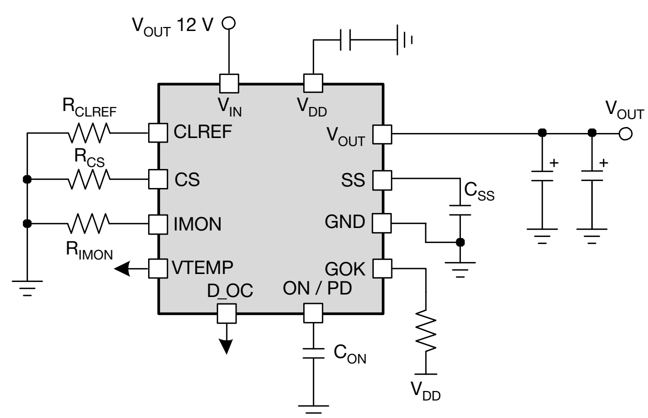


Fig. 26 - Standalone Operating Schematic

Current Limit at Start-Up

The SiC32311 load current is limited by the CLREF input. The CS voltage is compared with the CLREF voltage through an OTA amplifier to regulate the power FET gate. This prevents the switch current from exceeding the CLREF defined current limit. The CLREF voltage is set and internally clamped lower during start-up to allow a controlled, gradual ramping up of V_{OUT} voltage. Once V_{OUT} is ramped close to V_{IN}, the CLREF can be raised to the full current limit, the power FET gate is fully enhanced, and the system is ready to draw power from the input.

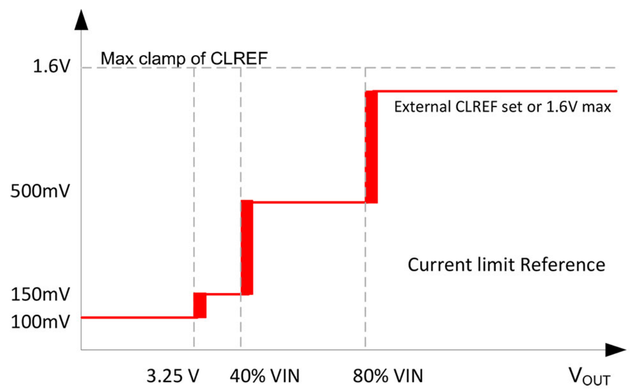


Fig. 27 - CLREF Maximum Clamp at Different V_{OUT} Levels

As shown in Fig. 27, in order to protect the device from overheating during start-up, a maximum power limit is included during start-up. The CLREF voltage has an internal maximum clamp that depends on V_{IN} and V_{OUT}. When V_{OUT} is less 3.25 V, CLREF is clamped at 100 mV. When V_{OUT} is between 3.25 V and 40 % of V_{IN}, CLREF is clamped at 150 mV. When V_{OUT} is between 40 % and 80 % of V_{IN}, CLREF is clamped at 500 mV. When V_{OUT} is > 80 % V_{IN}, CLREF is clamped to 1.6 V.

The desired start-up current limit is a function of the CS resistor RCS. The CLREF voltage is calculated with equation (1):

$$I_{LIMIT\_SS} = \frac{V_{CLREF\_SS}}{CSgain \times R_{CS}}$$

Where V_{CLREF_SS} is the CLREF voltage at start-up. Then the V_{OUT} power-up ramp time can be approximately estimated with equation (2):

$$t_{RAMP} = \frac{V_{IN}}{I_{LOAD}} \times C_{OUT}$$

The V_{OUT} ramp time varies with the load condition and the output capacitor (C_{OUT}) while adopting the CLREF current limit during start-up. For example, for V_{CLREF_SS} = 100 mV, RCS = 2 kΩ. The desired soft-start current limit is 5 A, that is, the maximum FET start-up current is limited to around 5 A. If C_{OUT} = 8500 μF, V_{IN} = 12 V, and the V_{OUT} ramp time is about 20.4 ms without an output load.

A capacitor connected to SS determines the soft-start time. When ON / PD is pulled high, a constant-current source ramps up the voltage on SS. The output voltage rises at aproximately ten times the SS slew rate. The SS capacitor can be set larger to increase the soft-start time. Load sharing during SS.

During start-up, if the CS voltage exceeds CLREF, the power FET gate-to-source voltage is regulated to hold the FET current constant. If the power FET remains on while the V_{OUT} remains lower than 90 % V_{IN} within the 200 ms maximum soft-start time, the power FET is shut down when the 200 ms time ends (see Fig. 28).

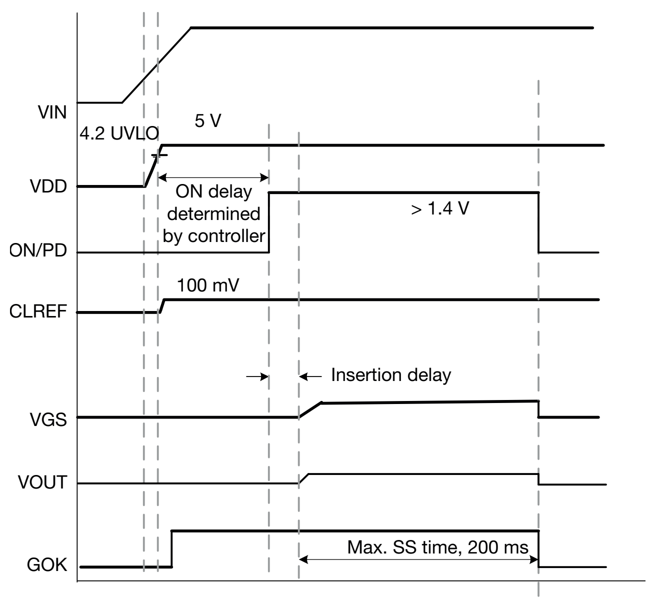


Fig. 28 - Start-Up at Fault

Normal Operation

When the output voltage has ramped up close to V_{IN} and it remains higher than 80 % V_{IN}, the CLREF voltage will be allowed to operate at full value (not to exceed 1.6 V). Once V_{OUT} has completed ramping, the charge pump will drive V_{GS} of the power FET to a fully enhanced phase. Fault supervision circuits will continue to monitor the need for corrective action.

Current Limit at Normal Operation

During normal operation, if the CS voltage exceeds V_{OC_TH}, which is typically 83 % of the CLREF voltage, the D_OC flag will activate. If the CS voltage exceeds CLREF voltage for more than 2.3 ms, the switch will be turned off, and the GOK flag will latch. During this 2.3 ms window, the V_{GS} of the power FET remains fully enhanced unless short circuit or over-temperature fault is detected. No current limiting occurs during this 2.3 ms interval. If the GOK pin latches, the power supply or ON / PD of SiC32311 will require cycling to clear the latch.

The desired OCP threshold at normal operation is a function of the CS resistor (R_{CS}). The threshold should be higher than the normal maximum load current, allowing the tolerances in the current sense value. The current limit can be set using equation (5):

$$I_{LIMIT} = \frac{V_{CLREF}}{CSgain \times R_{CS}}$$

Where V_{CLREF} is the voltage of CLREF in normal operation.

CSgain is 10 μA/A. For example, for V_{CLREF} = 1.2 V, R_{CS} = 2 kΩ; the desired current limit is 59.5 A at normal operation.

Short-Circuit Protection

Regardless of the programmed value of CLREF, if a current greater than 100 A is observed, the power FET V_{GS} is forced to 0 V rapidly (typically within 200 ns) and the GOK fault will be latched.

ON / PD Control

ON / PD is used to control both the on/off of the internal power FET and the pull-down mode of the output voltage. When ON / PD is used for power FET on / off control, the FET is turned on if the ON / PD voltage is higher than 1.4 V. If the ON / PD voltage is lower than 1.2 V, the FET is turned off. If ON / PD is used for V_{OUT} pull-down mode, the ON / PD voltage should be driven to aproximately 1.1 V for more than 80 μs. The device recognizes 0.8 V < ON / PD < 1.2 V as a special state that requires pulling down V_{OUT}.

The ON / PD has a fixed 1 ms insertion delay after V_{DD} and V_{IN} have passed the UVLO threshold. All fault functionality is operative during the insertion delay, so that the GOK signal is pulled high if no fault is detected or remains low if a fault is detected. If a non-latching fault self-clears, then a 1 ms timer will begin once the ON_PD pin is above 1.4 V. When V_{IN} is below the UVLO threshold an internal 1 MΩ pull down resistor will attempt to discharge the ON_PD pin.

Once V_{IN} UVLO is cleared, the pull down resistor is disabled and the 4.2 μA charge current is enabled.

Once the ON / PD voltage is pulled higher than 1.4 V, and the 1 ms insertion delay ends, the internal charge pump charges the power FET's GATE. Once the GATE voltage reaches its threshold (V_{GSTH}), the power FET turns on (Fig. 29). The output voltage rises following the soft-start control loop retarding the Gate voltage until V_{OUT} is sufficiently charged. This limits the power FET in-rush current.

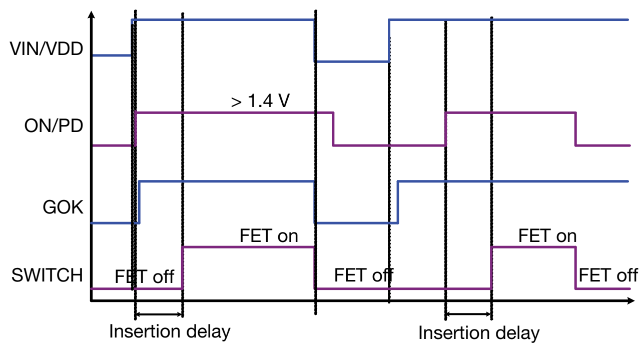


Fig. 29 - Power FET On / Off Control by ON / PD When no Fault Occurs

If the SiC32311 works in stand-alone mode, a capacitor on ON / PD can be used for automatic start-up by the internal 4.2 μA pull-up current source. Once the ON / PD voltage reaches its turn-on threshold, the power FET Gate is charged by the internal charge pump.

When the ON / PD voltage is set to around 1.1 V for more than 80 μs, devices enter in pull-down mode (see Fig. 9). In pull-down mode, an integrated 625 Ω pull-down resistor discharges the output after a fixed delay time (2 ms). If the ON / PD signal is pulled low directly, the pull-down mode is disabled, and the switch output voltage discharges through the external load.

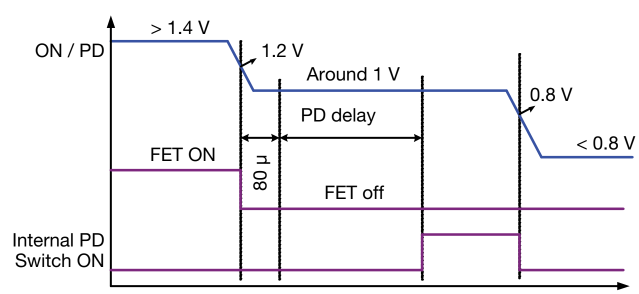


Fig. 30 - PD Mode Control by ON / PD

The connection of ON / PD shown in Fig. 31. controls ON / PD through a resistor divider from the controller. For example, choose R_{ON} =100 kΩ. If ON / PD is only used for the power FET on / off control, the resistor R_{PD} can be set to 0 Ω. Pull-down mode can be set by selecting a 22 kΩ R_{PD} resistor. ON / PD is set to around 1 V by the external resistor divider and the ON / PD internal 4.2 μA current source.

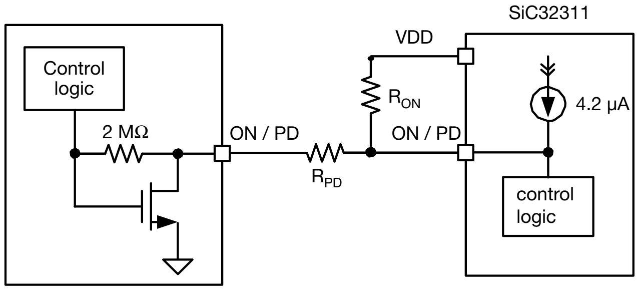


Fig. 31 - ON / PD Connection

GOK Report

GOK is an open-drain, active-low signal which reports the eFuse status. When a fault occurs, GOK is pulled low.

Pull up GOK to the V_{DD} voltage through a 100 kΩ resistor. During the V_{DD} power-up, the GOK output is driven low. Before the power FET is turned on, the GOK fault stats is checked during the ON / PD 1 ms insertion delay. All fault functionality is operative during the insertion delay time, therefore GOK is pulled high if no fault is detected or is pulled low if a fault is detected.

GOK monitors the following fault events:

1. Over-current protection: when the CS voltage exceeds the CLREF threshold during normal operation, the GOK signal is pulled low and latches after a 2.3 ms moderate over-current blanking time
2. Short-circuit protection: when the load current reaches 100 A, short circuit current threshold rapidly, GOK is pulled low immediately and latches
3. The integrated power FET D-S, G-D, and G-S short detection: detailed performance characteristics can be reviewed in the “Damaged Integrated Power FET Detection” section. Although these faults cause GOK to pull low immediately, the GOK pin does not latch unless the 200 ms soft start timer expires.
4. Over-temperature protection at junction temperature TJ > 142 °C: once a fault is detected GOK is pulled low and latches. Over-temperature protection hysteresis is 20 °C.

The release of the GOK fault latch can be accomplished by recycling V_{IN} or by toggling ON / PD.

Fig. 32 shows the FET on / off control with the GOK timing diagram.

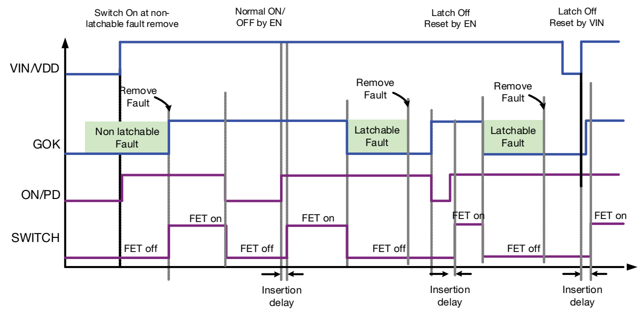


Fig. 32 - FET On / Off Control With GOK Timing Diagram

Damaged Integrated Power FET Detection

Damaged integrated power FET detection includes FET drain-source shorts, gate-drain shorts, and gate-source shorts.

1. D-S short detection during start-up

Once the V_{DD} is higher than the UVLO rising threshold, the controller detects a shorted pass FET during power-up by treating an output voltage that exceeds 70 % x V_{IN} during power up as a short on the MOSFET. The GOK signal remains low when the controller detects V_{OUT} > 70 % x V_{IN} during start up. Once the short is removed and the controller detects V_{OUT} < 70 % x V_{IN}, the GOK signal is released to high again, and the hot-swap controller prepares for normal start-up.

2. G-D short detection during start-up

The G-D short is detected by monitoring the G-S voltage. During power-up, the controller detects the power FET G-D short by the condition of power FET drain-to-gate voltage (V_{GS} > 2 V). The GOK signal remains low until the short is removed, and the controller detects V_{GS} < 2 V.

3. G-S, G-D short detection during normal operation

When the part operates normally and V_{OUT} remains higher than 90 % of V_{IN}, the controller determines the power FET G-S or G-D short by the V_{CP} - V_{GATE} voltage, where VCP is the internal charge pump voltage. The fault latch can be cleared by recycling V_{IN} or by toggling ON / PD.

The power FET short faults are listed in Table 1

TABLE 1 - THE POWER FET SHORT FAULTS

FET FAULT		DETECTION CONDITION	GOK FLAG
Start-up FET short	D - S	V_{OUT} > 70 % x V_{IN}	Keep low until V_{OUT} < 70 % x V_{IN}
	G - D	V_{GS} > 2 V	Keep low until V_{GS} < 2 V
Normal operation FET short	G - D / G - S	(V_{CP} - V_{GATE}) > 2 V after 200 ms	Pull low

D_OC Report

D_OC is an open-drain, active-low output to report the over-current fault. When the voltage on CS is higher than V_{OC_TH}, typically 83 % of CLREF, the D_OC is driven low. Pull up D_OC to the VDD voltage through a 100 k Ω resistor.

Input and Output Transient Protection

The hot-swap system experiences positive transients on the input during a hot plug or rapid turn-off with high current due to parasitic inductance in the input circuit.

For input transient protection, a TVS diode (transient voltage suppressor, a type of Zener diode) may be required on the input to limit transient voltages below the absolute maximum ratings.

The output may experience negative transients during rapid turn-off with high current due to inductance in the output circuit. The lowest voltage allowed on the device output is -0.3 V_{DC} and -1 V for 500 μs transient pulse. If a transient makes OUT more negative, the internal ESD Zener diode attached to the pin will become forward biased, and the current will be conducted across the substrate to the ground. The internal ESD diode may not be strong enough to sustain a large current, and the current may disrupt normal operation or, if large enough, damage the part.

An output voltage clamp diode may be required on the output to limit negative transients. Select a Schottky diode with a low forward voltage at the anticipated current during an output short. By doing this, the negative voltage spike at the output terminal can be clamped at less than -0.7 V, thus the IC is protected during a short output.

Current Sense (CS Output)

CS provides a current proportional to the output current (the current through the power device). The gain of the current sense is 10 μA/A.

There is a resistor (R_{CS}) connected from CS to form an external voltage. Use equation (6) and equation (7) to determine a proper reference voltage:

$I_{CS} = I_{OUT} \times 10\ \mu A/A + 5\ \mu A$ (6)

$V_{CS} = I_{CS} \times R_{CS}$ (7)

Once the CS voltage reaches the CLREF current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant.

Current Monitor (I_{MON} Output)

The gain of the current monitor is 10 μA/A. There is a resistor (R_{IMON}), connected from I_{MON} to ground. The I_{MON} voltage range of 0 V to 1.6 V is required to keep I_{MON}'s output current linearly proportional to the output current use equation (8) and equation (9) to determine a proper reference voltage:

$I_{MON} = I_{OUT} \times 10\ \mu A/A + 5 \mu A$ (8)

$V_{IMON} = I_{MON} \times R_{IMON}$ (9)

The current monitor output can be used by the controller to accurately monitor the output current. Place a 100 nF capacitor from I_{MON} to GND to smooth the indicator voltage.

Generally, connect a 2 kΩ resistor (R_{IMON}) to ground to set the gain of the output, which is about 20 mV per ampere. For best accuracy, use resistors within 1 percent.

Temperature Sense Output, V_{TEMP}

V_{TEMP} reports the junction temperature. It is a voltage output proportional to the junction temperature. The V_{TEMP} output voltage is 10 mV/°C with a 200 mV offset. See equation (10):

$V_{TEMP} = T_{JUNCTION} \times 10\ mV/°C + 200\ mV$ (10)

For example, if the junction temperature is 100 °C, the V_{TEMP} voltage is 1.2 V. If V_{TEMP} = 0 V, the junction temperature is about -20 °C. The total temperature sense range is -20 °C to +140 °C. When the junction temperature is below -20 °C, V_{TEMP} remains at 0 V.

In multi-fuse operation, V_{TEMP} pins of every paralleled fuse can be connected to the temperature monitor pin of the controller (see Fig. 33). When TMON pins are paralleled the highest temperature of all units will be reported.

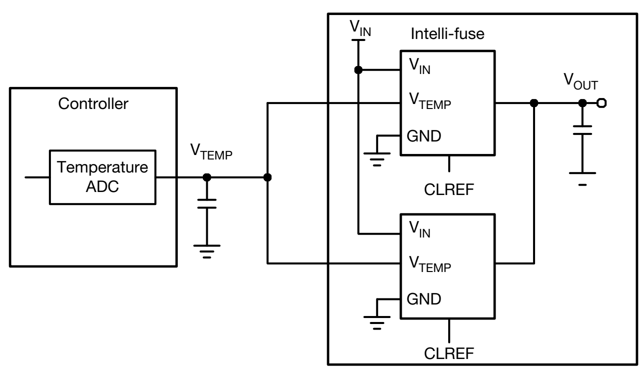


Fig. 33 - Multi-Fuse Temperature Sense Utilization

Thermal Protection

The device temperature is sensed by monitoring the junction temperature of the IC. The temperature information can be read from V_{TEMP}.

The device itself has thermal protection. When the junction temperature exceeds the threshold (142 °C), the power FET is turned off, and GOK is pulled low.

UVLO Protection

The device has a under-voltage lockout protection feature on V_{DD} exceeds the UVLO threshold. The devices can start up only when V_{DD} exceeds the UVLO threshold. The UVLO protection is non-latching fault.

APPLICATION SCHEMATICS

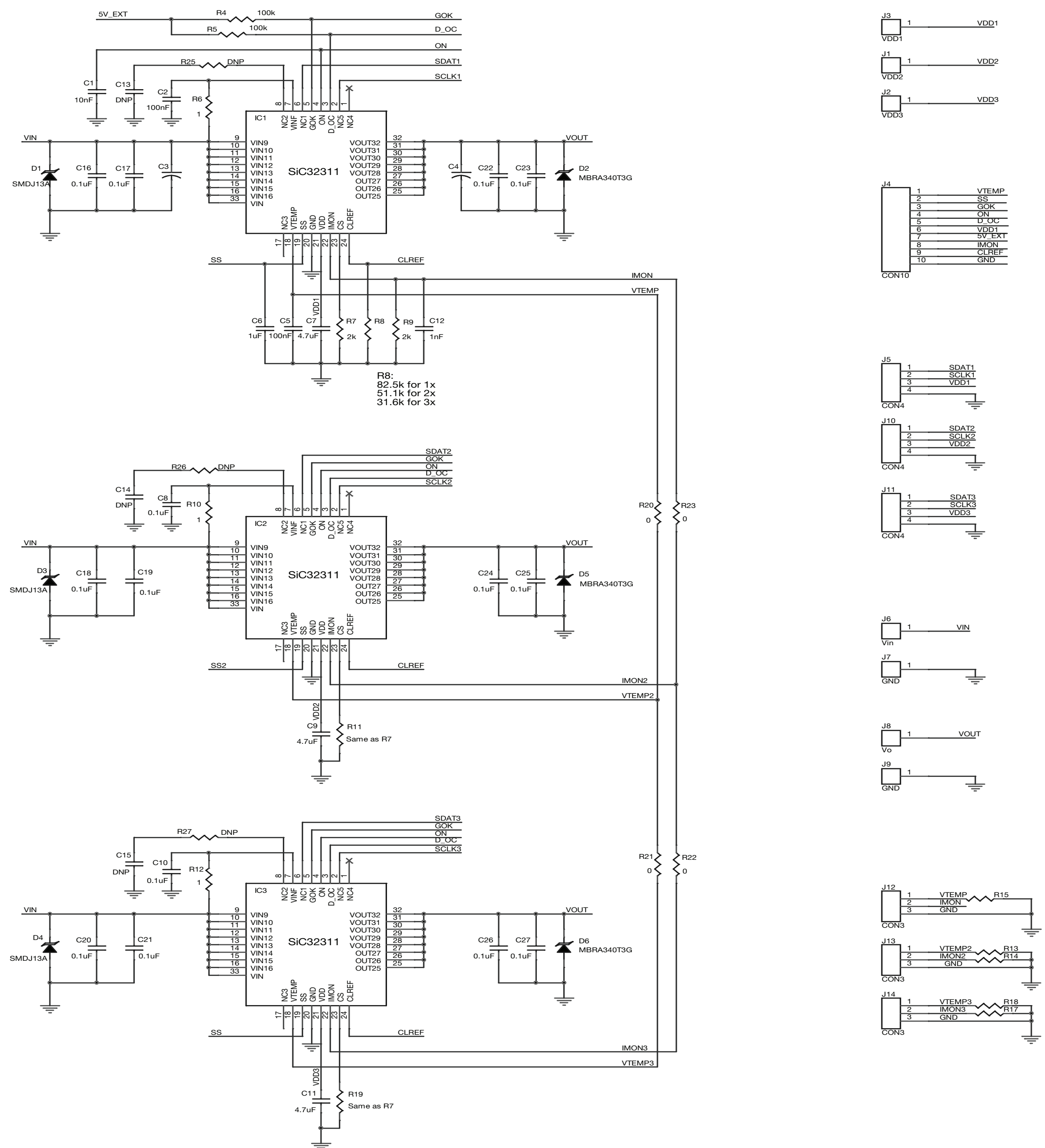


Fig. 34 - SiC32311, Parallel Fuse Operation With Controller

The ON pin can interface with micro-processor for on / off and discharge control. Toggling the ON pin will reset the fuse latch. The ON / PD can also be connected to a voltage divider from V_{IN} to set circuit UVLO level.

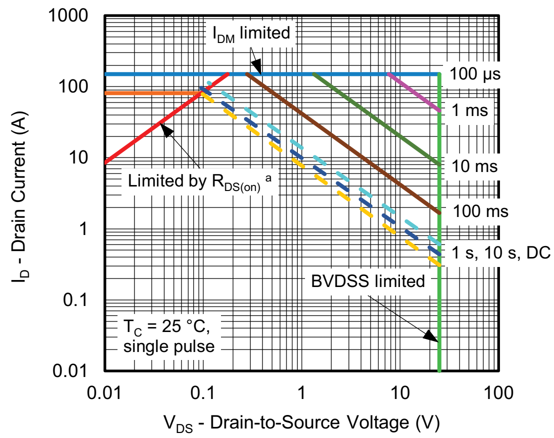


Fig. 35 - Safe Operating Area Curve

PRODUCT SUMMARY	
Part number	SiC32311
Description	0.6 mΩ, hot-swap eFuse, I_{MON}, GOK, D_OC report latch on fault
Configuration	Parallable
Slew rate time (μs)	Adjustable
On delay time (μs)	1000
Input voltage min. (V)	4.5
Input voltage max. (V)	25
On-resistance at input voltage min. (mΩ)	0.6
On-resistance at input voltage max. (mΩ)	0.6
Quiescent current at input voltage min. (μA)	2100
Quiescent current at input voltage max. (μA)	2800
Output discharge (yes / no)	Yes
Reverse blocking (yes / no)	No
Continuous current (A)	60
Package type	PowerPAK MLP32-55
Package size (W, L, H) (mm)	5 x 5 x 1
Status code	-
Product type	Hot swap, eFuse, slew rate, current report
Applications	Computers, telecom, industrial

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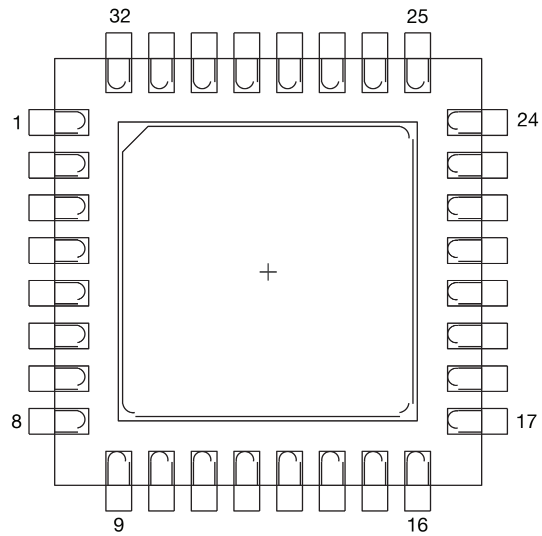
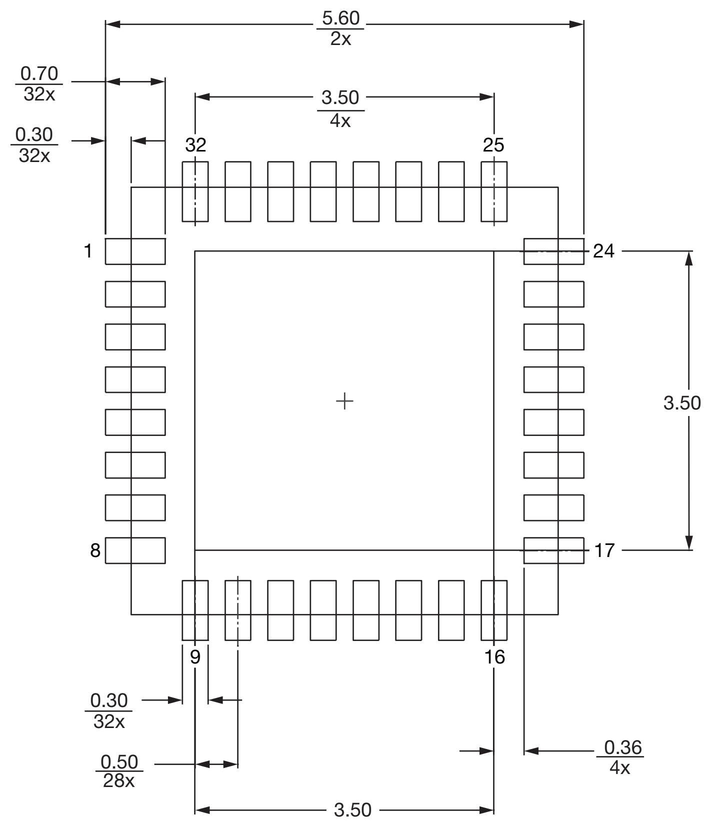
Recommended Land Pattern PowerPAK® MLP32S-55





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DWG: 3033

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