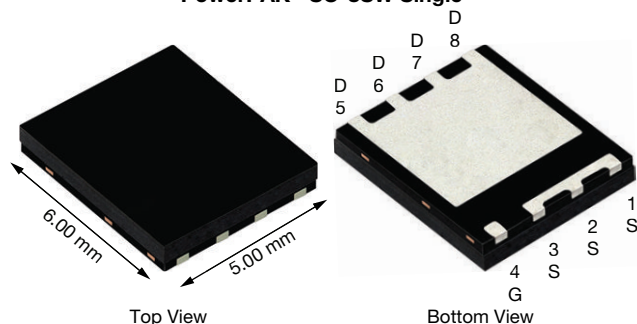


Automotive N-Channel 40 V (D-S) 175 °C MOSFET

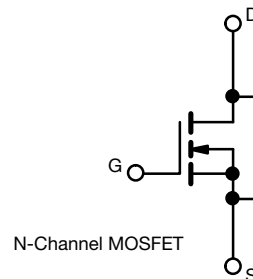
PowerPAK® SO-8SW Single


FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0008
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0011
I_D (A) ^e	372
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK® SO-8SW
Lead (Pb)-free and halogen-free	SQRS144ELP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ^e	I_D	$T_C = 25$ °C	372
		$T_C = 125$ °C	215
Continuous source current (diode conduction)	I_S	184	A
Pulsed drain current ^{a, e}	I_{DM}	1028	A
Single pulse avalanche current	I_{AS}	60	A
Single pulse avalanche energy	E_{AS}	180	mJ
Maximum power dissipation ^a	P_D	$T_C = 25$ °C	202
		$T_C = 125$ °C	67
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	42	°C/W
Junction-to-case (drain) ^d	R_{thJC}	0.74	°C/W

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per on JESD51-14
- Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

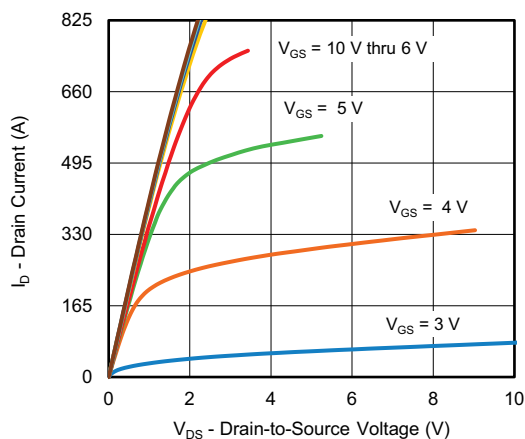
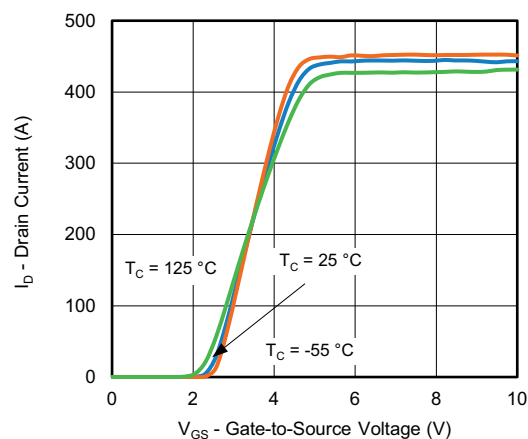
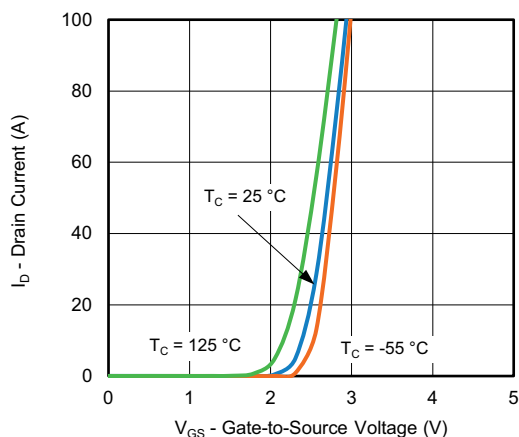
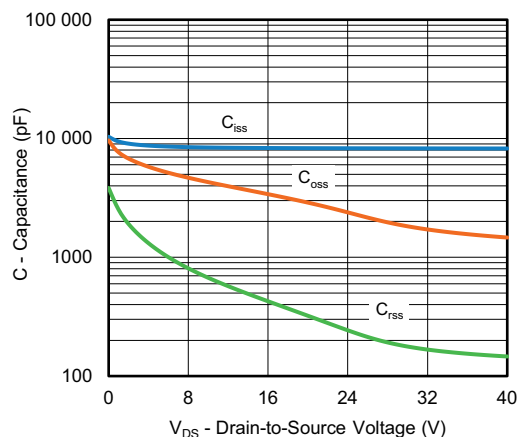
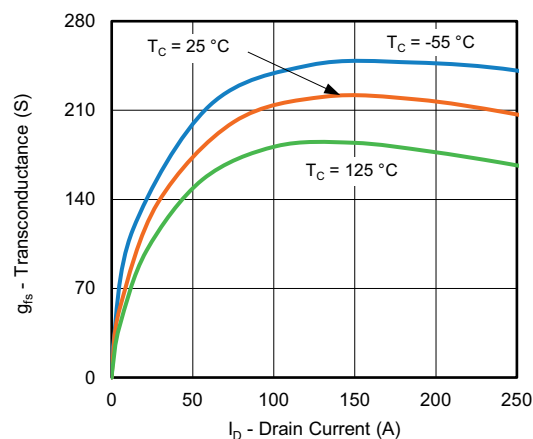
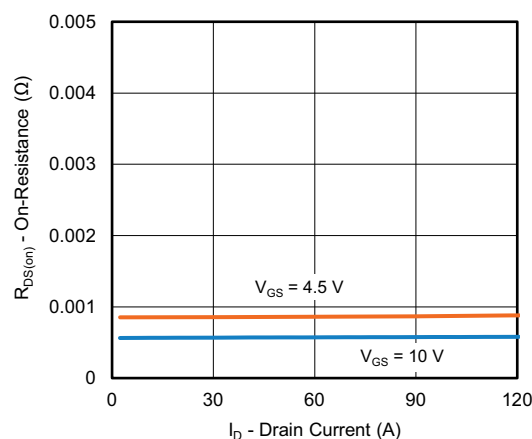


SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.2	1.7	2.2	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	250	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A	-	0.00064	0.0008	Ω
		V _{GS} = 10 V	I _D = 15 A, T _J = 125 °C	-	-	0.0012	
		V _{GS} = 10 V	I _D = 15 A, T _J = 175 °C	-	-	0.0014	
		V _{GS} = 4.5 V	I _D = 15 A	-	0.00089	0.0011	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 30 A		-	140	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	8445	11 823	pF
Output capacitance	C _{oss}			-	2184	3058	
Reverse transfer capacitance	C _{rss}			-	217	305	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 40 A	-	147	221	nC
Gate-source charge ^c	Q _{gs}			-	27	-	
Gate-drain charge ^c	Q _{gd}			-	27	-	
Gate resistance	R _g	f = 1 MHz		0.5	1.1	1.7	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 0.5 Ω I _D ≅ 40 A, V _{GEN} = 10 V, R _g = 1 Ω		-	16	24	ns
Rise time ^c	t _r			-	20	30	
Turn-off delay time ^c	t _{d(off)}			-	50	75	
Fall time ^c	t _f			-	17	26	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	736	A
Forward voltage	V _{SD}	I _F = 15 A, V _{GS} = 0 V		-	-	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs		-	67	134	ns
Body diode reverse recovery charge	Q _{rr}			-	114	229	nC
Reverse recovery fall time	t _a			-	40	-	ns
Reverse recovery rise time	t _b			-	27	-	
Body diode peak reverse recovery current	I _{RM(REC)}					-	2.9

Notes

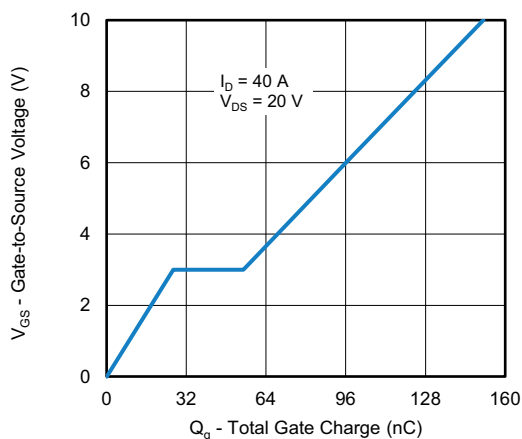
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

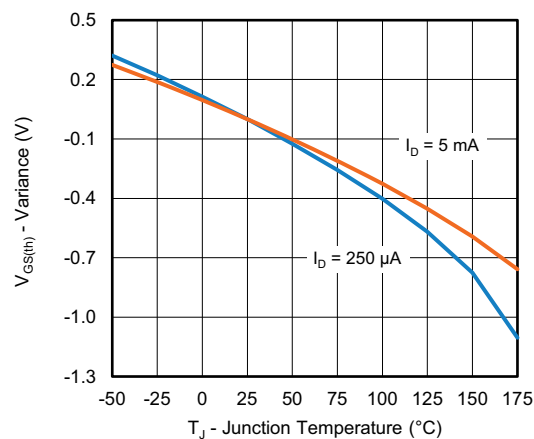
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Capacitance

Transconductance

On-Resistance vs. Drain Current



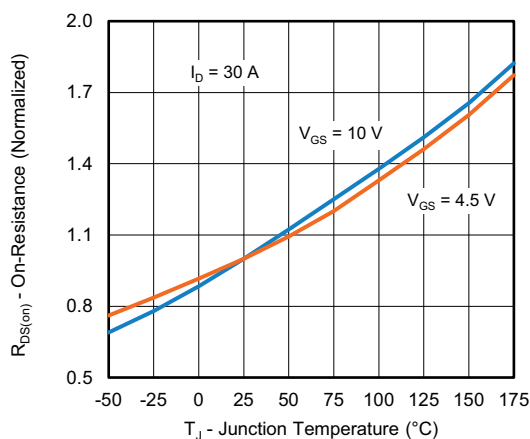
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



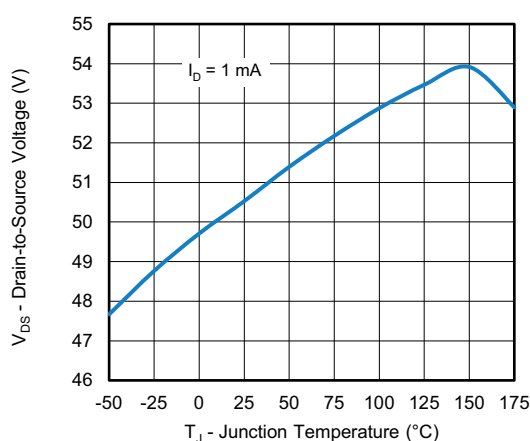
Gate Charge



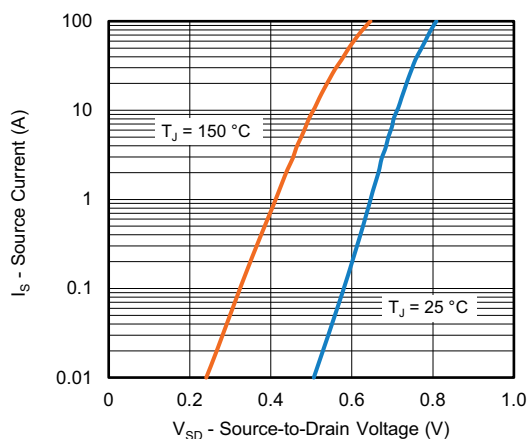
Threshold Voltage



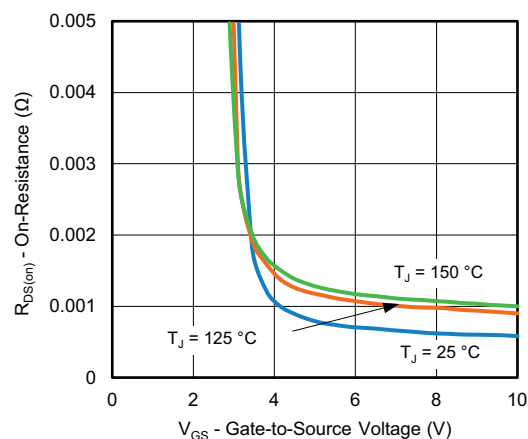
On-Resistance vs. Junction Temperature



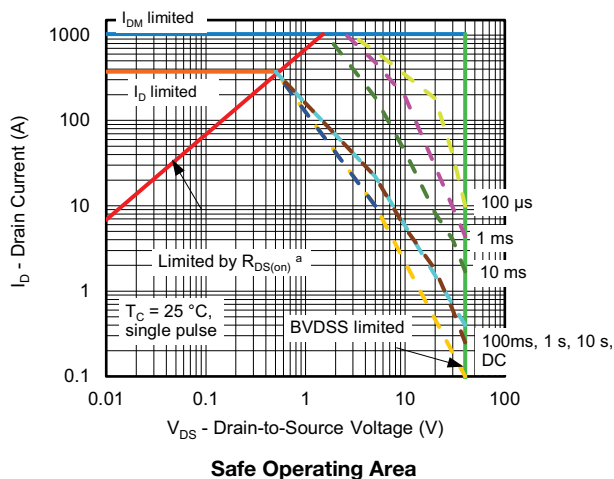
Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage



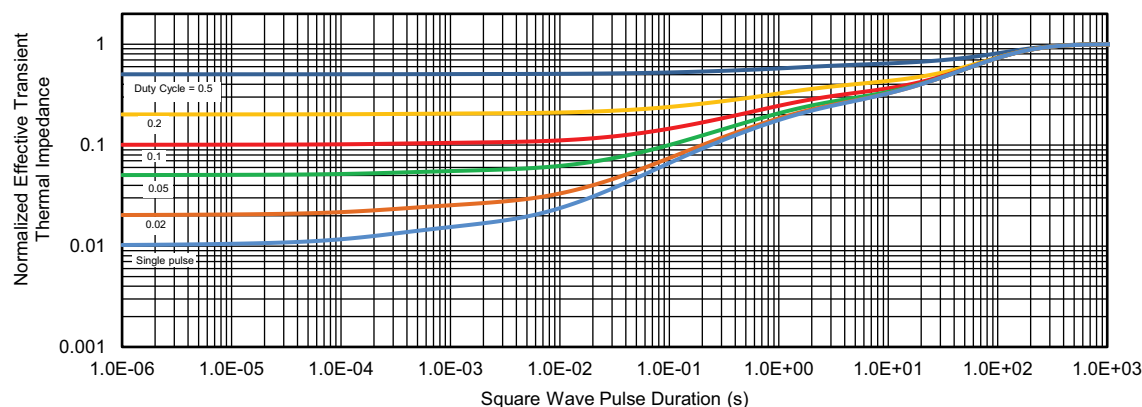
On-Resistance vs. Gate-to Source Voltage


Note

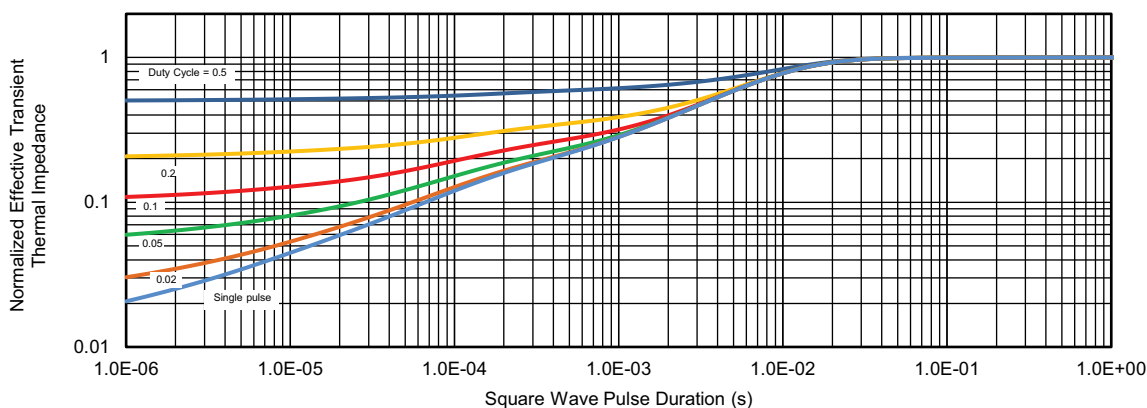
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



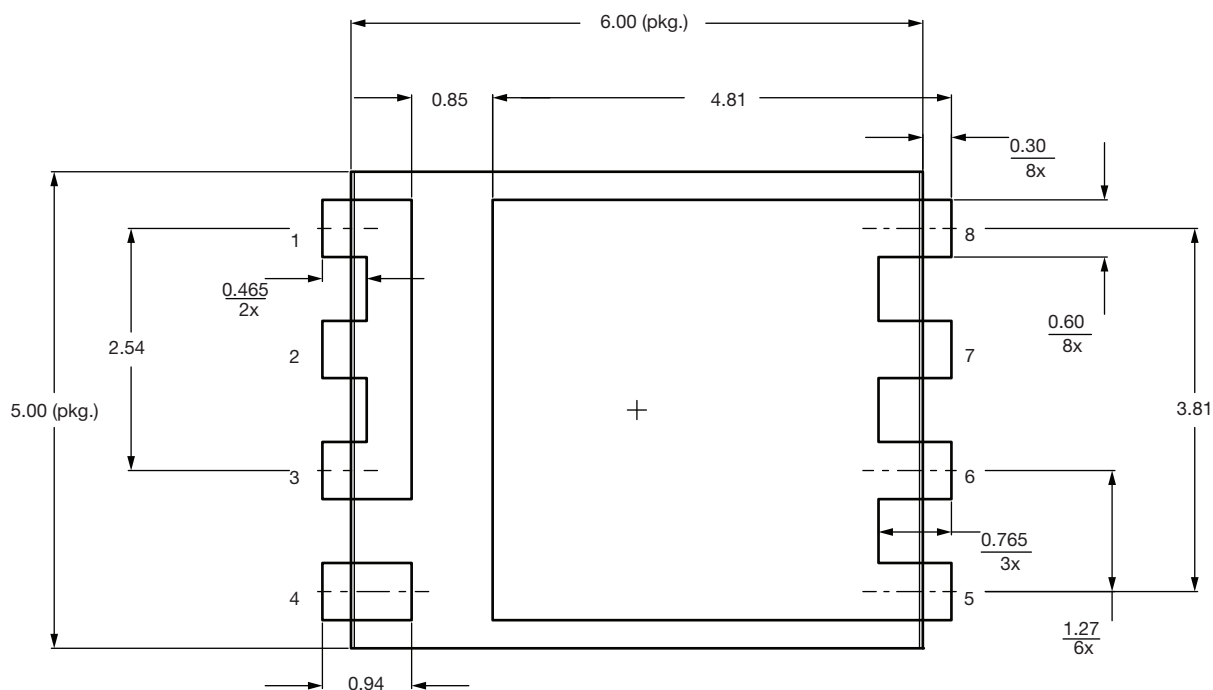
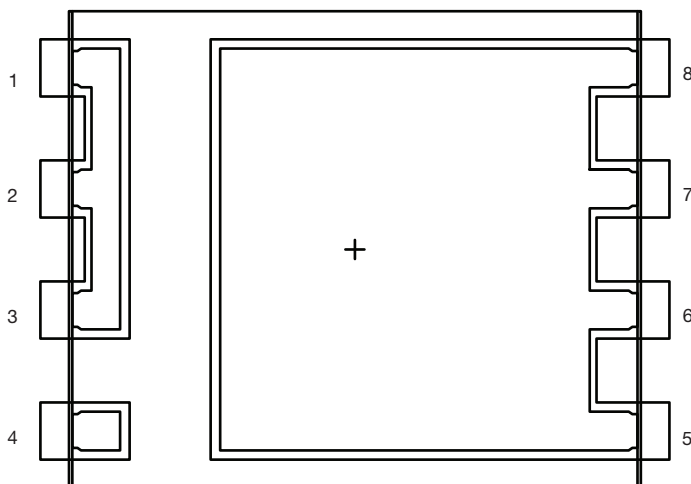
Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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Recommended Land Pattern PowerPAK® SO-8SW (PKSO8SWSCL)


Note

- Dimensions in mm

ECN: C24-0483-Rev. A, 20-May-2024
DWG: 3027



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