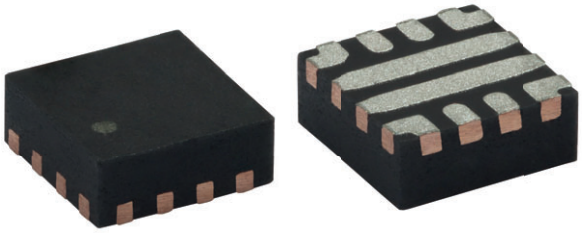
8 A, 2.7 V to 23 V, 9.2 mΩ eFuse with Transient Over Current Blanking



DESCRIPTION

The SiP32435, SiP32436, and SiP32437 are single channel eFuses in compact 2 x 2mm package.

The family integrates multiple power management, circuit control, and protection features which provide robust defense against voltage surges, excessive inrush current, short circuit, overcurrent, and load dynamic.

The family provides increase controllability and reliability with simplified design, protect both power source and the downstream circuitry connected to the switch.

FEATURES

- 2.7 V to 23 V operation voltage
- 9.2 mΩ typical switch resistance
- Overvoltage protection
  - Overvoltage clamp with pin-selectable threshold and 5 µs response time or
  - Settable overvoltage lockout with 1 µs response time
- Programmable output turn-on slew rate
- Adjustable UVLO through EN / UVLO pin
- Adjustable OVP
- ESD / HBM: > 2 kV
- ESD / CDM: > 500 V
- Status output
  - Fault indication or
  - Power Good with settable threshold (PGTH)
- Compact TDFN10 2 mm x 2 mm package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Server, computer, and add-in cards
- Networking and data storage
- Medical, healthcare, and patient monitoring devices
- Pad, table, and ebook

TYPICAL APPLICATION CIRCUIT

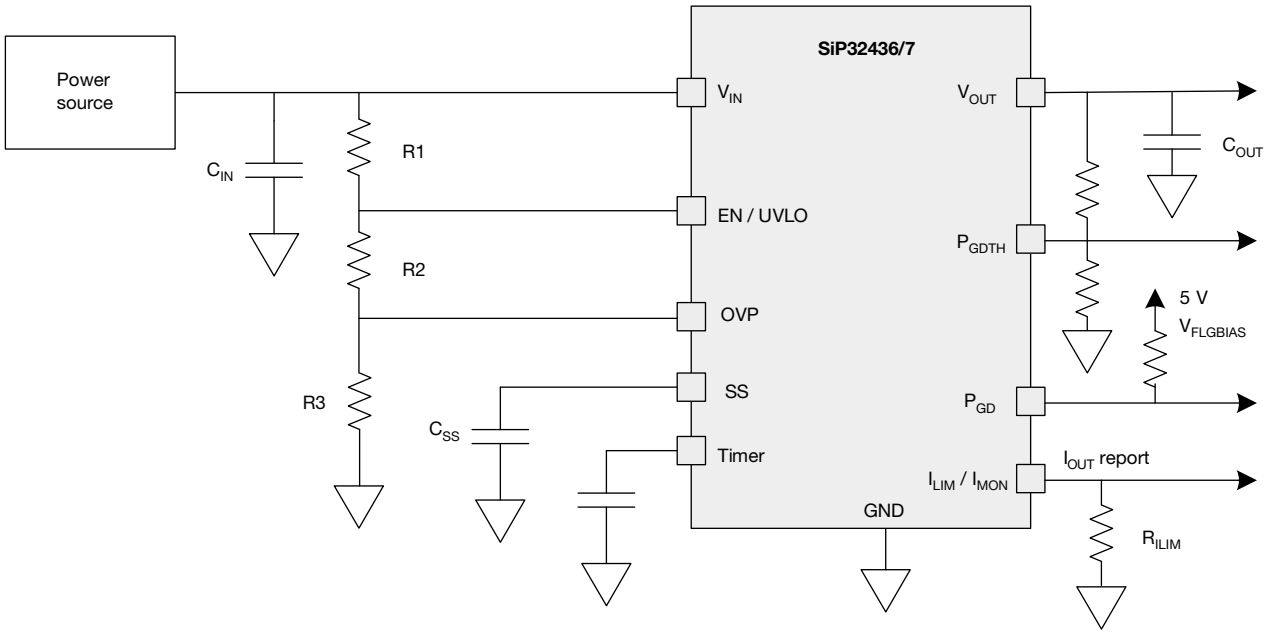


Fig. 1 - Application Circuit

PACKAGE OUTLINE

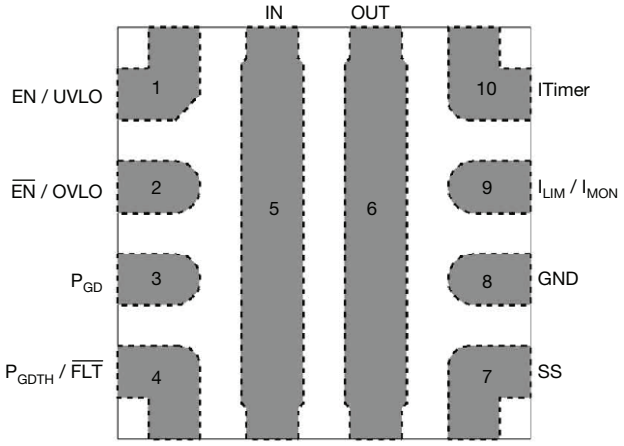


Fig. 2 - Pin Out Drawing (Top View)
Pin 1 Dot Marking is on Top of the Device

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	EN / UVLO	Active high switch control input. V_{THL}< 0.3 V, V_{THH} > 1.2 V/Typ
2	$\overline{EN}$ / OVLO (SiP32435x, SiP32437)	Input pin for setting the overvoltage switch off threshold. A resistor divider on this pin from IN to GND can be used for the setting. Connected it to GND if OVP feature isn't required. Don't leave floating
	OVCSEL (SiP32436x)	Input pin for selecting overvoltage clamp threshold. Please refer to "SiP32436x OVCSEL PIN SETTING" table for details.
3	PG (SiP32436/7)	Open drain output. It is asserted high after a de-glitch time when the switch is fully on, and PGTH input voltage exceeds thresholds of related condition. It is de-asserted if PGTH voltage falls below its threshold, or a fault is detected except over current. Assertion and de-assertion have de-glitching time
	DNC (SiP32435)	Left floating
4	PGTH (SiP32436/7)	Power good threshold feedback input pin
	/FLT (SiP32435)	An open drain output, active low fault event indicator. It is pulled low when a fault is detected
5	IN	Power switch input pins. Two pins are fused inside the package
6	OUT	Power switch output pins. Two pins are fused inside the package
7	SS	A capacitor from this pin to GND sets output voltage slew rate
8	GND	A resistor from this pin to GND sets the overload and short-circuit current limit. The pin can be used for current reporting, referring to the voltage developed over the current limit setting resistor
9	I_{LIM} / I_{MON}	A resistor from this pin to GND sets the overload and short-circuit current limit. The pin can be used for current reporting, referring to the voltage developed over the current limit setting resistor
10	ITimer	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for the fastest response to overcurrent events. Refer to circuit-breaker or active current limiting for more details

ORDERING INFORMATION

PART NUMBER	OVP	OCP	FAULT OUTPUT	RESPONSE TO FAULT	MARKING
SiP32435ADN-T5E3 (1)	Adjustable OVP	Active current clamping	/FLT	Latch-off	AA
SiP32435BDN-T5E3 (1)				Auto-retry	AB
SiP32436ADN-T5E3	Selectable over voltage clamping (3.9 V, 5.8 V, 14 V)		PGD	Latch-off	AC
SiP32436BDN-T5E3				Auto-retry	AD
SiP32437ADN-T5E3	Adjustable OVP	Circuit breaker		Latch-off	AE
SiP32437BDN-T5E3				Auto-retry	AF

Note
(1) In development. Contact Vishay for availability

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**CONDITION**	**LIMIT**	**UNIT**
Input voltage (V_{IN})	Reference to GND	-0.3 to +26.5	V
Output voltage (V_{OUT})	Reference to GND (non-reverse blocking option)	-0.6 to (VIN +0.3)	
	V_{OUT} pulse, < 1 µs	-0.7 V	
EN voltage	Reference to GND	-0.3 to +6.5	
OVP	Reference to GND	-0.3 to +6.5	
SS		Internally limited	
I_{TIMER}		Internally limited	
V_{PGTH}		-0.3 to +6.5	
PG and FLT voltage		-0.3 to +6.5	
VLIM		Internally limited	V
Maximum continuous switch current		Internally limited	A
Thermal resistance (R_{thJA})	Per JESD51-7: High Effective Thermal Conductivity Board for Leaded Surface Mount Packages. 4 thermal vias. 4 layers PCB	19	°C/W
ESD rating	HBM	± 2	kV
ESD rating	CDM	± 500	
Latch up current (V_{IN} and V_{OUT})		200	mA
Latch up current (control and signal puls)	Power input and output pins	100	
Temperature			
Operating junction temperature		-40 to +150	°C
Storage temperature		-65 to +150	
Maximum lead temperature		-	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
ELECTRICAL	**PIN**	**MIN.**	**MAX.**	**UNIT**
Input voltage (V_{IN})	IN	2.7	23	V
Output voltage (V_{OUT})	OUT	-	VIN	V
Enable pin voltage (V_{EN})	EN / UVLO	-	5	
OVP pin voltage (V_{OVP})	OVP	0.5	1.5	
P_{GTH} pin voltage (V_{PGTH})	P_{GTH}	-	5	
FLT pin voltage (V_{FLT})	FLT	-	5	
PG pin voltage (V_{PG})	PG	-	5	
ITIMER capacitor voltage (V_{ITIMER})	ITIMER	4	-	
LIM pin resistance to ground (R_{LIM})	I_{LIM}	-	-	
Reporting ratio, $I_{OUT} \geq 1$ A (V_{IMON})	I_{LIM}	96.5	114	µA/A
Continuous switch current (I_{MAX})	IN to OUT	-	8	A
Operating junction temperature (T_J)	-	-40	+125	°C

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED -40 °C < T_J < 125 °C, V_{IN} = 12 V, OUT = open, V_{EN} high = 2 V, V_{OVP} = 0 V for SiP32435 and SiP32437, R_{ILIM} = 715 Ω (target set 8 A), SS = open, I_{TIMER} = open, FLT = open for SiP32435, P_{GTH} = open for SiP32436 and SiP32437, P_G = open for SiP32436 and SiP32437	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply						
Quiescent current	$I_{Q(ON)}$	EN = 1.8 V, V_{IN} = 2.8 V to 23 V, V_{OUT} open	-	290	575	µA
Switch off current	$I_{Q(OFF)}$		-	55	135	
Shutdown current	I_{SD}	EN / UVLO < V_{SD} (F)	-	1.6	3	
V_{IN} undervoltage rising threshold	V_{UVP} (R)		2.39	2.6	2.82	V
V_{IN} undervoltage falling threshold	V_{UVP} (F)		2.32	2.48	2.64	
V_{IN} undervoltage threshold hysteresis	V_{UVP} (HYST)		-	120	-	mV
Overvoltage Clamp (OVC)						
Over voltage clamp threshold	V_{OVC}	OVCSEL = GND	3.6	3.8	4.2	V
		OVCSEL = open	5.25	5.75	6.15	
		OVCSEL = 390 k to GND	13	14.1	15.3	
Clamped output voltage	V_{CLAMP}	OVCSEL = GND	2.7	3.45	4.1	
		OVCSEL = open	4.8	5.5	6.2	
		OVCSEL = 390K to GND	12.3	13.4	14.6	
Output Load Current Monitor (I_{LIM})						
Analog switch current reporting gain	G_{IMON}	I_{OUT} < I_{LIM}, 1 A < I_{OUT} < 8 A	96.5	105.5	113.5	µA/A
	I_{MON} offset	When I_{OUT} < 1 A	-18	-	+16	µA
Overcurrent Protection						
Overcurrent threshold	I_{LIM}	R_{ILIM} = 6.65 kΩ	0.76	0.87	0.97	A
		R_{ILIM} = 3.32 kΩ	1.55	1.73	1.9	
		R_{ILIM} = 1.65 kΩ	3.2	3.48	3.7	
		R_{ILIM} = 750 Ω	7	7.67	8.15	
	I_{LIM}	I_{LIM} pin open	-	-	0.13	A
Pin shorted to GND	I_{LIM}	I_{LIM} pin shorted to GND	0.45	1.35	2.3	
	I_{FT}	Based on characterization	24	27	33	
Fast trip current to I_{LIM} ratio	$I_{SCRATIO}$		1.7	2	2.4	
Current limit foldback threshold	V_{FB}		-	50	-	%
Switch On Resistance						
	R_{ON}	I_{OUT} = 1 A, T_J = 25 °C	-	9.2	14	mΩ
Enable / Undervoltage Lockout (EN / UVLO)						
EN / UVLO rising threshold	V_{EN} (R)		1.17	1.21	1.25	V
EN / UVLO falling threshold	V_{EN} /F)		1.05	1.1	1.15	
EN/UVLO threshold hysteresis	V_{ENHYST}		60	100	140	mV
EN/UVLO leakage	I_{EN}	T_J = 25 °C	-0.1	-	+0.1	µA
EN / UVLO falling threshold for low shutdown current	V_{SD} (F)	Pull low enabled when voltage is less than VSD (F)	0.55	0.7	0.9	V
Overvoltage Protection (OVLO)						
OVLO rising threshold	V_{OV} (R)		1.15	1.2	1.25	V
OVLO falling threshold	V_{OV} (F)		1.05	1.1	1.17	
OVLO hysteresis	$V_{OV(HSYST)}$		25	90	150	mV
OVLO pin leakage current	V_{OVLKG}	0.5 V < VOVLO < 1.5 V, T_J = 25 °C (SiP32437x only)	-0.1	-	0.1	µA
		0.5 V < VOVLO < 1.5 V, T_J = 25 °C (SiP32436x)	-	1	4	

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED -40 °C < T_J < 125 °C, V_{IN} = 12 V, OUT = open, V_{EN} high = 2 V, V_{OVP} = 0 V for SiP32435 and SiP32437, R_{ILIM} = 715 Ω (target set 8 A), SS = open, I_{TIMER} = open, FLT = open for SiP32435, P_{GTH} = open for SiP32436 and SiP32437, P_G = open for SiP32436 and SiP32437	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Overcurrent Fault Timer (I_{TIMER})						
	I_{TIMER}	I_{TIMER} pin internal discharge current under OC condition	1.65	2	2.45	µA
30 % charge or discharge, but 1.5 V delta voltage on this pin, reference to GND or 1.2 V whatever. Below are parameter for discharge						
I_{TIMER} pin internal pull-up resistance	R_{ITIMER}		3	6	11	kΩ
I_{TIMER} pin internal pull-up voltage	V_{INT}		1.58	1.76	1.94	
I_{TIMER} comparator threshold under OC condition	V_{ITIMER} (F)		0.13	0.2	0.27	
I_{TIMER} charge / discharge differential voltage threshold under OC condition	ΔV_{ITIMER}		1.35	1.55	1.75	V
PGD, Power Good, SiP32436 and SiP32437						
Power good indication voltage	V_{PGD}	When asserted, V_{IN} > V_{UVP} (R), PG pin voltage while de-asserted	-	1.6	7.6	mV
		When de-asserted, V_{IN} < V_{UVP} (F), device is off, EN < V_{SD} (F), 250 µA pull up current.	650	830	1010	
PG pin leakage current	I_{PGLKG}	PG asserted, T_J = 25 °C	-	-	1	µA
Power Good Threshold (PGTH)						
PGTH rising threshold	V_{PGTH} (R)		1.14	1.2	1.28	V
PGTH falling threshold	V_{PGTH} (F)		1.03	1.1	1.16	
PGTH hysteresis	$V_{PGTH(HYST)}$		70	115	150	mV
PGTH pin leakage current	$I_{PGTHLKG}$	T_J = 25 °C	-0.1	-	0.1	µA
Over-temperature Protection (OTP)						
Thermal shutdown rising threshold	T_{SD}	Rising T_J	-	150	-	°C
Thermal shutdown hysteresis	T_{SDHYS}	Falling T_J	-	30	-	
Suggested max. operation T_J is 125 °C						
Soft Start Slew Rate (SS)						
SS internal charging current	I_{SS}		225	335	445	nA

PRODUCT TIMING

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply						
Overvoltage lockout response time	t_{OVLO}	V_{IN} > $V_{OV®}$ to V_{OUT} starts to fall	-	0.6	-	µs
Overvoltage clamp response time	t_{OVC}	V_{IN} > V_{OVC} to V_{OUT} starts to fall	-	5	-	
Circuit breaker response time	t_{CV}	From I_{OUT} at 1.3 x I_{LIM} to V_{OUT} fall. I_{TIMER} open	-	5.9	-	
Current limit response time	t_{LIM}	From I_{OUT} at 1.3 x I_{LIM} to I_{OUT} settling to within 5 % of I_{LIM}	-	0.35	-	
Short-circuit response time	t_{SC}	I_{OUT} > 3 x I_{LIM} to I_{OUT} cut off	-	300	-	ns
Fixed fast-trip response time	t_{FT}	I_{OUT} > IFT to I_{OUT} cut off	-	200	-	
Thermal Shutdown to auto-retry interval	$t_{TSD, RST}$	T_J < T_{SD} - T_{SDHYS}	-	34	-	
PG assertion de-glitch time	t_{PGA}	V_{PGTH} > V_{PGTH} (R) to PG rises	-	18	-	µs
PG de-assertion de-glitch time	t_{PGD}	V_{PGTH} > V_{PGTH} (F) to PG falls	-	18	-	
V_{OUT} slew rate	SR	R_L = 100 Ω, CL = 1µF, C_{SS} = 3.3 nF, V_{IN} = 2.7 V to 23 V, 25 °C	4.3	11	17.5	V/ms
Turn on delay	t_{ONDLY}	EN high to 10 % V_{OUT}, SiP32436x	540	865	1200	µs
		EN high to 10 % V_{OUT}, SiP32437x	335	655	985	

PGD LOGIC TABLE - SiP32436 AND SiP32437

EVENT	SWITCH STATUS	PGD OUTPUT	PGD DELAY
V_{IN} undervoltage, UVP or UVLO	Off	Low	NA
Overvoltage clamping, SiP32436	On, clamp	High, if P_{GTH} > V_{PGTH}(R) Low, if P_{GTH} < V_{PGTH}(F)	t_{PGA} t_{PGD}
Overvoltage, SiP32437 only	Off	Low	t_{PGD}
Switch ON	On	High, if P_{GTH} > V_{PGTH}(R) Low, if P_{GTH} < V_{PGTH}(F)	t_{PGA} t_{PGD}
Overcurrent during I_{TIMER} period	On	High, if P_{GTH} > V_{PGTH}(R) Low, if P_{GTH} < V_{PGTH}(F)	t_{PGA} t_{PGD}
Overcurrent, persistent, SiP32436, current clamping	On, clamp	High, if P_{GTH} > V_{PGTH}(R) Low, if P_{GTH} < V_{PGTH}(F)	t_{PGA} t_{PGD}
Overcurrent, persistent, SiP32437, circuit breaker	Off	Low	t_{PGA} t_{PGD}
Output short circuit / sever overcurrent	On, clamp	High, if P_{GTH} > V_{PGTH}(R) Low, if P_{GTH} < V_{PGTH}(F)	t_{PGA} t_{PGD}
Overtemperature	Off	Low, if P_{GTH} < 1.1 V	t_{PGD} + t_{ITIMER}
I_{LIM} pin open	Off	Low	t_{PGD}
I_{LIM} pin short to GND	Off	Low	t_{PGD}

FAULT RESPONSE AND /FLT LOGIC TABLE				
EVENT	**SWITCH RESPONSE**	**LATCHABLE FAULT**	**/FLT STATUS (SiP32435 ONLY)**	**/FLT ASSERTION DELAY**
V_{IN} undervoltage, UVP or UVLO	Off	No	High	
Overvoltage, SiP32435	Off	No	High	
Overvoltage, SiP32436	Voltage clamp	No	n/a	
Overvoltage, SiP32437	Off	No	n/a	
Overcurrent during I_{TIMER} period	No	No	n/a	
Overcurrent, persistent, SiP32436, current clamping	Current clamping	No	n/a	
Overcurrent, persistent, SiP32437x, circuit breaker	Off	Yes	n/a	
Output short circuit/sever overcurrent	Breaker then current limit	No	High	After I_{TIMER}
Overtemperature	Off	Yes	Low	
I_{LIM} pin open during normal steady state	Off	No	Low	After I_{TIMER}
I_{LIM} pin short to GND	Off	Yes	Low	After I_{TIMER}

Latchable faults can be reset either by V_{IN} power cycling or by pulling EN / UVLO below V_{SD} (F). This also resets the auto-retry timer. EN / UVLO should be below V_{SD} (F), not UVLO threshold.

Auto Retry option devices restart automatically and alert pin is de-asserted on the expiry of the t_{RST} (100 ms ~150 ms) timer.

TYPICAL CHARACTERISTICS

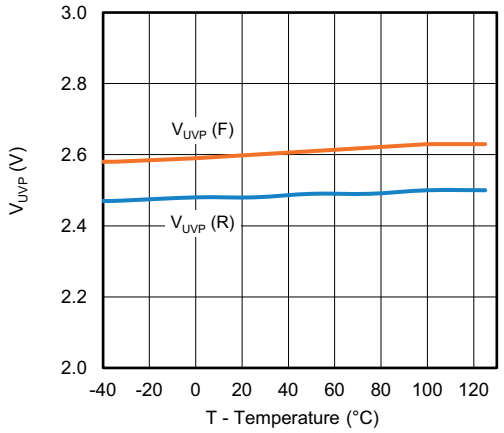


Fig. 3 - V_{IN} UVLO vs. Temperature

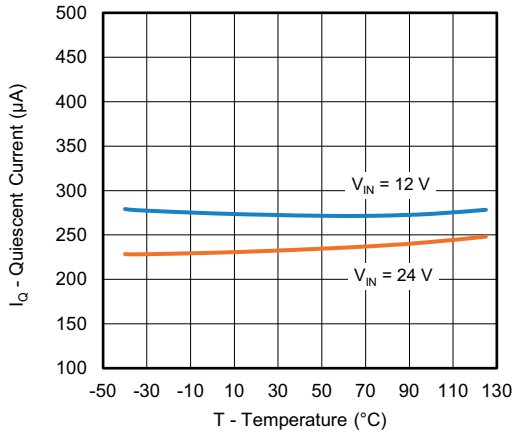


Fig. 4 - I_{QON} vs. Temperature

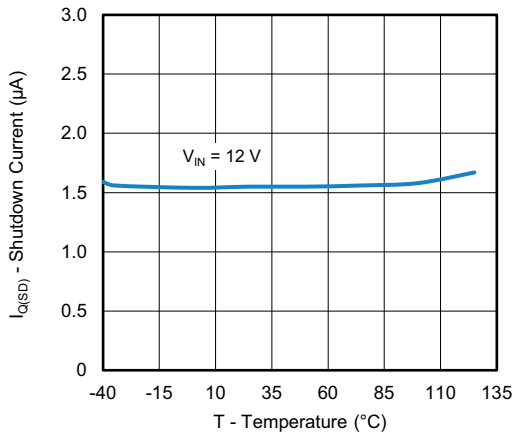


Fig. 5 - Shutdown Current vs. Temperature

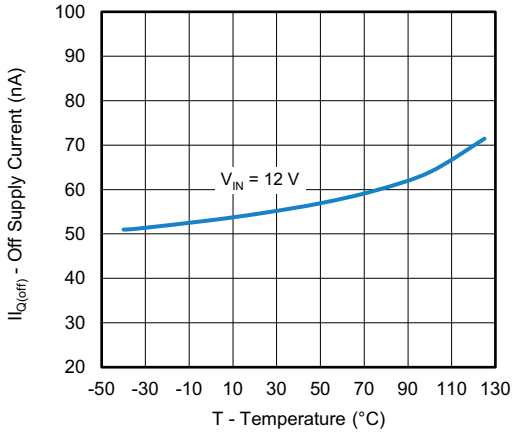


Fig. 6 - I_{QOFF} vs. Temperature

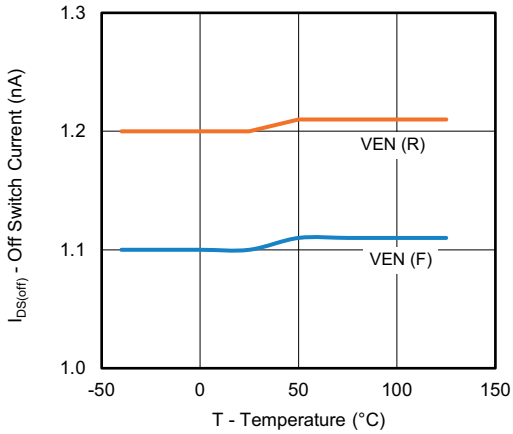


Fig. 7 - V_{EN} vs. Temperature

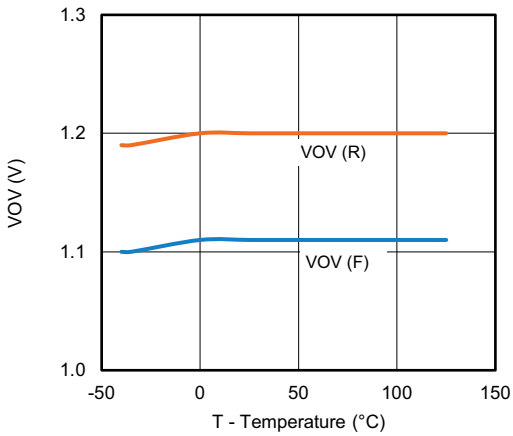


Fig. 8 - V_{OV} vs. Temperature

TYPICAL CHARACTERISTICS

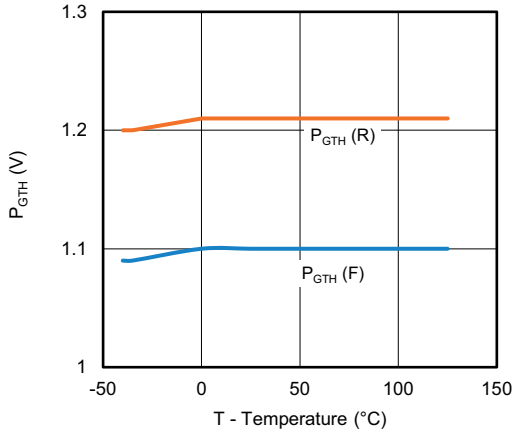


Fig. 9 - P_{GTH} Threshold vs. Temperature

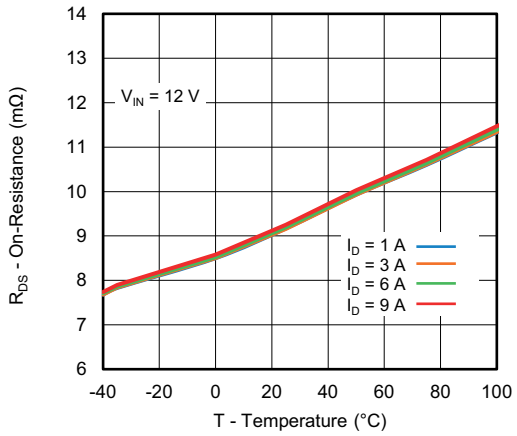


Fig. 10 - $R_{DS(on)}$ vs. Temperature

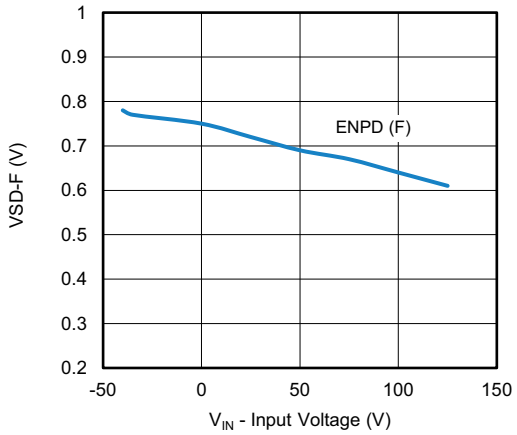


Fig. 11 - EN Shutdown Threshold vs. Temperature

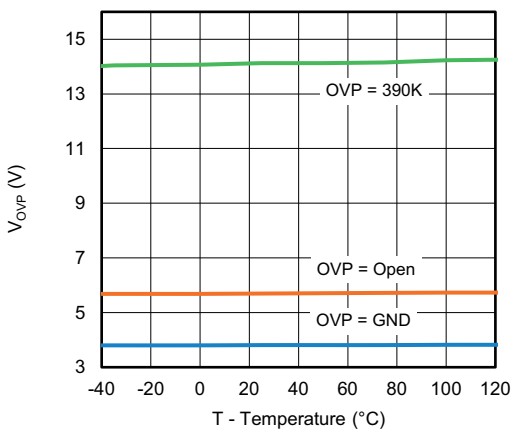


Fig. 12 - OV Threshold vs. Temperature

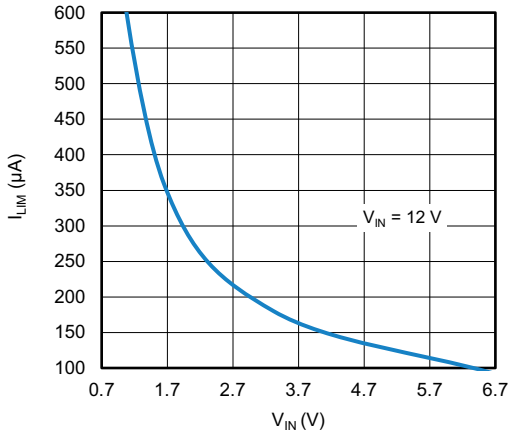


Fig. 13 - R_{LIM} vs. I_{LIM}

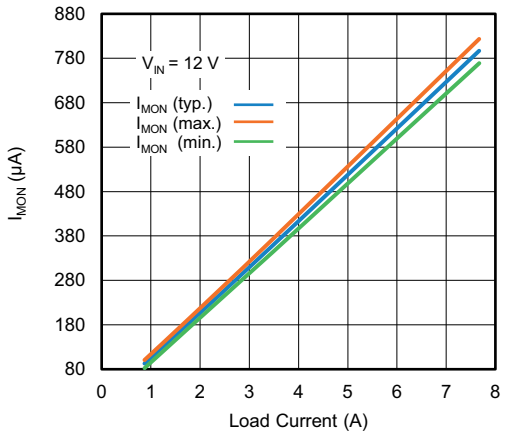


Fig. 14 - I_{LIM} vs. Load Current

TYPICAL CHARACTERISTICS

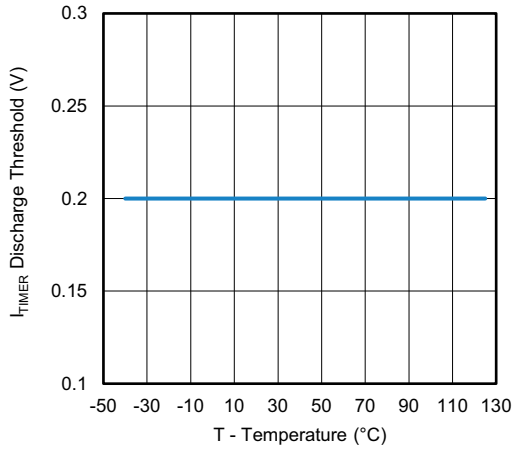


Fig. 15 - Timer Discharge Voltage vs. Temperature

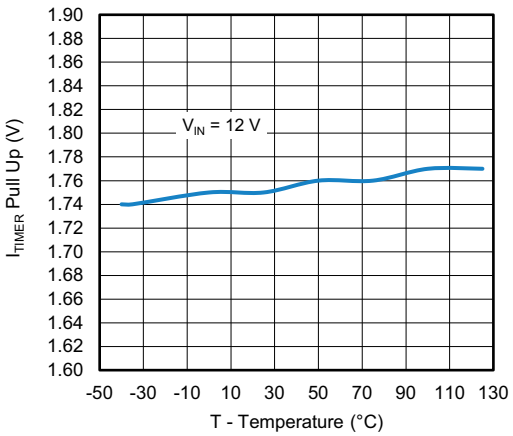


Fig. 17 - Timer Pull Up Voltage vs. Temperature

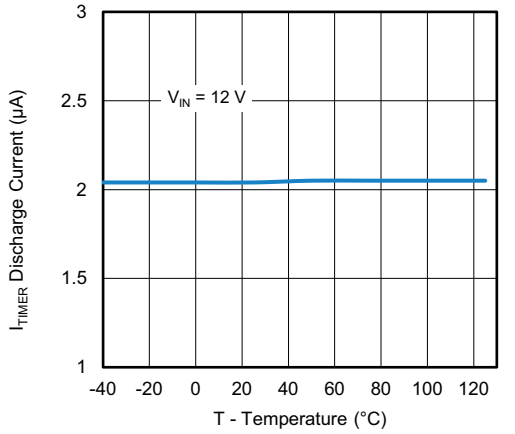


Fig. 16 - Timer Discharge Current vs. Temperature

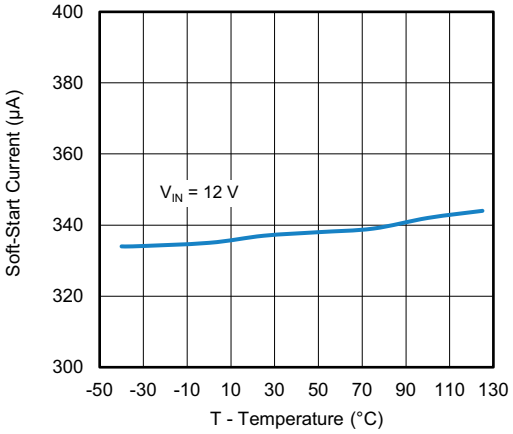


Fig. 18 - Soft-Start Current vs. Temperature

TYPICAL CHARACTERISTICS

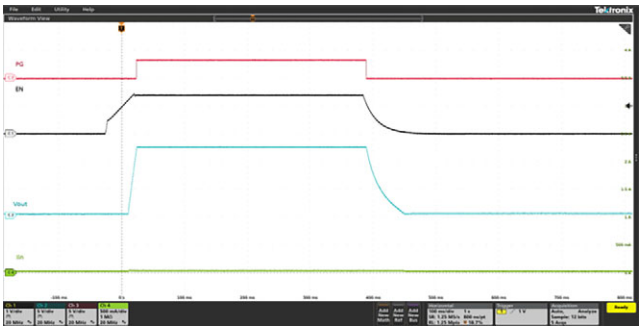


Fig. 19 - Power Up and Down With EN/UVLO Control
V_{IN} = 12 V, C_{OUT} = 22 µF, C_{SS} = 3.3 nF,
VEN/UVLO ramped from 0 V → 1.4 V → 0 V

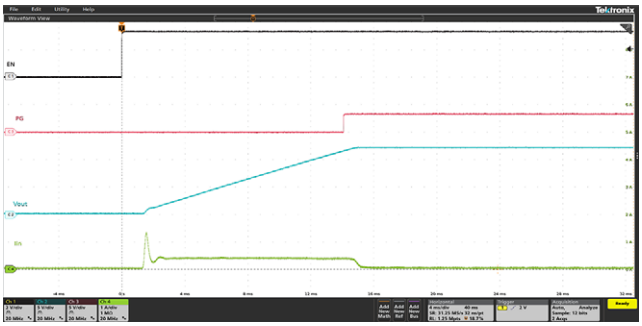


Fig. 22 - Inrush Current With Slew Rate Control – Capacitive Load
V_{IN} = 12 V, C_{OUT} = 470 µF, C_{SS} = 3.3 nF,
VEN/UVLO stepped up to 3.3 V

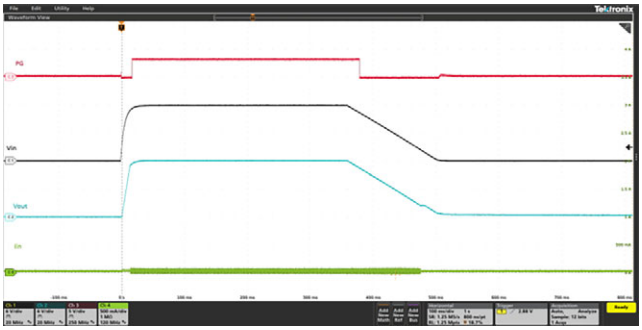


Fig. 20 - Power Up and Down With Input Supply
V_{IN} = 22 V, C_{OUT} = 22 µF, C_{SS} = 3.3 nF,
VEN/UVLO ramped from 0 V → 12 V → 0 V

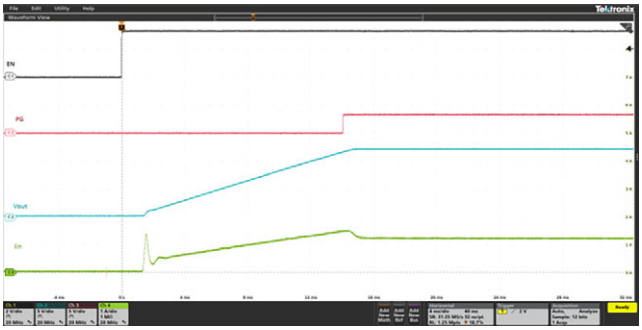


Fig. 23 - Inrush Current With Slew Rate Control – Resistive and Capacitive Load
V_{IN} = 12 V, C_{OUT} = 470 µF, R_{OUT} = 10 Ω, C_{SS} = 3.3nF,
VEN/UVLO stepped up to 3.3 V

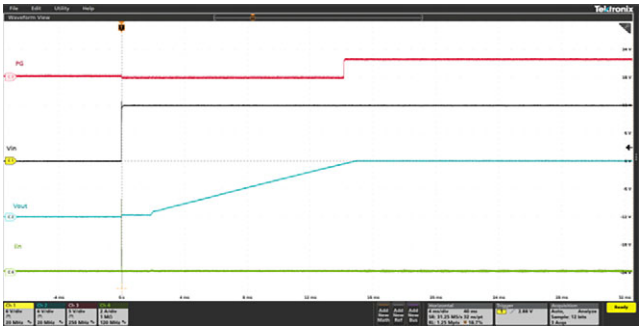


Fig. 21 - Power Up and Down With Input Supply
C_{OUT} = 22 µF, C_{SS} = 3.3 nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

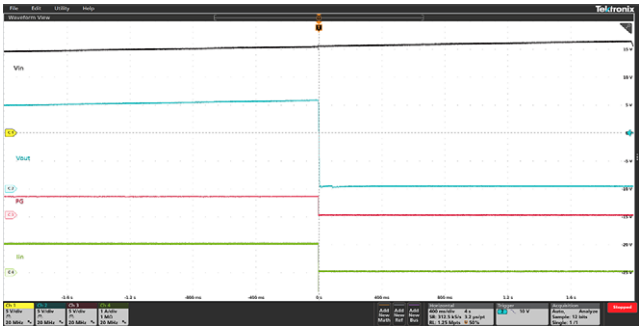


Fig. 24 - Overvoltage Lockout Response – SiP32437
OV threshold set to 15.8 V,
V_{IN} ramped up from 12 V to 16.5 V

TYPICAL CHARACTERISTICS

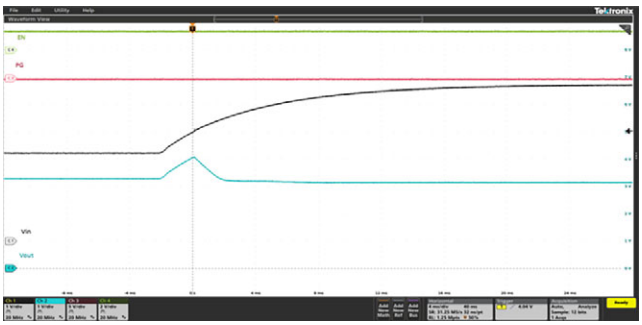


Fig. 25 - Overvoltage Clamp Response - SiP32436
ROVCSEL = GND, C_{OUT} = 220 µF, I_{OUT} = 200 mA,
V_{IN} ramped up from 3.3 V to 5.8 V

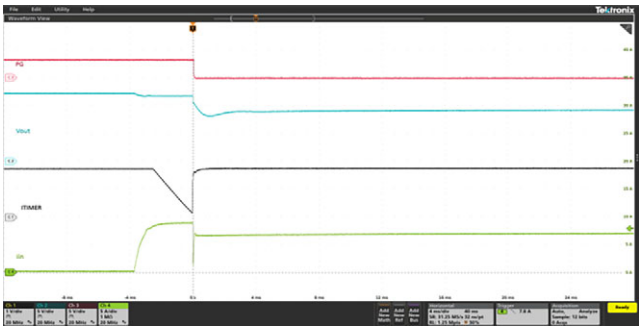


Fig. 28 - Active Current Limit Response - SiP32436
V_{IN} = 12 V, CITIMER = 3.3 nF, C_{OUT} = 220*2 µF,
R_{ILM} = 680 Ω, Resistor stepped from Open Ω → 1.3 Ω

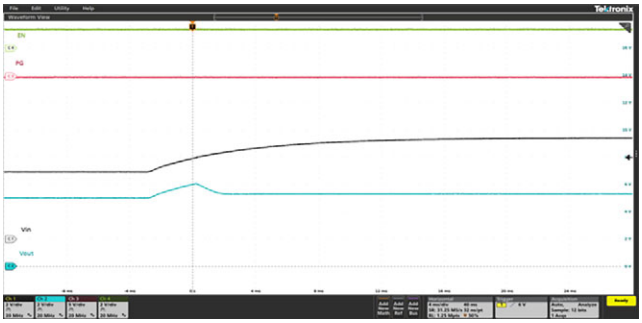


Fig. 26 - Overvoltage Clamp Response - SiP32436
ROVCSEL = Open, C_{OUT} = 220 µF, I_{OUT} = 200 mA,
V_{IN} ramped up from 5 V to 7.5 V

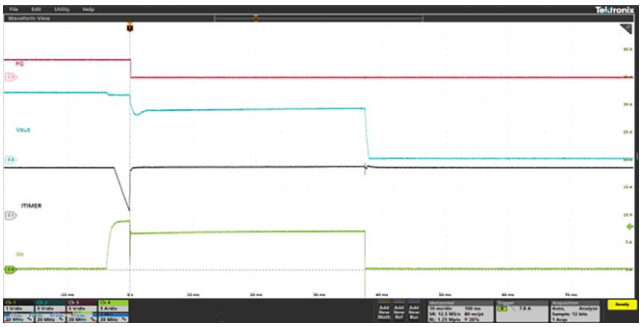


Fig. 29 - Active Current Limit Response Followed by TSD - SiP32436
V_{IN} = 12 V, CITIMER = 3.3 nF, C_{OUT} = 220*2 µF,
R_{ILM} = 680 Ω, Resistor stepped from Open Ω → 1.3 Ω

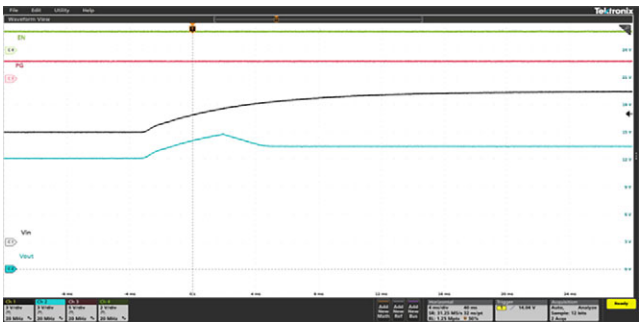


Fig. 27 - Overvoltage Clamp Response - SiP32436
ROVCSEL = 390 kΩ, C_{OUT} = 220 µF, I_{OUT} = 200 mA,
V_{IN} ramped up from 12 V to 16.5 V

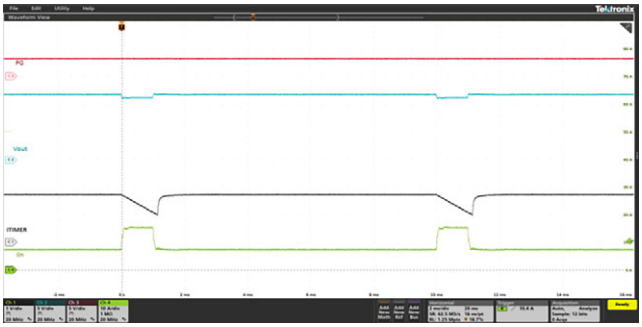


Fig. 30 - Transient Overcurrent Blanking Timer Response
V_{IN} = 12 V, CITIMER = 3.3 pF, C_{OUT} = 220*2 µF,
R_{ILM} = 680 Ω, I_{OUT} ramped
from 7 A → 15 A → 7 A within 1 ms

TYPICAL CHARACTERISTICS

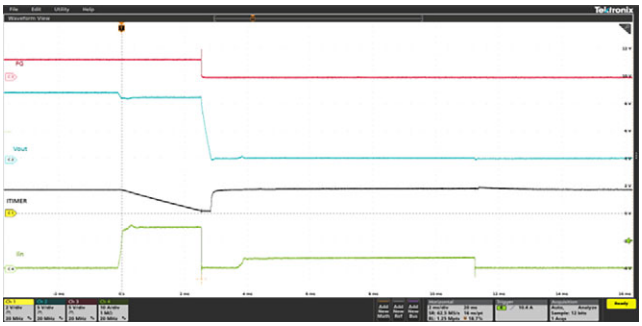


Fig. 31 - Circuit-Breaker Response SiP32437
V_{IN} = 12 V, CITIMER = 3.3 nF, C_{OUT} = 220*2 µF,
R_{ILM} = 680 Ω, I_{OUT} stepped from 0 A → 15 A

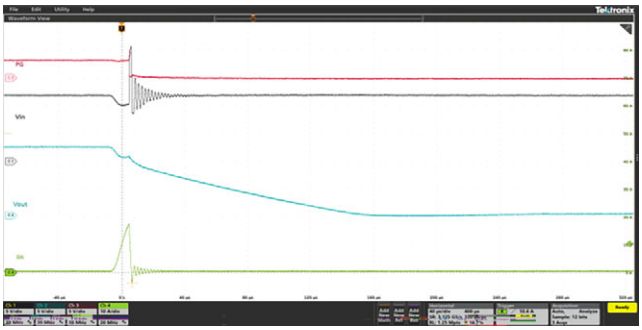


Fig. 33 - Output Short-Circuit During Steady State (Zoomed In)
V_{IN} = 12 V, R_{ILM} = 680 Ω,
OUT stepped from Open → Shortcircuit to GND

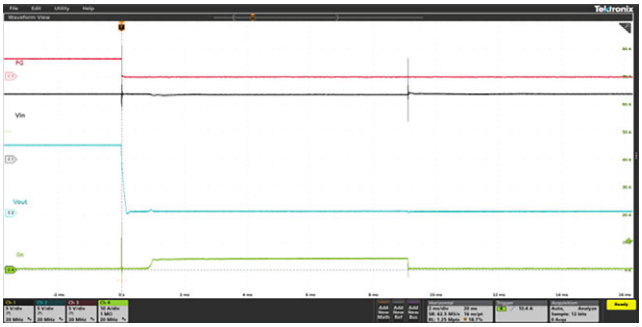


Fig. 32 - Output Short-Circuit During Steady Stat
V_{IN} = 12 V, R_{ILM} = 680 Ω,
OUT stepped from Open → Shortcircuit to GND

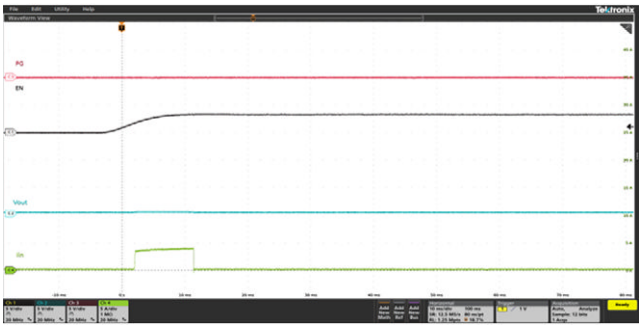


Fig. 34 - Power Up into Short-Circuit
V_{IN} = 12 V, C_{OUT} = Open, OUT short-circuit to GND,
R_{ILM} = 680 Ω, VEN/UVLO stepped from 0 V to 3.3 V

OVERVIEW

The SiP32435/6/7x is an eFuse that provides controllability and safety in power management system designs. The SiP32435/6/7x features programmable overvoltage, undervoltage, power good, and overcurrent protections, in addition to overtemperature shutdown. Its start-up output voltage slew rate can be set to control the inrush current level.

The devices operate when powered at the V_{IN}. When the V_{IN} clears the undervoltage lockout (UVLO) threshold, a logic high signal - higher than the VUVLO - on the EN / UVLO enables the integrated power path in a controlled slew rate.

The device monitors switch current from the start of the power path, and enables and controls the switch to ensure the user-defined overcurrent limit is not exceeded. The switch will go off swiftly to protect it from severe overcurrent conditions, such as short circuit. To cater for load circuits that require moderate transient surge current, an user-defined overcurrent blanking timer, iTimer, sets the time to allow the higher than I_{LIM} current to pass through the switch without switch-off interruption. Overvoltage on the V_{IN} is either clamped to selected thresholds (VOVC), or switched off if the overvoltage is higher than the user-defined UVLO thresholds. Such a design provides precise and prompt protection, in addition to immunity to circuit transients, for smooth circuit operation.

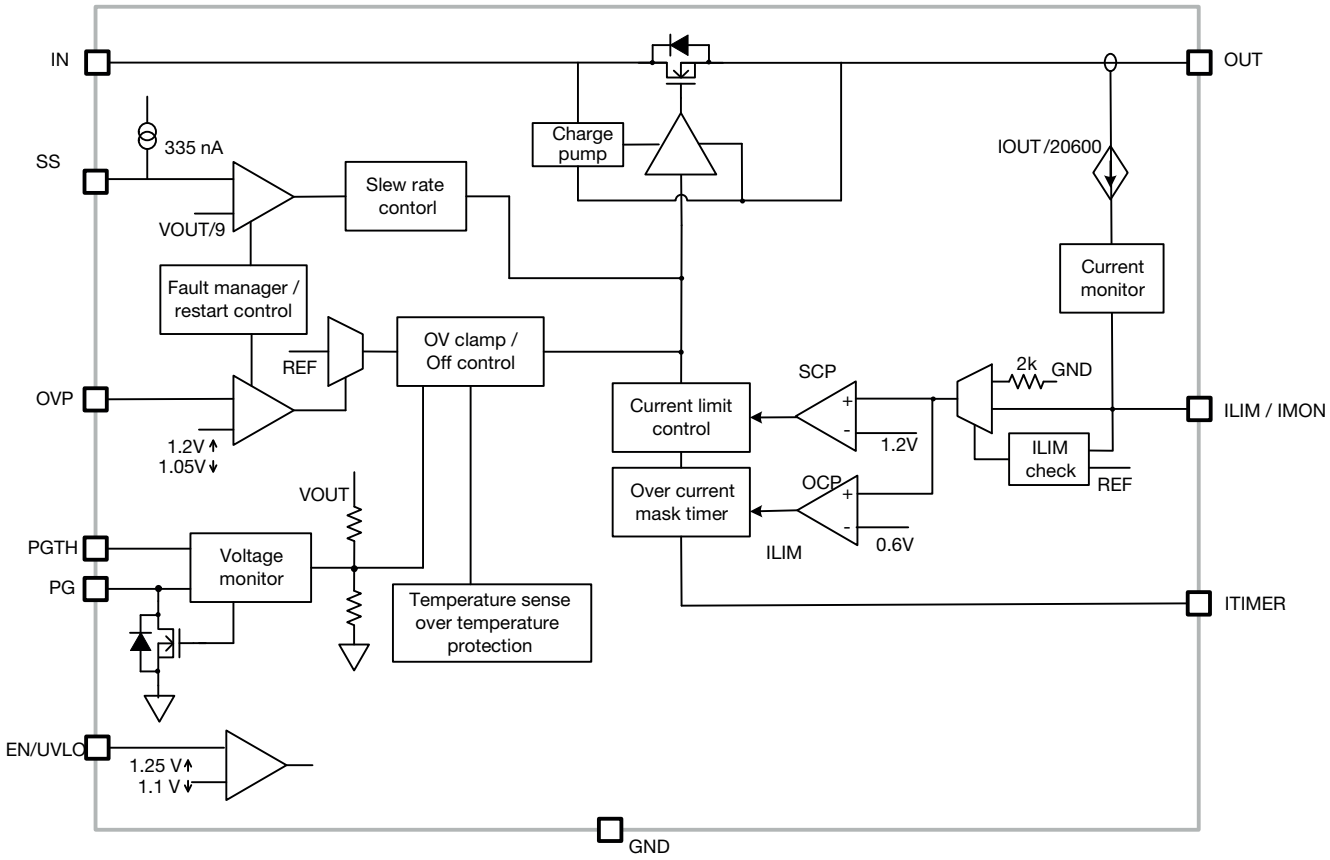


Fig. 35 - SiP3243x Block Diagram

PRODUCT FEATURES

Undervoltage Protections: Undervoltage Protection (UVP) and Undervoltage Lockout (UVLO)

The devices have two undervoltage protections. One is a built-in fixed threshold V_{IN} UVP (VUVP), which ensures that the V_{IN} voltage is sufficient for proper device operation. The other is undervoltage lockout (UVLO). A user-defined UVLO threshold can be set by the voltage resistor divider, as shown in Fig. 36.

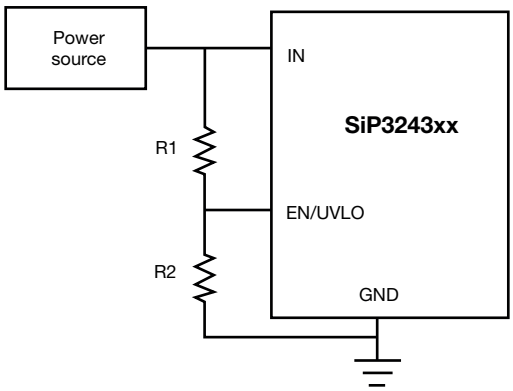


Fig. 36 - User-Defined V_{IN} Undervoltage Lockout

The equation below shows how a resistor divider sets the UVLO threshold per a given V_{IN} level.

$$V_{IN(UVP)} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2}$$

Overvoltage Protection

The SiP32435/6/7x has two overvoltage protection options to protect the load from input overvoltage conditions:

- The SiP32435x and SiP32437x feature user-defined overvoltage lockout (OVLO)
- The SiP32436x features overvoltage clamping (OVC) on three user-selected voltage levels (VOVC)

Overvoltage Protection (OVLO)

The SiP32435x and SiP32437x VIN OVLO thresholds can be set by a resistor divider, as per Fig. 37. When the voltage on OVLO crosses the OVLO rising threshold, $V_{OV(R)}$, the switch is off. The switch will be ON again when the voltage on OVLO falls across $V_{OV(F)}$. The switch on follows the slew rate. Overvoltage is not a latchable fault, meaning when the fault is removed, the switch will turn on again.

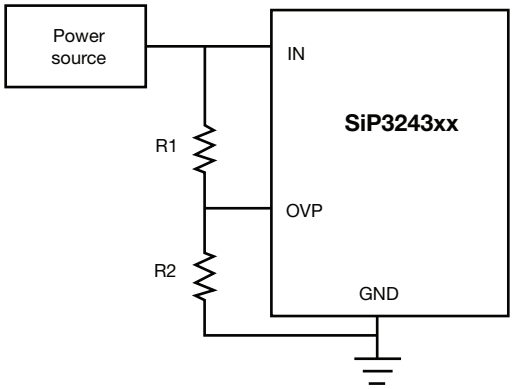


Fig. 37 - User-Defined Overvoltage Lockout

The equation below shows how a resistor divider sets the OVLO threshold per a given V_{IN} level.

$$V_{IN(OV)} = \frac{V_{OV} \times (R_1 + R_2)}{R_2}$$

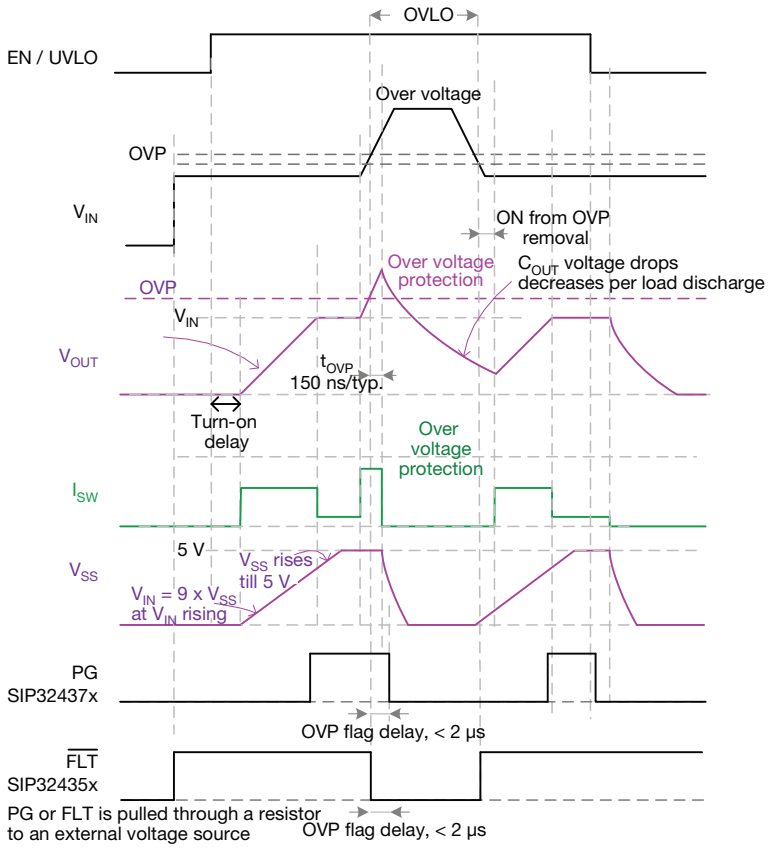


Fig. 38 - SiP32435x and SiP32437x Overvoltage Lockout and Recovery

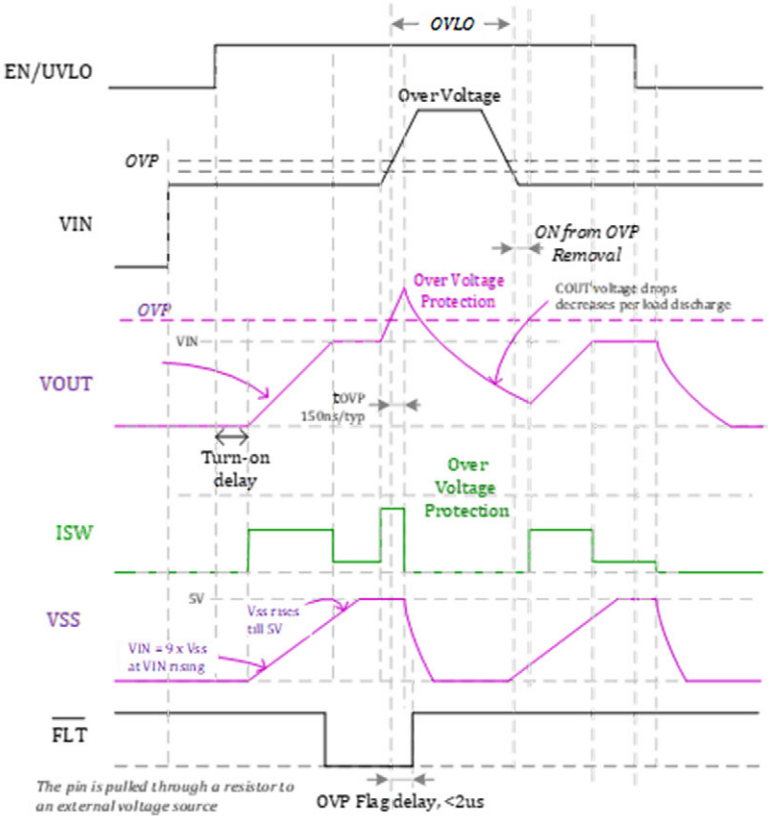


Fig. 39 - SiP32435x Overvoltage Lockout and Recovery

Overvoltage Clamping (OVC)

When the V_{IN} voltage exceeds the overvoltage clamp threshold (V_{OVC}), the SiP32436x regulates the switch and clamps the output to the voltage level of V_{CLAMP}. There are three V_{CLAMP} threshold levels that can be selected by the OVCSEL pin.

SiP32436x OVCSEL PIN SETTING	
OVCSEL PIN SETTING	**OVERVOLTAGE CLAMPING THRESHOLD**
Connected to GND	3.8 V
Open	5.8 V
Connect to GND through a 390 kΩ resistor	14.2 V

The device stays in the clamping state as long as the V_{IN} overvoltage persists. The device's power dissipation could be high in this state. If such a clamping condition lasts for an extended period, overtemperature protection could shut down the switch if T_J reaches the OTP threshold. For the auto-retry option, the device will restart after a delay time of 34x of t_{SS}.

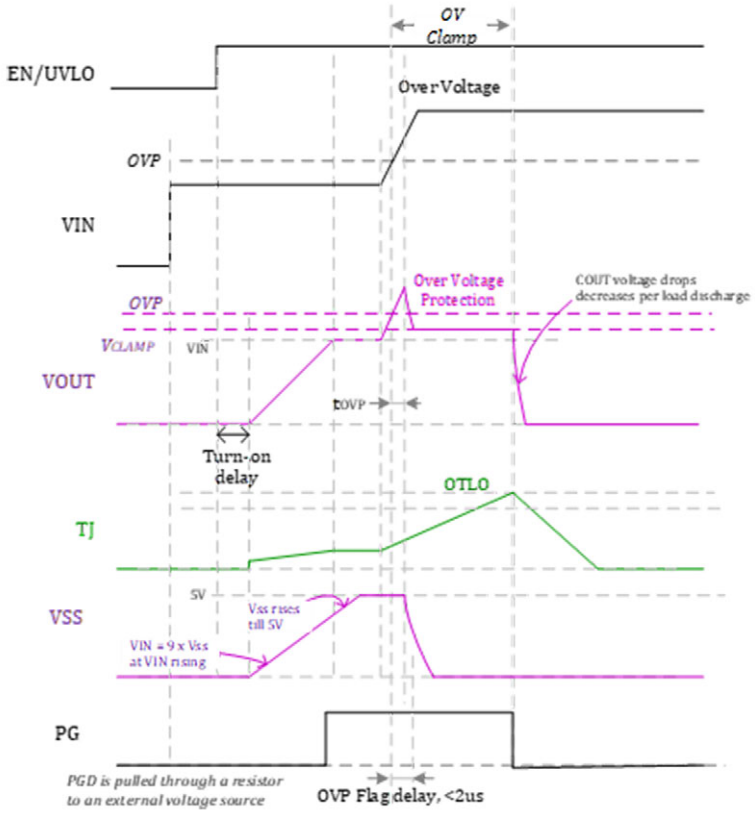


Fig. 40 - SiP32436x Overvoltage Clamping and Recovery

Turn-on Slew Rate and Inrush Current Management

A heavy capacitive load or hot-plug event can result in large inrush current or sparking at the connector contact. Such conditions should be properly managed to minimize the inrush current for a smooth switch-on transition without causing system power bus interruption or connector damage. The below equation shows how to determine the slew rate, given inrush current limit and load capacitance. Given the inrush current limit, load capacitance, and operation voltage, the proper soft start time can be determined.

$$\text{Slew Rate} = \frac{V_{OUT}}{t_{SS}} = \frac{I_{INRUSH}}{C_{OUT}}$$

The capacitor connected between SS and GND determines the device's soft start slew rate. The output slew rate control circuit regulates the V_{OUT} to 9x of V_{SS}.

$$\text{Slew Rate} = \frac{V_{OUT}}{t_{SS}} = \frac{I_{SS}}{C_{SS}} \times 9$$

For the fastest output slew rate, please leave the SS pin open.

During the soft start, when V_{OUT} is below 50 % of V_{IN}, the overcurrent limit threshold is folded back by 50 %. Together with overtemperature protection, the devices are protected from overstress conditions that could result in degraded reliability.

Circuit Breaker - SiP32437x

The SiP32437x will turn off the switch if the output overcurrent condition persists after the user-defined fault blanking time.

The device overcurrent threshold is set by R_{LIM} and its overcurrent fault blanking time is set by iTimer. When the load current crosses the overcurrent threshold, the iTimer circuit starts counting the time by discharging the capacitor (C_{ITIMER}) with a constant I_{ITMER} (2 µA). If the overcurrent condition still exists when the voltage on C_{ITIMER} is discharged by ΔV_{ITIMER}, the switch will be turned off, otherwise iTimer will reset as soon as the current falls below the I_{LIM} level. In the event the load current reaches the short circuit protection threshold (2 x I_{LIM}), the switch will be turned off immediately.

The overcurrent limit (I_{LIM}) for a set resistor (R_{ILIM}) can be calculated by the equation below.

$$R_{ILIM} = \frac{600\ mV}{G_{IMON} \times I_{LIM}}$$

G_{IMON} is the switch current sense gain on the I_{LIM} / I_{MON} pin of 105.5 µA/A.

The overcurrent blanking time, which allows the load current transient, can be programmed by the capacitor (C_{ITIMER}) connected between the iTimer pin and GND.

$$iTimer = \frac{I_{ITIMER}}{C_{ITIMER} \times \Delta V_{ITIMER}}$$

ΔV_{ITIMER} is 1.55 V

I_{ITIMER} is 2 µA

It is recommended to leave the iTimer pin open if the fastest overcurrent switch-off response is required.

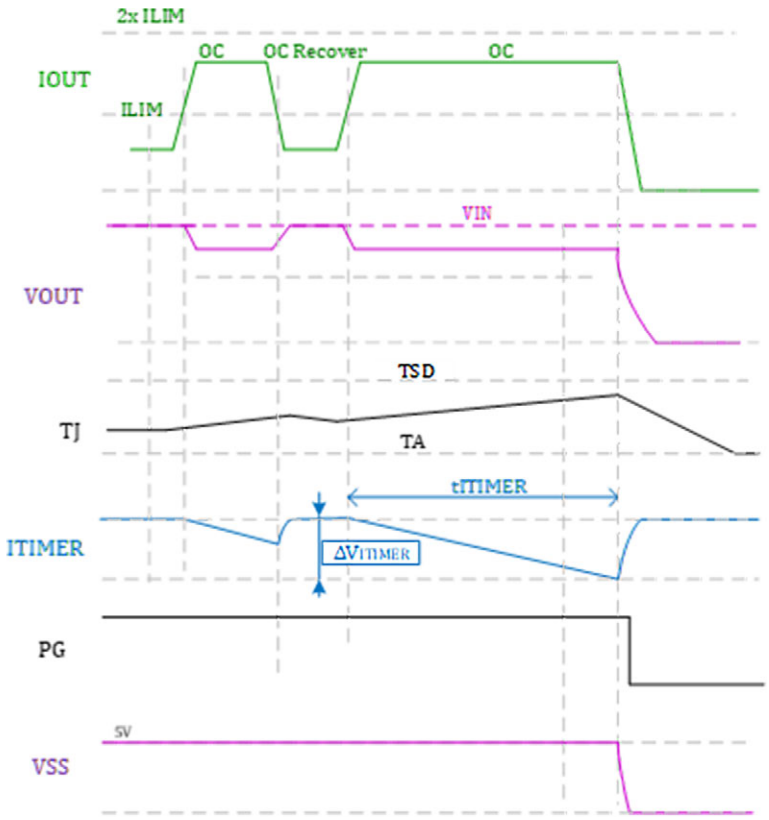


Fig. 41 - SiP32437x Overcurrent Operation

The switch-off upon overcurrent will stay latched off until the V_{IN} power reset, logic toggling, or the auto-retry feature is active.

Current Limiting / Active Current Clamping - SiP32435x and SiP32436x

The SiP32435x and SiP32436x will actively regulate the output current if the output overcurrent condition persists after the user-defined fault blanking time.

The device overcurrent threshold is set by R_{LIM} and its overcurrent fault blanking time is set by iTimer. When the load current crosses the overcurrent threshold, the iTimer circuit starts counting the time by discharging the capacitor (C_{ITIMER}) with a constant I_{ITMER} (2 µA). If the overcurrent condition still exists when the voltage on C_{ITMER} is discharged by ΔV_{ITMER}, the switch will actively regulate the output current to the overcurrent threshold set by R_{ILIM}. Otherwise, iTimer will reset as soon as the current falls below the I_{LIM} level. In the event the load current reaches the short circuit protection threshold (2 x I_{LIMI}), the switch will be turned off immediately.

The overcurrent threshold is set up by the resistor (R_{ILIM}) on the I_{LIM} pin. The overcurrent limit (I_{LIM}) set by the resistor (R_{ILIM}) can be calculated by the equation below.

$$R_{ILIM} = \frac{600\ mV}{G_{IMON} \times I_{LIM}}$$

G_{IMON} is the switch current sense gain on the I_{LIM} / I_{MON} pin of 105.5 µA/A.

The overcurrent blanking time, which allows the load current transient, can be programmed by the capacitor (C_{ITIMER}) connected between the iTimer pin and GND.

$$iTimer = \frac{I_{ITIMER}}{C_{ITIMER} \times \Delta V_{ITIMER}}$$

When the I_{LIM} pin is open, the current limit is set to a low current level below 0.13 A. The part will begin overcurrent clamping with the very light load. In case the I_{LIM} is short is GND, the overcurrent clamping is set to 1.35 A typically.

The overcurrent protection circuit implements a foldback scheme when the V_{OUT} is below 50 % of V_{IN}.

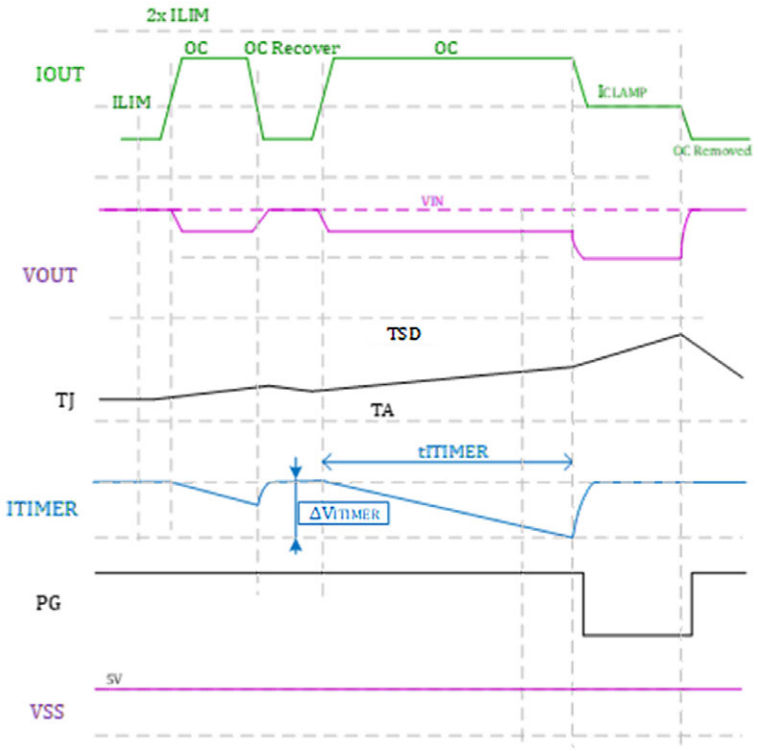


Fig. 42 - SiP32435x and SiP32436x Active Overcurrent Clamping Operation

When the iTimer pin is open, the devices will respond to overcurrent with a minimum possible delay.

During start-up, the devices will respond to overcurrent events without any delay (blanking time). They will actively regulate the output current to the set I_{LIM} level. There is no circuit breaker mode during start-up. iTimer is active only after the start-up is completed.

If overcurrent happens during output voltage clamping for the SiP32436x, overcurrent clamping will be engaged immediately without the blanking timer.

Overcurrent clamping could result in overheating due to increased power dissipation across the switch. Thermal protection will kick in once the junction temperature reaches the thermal shutdown threshold (TSD).

Severe Overcurrent and Short Circuit Protection

The severe overcurrent threshold is 2x I_{LIM}. There is also an internal fixed short circuit protection threshold of 27 A. The severe overcurrent will turn off the switch.

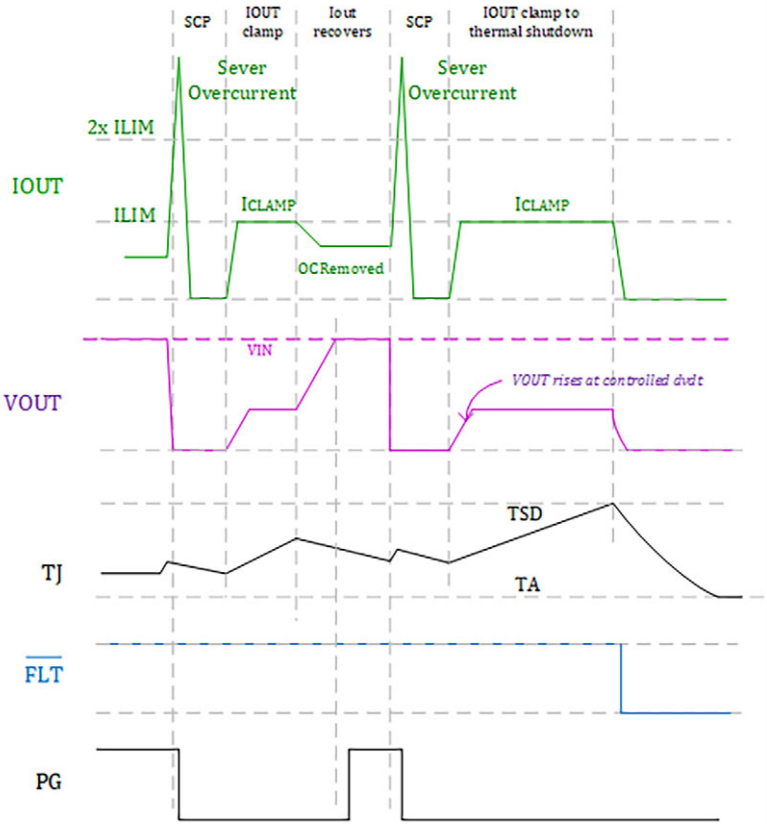


Fig. 43 - SiP32435x and SiP32436x Active Overcurrent Clamping Operation

Analog Current Reporting Through ILIM

The I_{LIM} pin can serve both overcurrent limit setting and current reporting functions. The application circuit can acquire switch current through reading the voltage on the I_{LIM} pin, since its voltage developed over R_{LIM} is proportional to its switch current. 600 mV on the I_{LIM} pin represents the current of the overcurrent threshold level.

$$I_{OUT} = \frac{V_{ILIM}}{R_{ILIM} \times G_{IMON}}$$

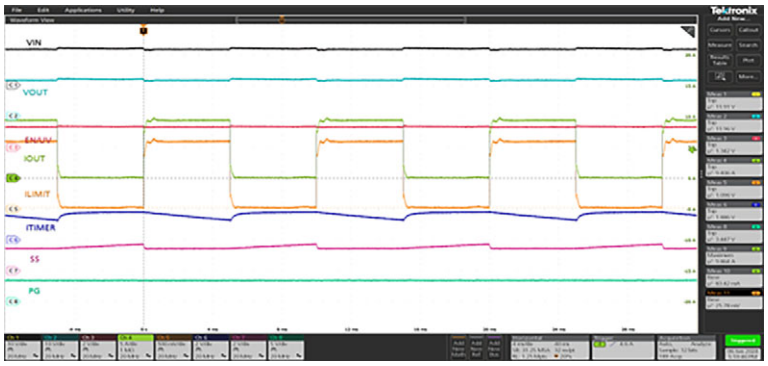


Fig. 44 - I_{MON} Current Monitor Response

The circuit load current is the switch current plus the output capacitance current.

Overtemperature Protection

The overtemperature protection circuit is active all the time, monitors the junction temperatures, and shuts the switch off under any condition as soon as it reaches thermal shutdown threshold (TSD), protecting the device from damage or performance and reliability degradation. When the junction temperature cools down by the thermal shutdown hysteresis (TSDHYS), the device can be turned on.

DEVICE	OVERTEMPERATUR PROTECTION RESET
SiP3243xA, latch-off option	T_J falls by TSDHYS below the TSD; V_{IN} recycled or EN / UVLO toggled
SiP3243xB, auto-retry option	Once T_J falls by TSDHYS below the TSD, the device's auto-retry timer will be on and gets in start-up if EN / UVLO is at logic high (Fig. 45, auto-retry option)

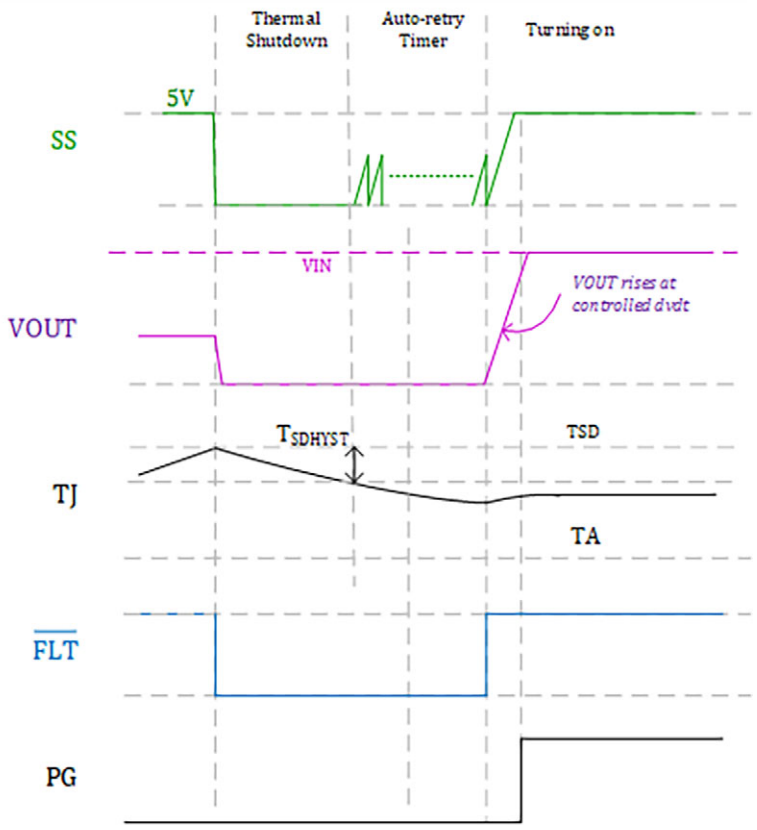


Fig. 45 - SiP3243xB Auto-Retry, Exit From Thermal Shutdown

Fault Event Response and FLT Output

The SiP32435x has an open drain output pin (FLT) that indicates a fault with an active low signal. The table below summarizes the device's responses to various fault conditions.

FAULT EVENT	LATCHED FAULT	FLT PIN OUTPUT	DEVICE RESPONSE
Overtemperature	Y	L	Shutdown
Undervoltage	N	H	Shutdown
Overvoltage (SiP32437x)	N	H	Shutdown
Overvoltage (SiP32436x)	N	H	Voltage clamp
Overcurrent (transient, < 2 x I_{LIM})	N	H	No
Continuous overcurrent (SiP32437x)	Y	L	Circuit breaker
Continuous overcurrent (SiP32436x)	Y	H	Current clamp after iTIMER
Output severe overcurrent (SiP32437x)	Y	L	Circuit breaker
Output severe overcurrent (SiP32436x)	Y	L	Current clamp
Overtemperature	Y	L	Shutdown
I_{LIM} pin open	N	L	Shutdown after iTIMER
I_{LIM} pin short to ground	N	L	Shutdown after iTIMER

The devices' latched fault status can be reset by recycling V_{IN} to GND or toggling the EN / UVLO pin below VSD. This will clear the fault indication on /FLT and reset the auto-retry timer for the SiP32435B variant.

Auto-retry variants, SiP3243xB, restart automatically after t_{RST}, which is 34x of t_R, upon the fault latch.

Fault Event Response and PG Output

The PG pin of the SiP32436x and SiP32437x provides an active high output indicating power good. This is an open drain output pin that must be pulled up to an external bias voltage source. P_G high is asserted when the P_{GTH} pin voltage meets the required level and proper device states.

P_G is de-asserted during operation in the event the P_{GTH} voltage falls below $V_{PGTH(F)}$, or a fault is detected.

This open drain output pin indicates a fault with an active low signal.

PG PIN INDICATION SUMMARY		
FAULT EVENT	**SWITCH RESPONSE**	**PG PIN STATUS**
Overtemperature	Off	L
Normal ON operation	On	H, if P_{GTH} pin voltage > $V_{PGTH(R)}$ L, if P_{GTH} pin voltage < $V_{PGTH(L)}$
Undervoltage	Off	L
Overvoltage (SiP32436x)	On (VOUT clamping)	H, if P_{GTH} pin voltage > $V_{PGTH(R)}$ L, if P_{GTH} pin voltage < $V_{PGTH(L)}$
Overvoltage (SiP32437x)	Off	L
Overcurrent (transient, < 2 x I_{LIM})	On	H, if P_{GTH} pin voltage > $V_{PGTH(R)}$ L, if P_{GTH} pin voltage < $V_{PGTH(L)}$
Continuous overcurrent (SiP32436x)	On (IOUT limiting)	H, if P_{GTH} pin voltage > $V_{PGTH(R)}$ L, if P_{GTH} pin voltage < $V_{PGTH(L)}$
Continuous overcurrent (SiP32437x)	Off (circuit breaker variants)	L
Output severe overcurrent (SiP32436x)	Current limit	H, if P_{GTH} pin voltage > $V_{PGTH(R)}$ L, if P_{GTH} pin voltage < $V_{PGTH(L)}$
Output severe overcurrent (SiP32437x)	Current limit	H, if P_{GTH} pin voltage > $V_{PGTH(R)}$ L, if P_{GTH} pin voltage < $V_{PGTH(L)}$
I_{LIM} pin open	Off	L
I_{LIM} pin short to ground	Off	L

Device Applications

The recommended V_{IN} operation voltage for the SiP3243xx series is 2.7 V to 23 V. It provides protection features of undervoltage, adjustable overvoltage, adjustable slew rate and inrush control, overcurrent, and overtemperature. It is always suggested to have a ceramic input bypass capacitor of 0.1 µF or higher. The switch current flow is shut off promptly in the event of short circuit or overcurrent events, the input path inductance generates a positive voltage, and the output path inductance brings a negative spike at the V_{OUT} pin. Such a surge / spike voltage could exceed the devices' rating. Measures that can be taken to address the voltage spike include:

- Minimized power path length
- Maximized V_{IN} PCB trace and GND plane
- Adding TVS at V_{IN}, and a Schottky diode at V_{OUT}
- Adding a 1 µA ceramic capacitor at VIN, close to the device

Fig. 46 and Fig. 47 show typical designs for single device self-controlled and host device controlled. In case of host device controlled designs, the EN / UVLO and / or OVLO pins can be driven by the host device's GPIOs to achieve both logic high and logic low enable.

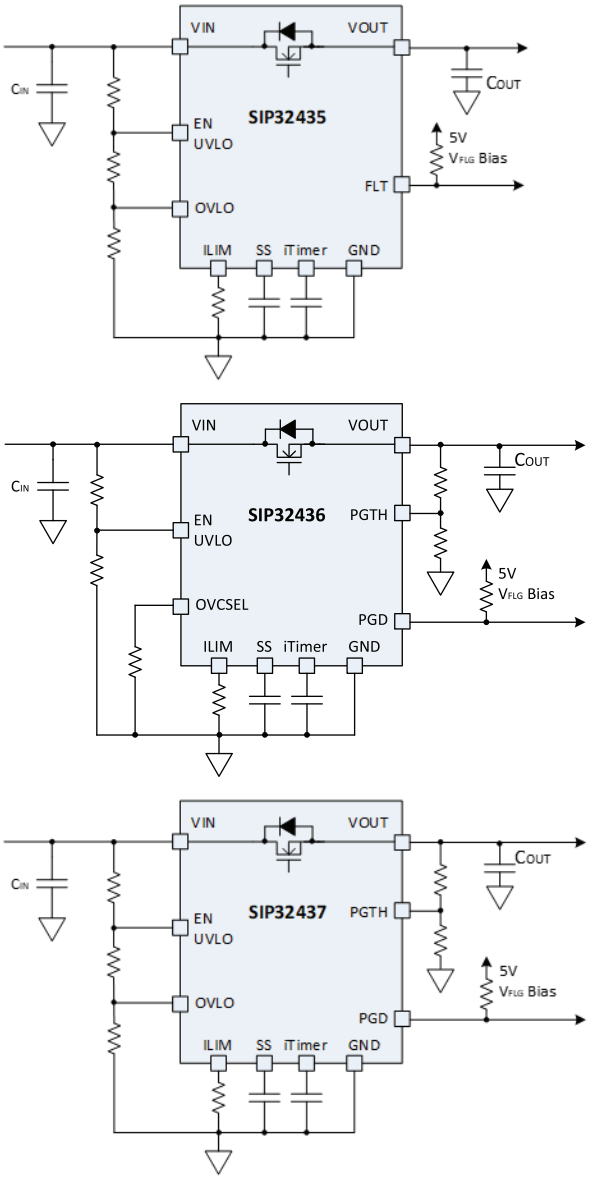


Fig. 46 - Typical Single Device, Self-Controlled Designs

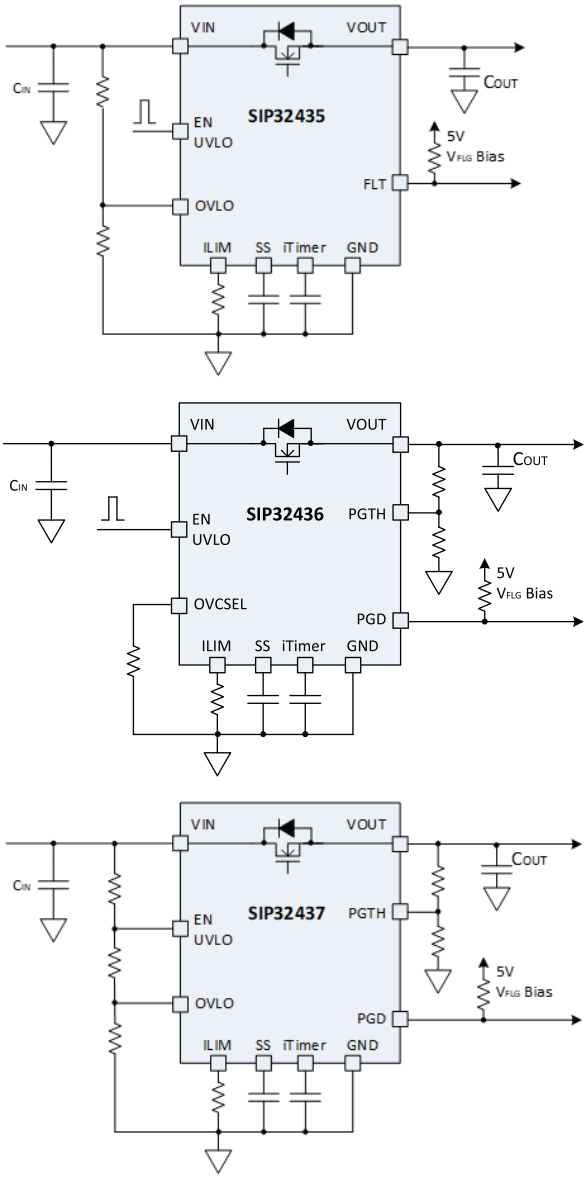


Fig. 47 - Typical Single Device, Host Device Controlled Designs

Application Circuit Designs

Fig. 48 shows a typical design to protect input power from load overcurrent events. This is common on various add-on functional cards in computing and network systems. For PCIE-powered cards, the SiP3243xx fits both 12 V and 3.3 V power rails.

The SiP32437B is selected for this design, which requires circuit breaker response overcurrent protection with auto retry upon a fault condition.

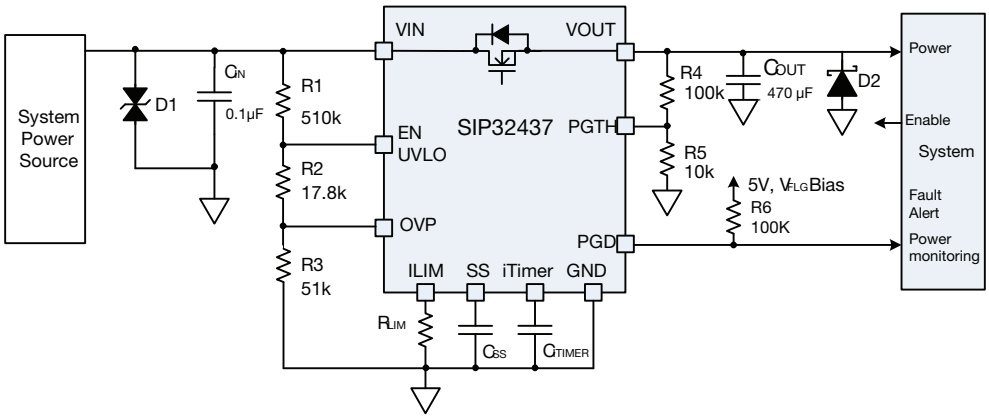


Fig. 48 - Application Circuit Design Example

CIRCUIT DESIGN REQUIREMENTS	
PARAMETER	**TARGET VALUE**
Input power voltage (V_{IN})	12 V
Undervoltage ($V_{IN(UVLO)}$)	10.2 V
Input overvoltage (VIN(OVLO))	13.8 V
Output power good ($V_{OUT(PG)}$)	11.4 V
Max. continuous current	7 A
Start-up V_{OUT} rise time (t_R)	25 ms
Output transient current blanking time (t_{iTIMER})	2 ms
Output capacitance (C_{OUT})	470 µA
Overcurrent limit	8 A

Setting Power Input Undervoltage and Overvoltage Thresholds

The R_1, R_2, and R_3 resistors set the V_{IN} overvoltage and undervoltage thresholds per the equations below:

$$V_{IN(OVLO)} = \frac{V_{OVLO(R)} \times (R_1 + R_2 + R_3)}{R_3}$$

$$V_{IN(UVLO)} = \frac{V_{UVLO(R)} \times (R_1 + R_2 + R_3)}{R_2 + R_3}$$

The R_1, R_2, and R_3 stand for a leakage path to the V_{IN}. The lower resistance of these resistors will increase the leakage. In the meantime, the EN / UVLO and OVLO pin leakages affect the accuracy of the V_{IN} overvoltage and undervoltage settings. Considering this factor, it is suggested to select the R_1, R_2, and R_3 resistance levels to ensure its current is 20x higher than the EN / UVLO and OVLO pin leakages.

Both the EN / UVLO and OVLO pins' maximum leakage currents are 0.1 µA. The R_1, R_2, and R_3 total resistance should be less than 3 MΩ. The design targets $V_{IN(OVLO)}$ of 13.8 V and $V_{IN(UVLO)}$ of 10.2 V, with $V_{OVLO(R)}$ and $V_{UVLO(R)}$ of 1.2 V. First select 510 kΩ for R_1, then resolve equations (1) and (2) with R_2 of 17.74 kΩ and R_3 of 50.26 kΩ. Round to the closest standard values: R_1 = 510 kΩ, R_2 = 17.74 kΩ, and R_3 = 51 kΩ.

Setting Power-Good Threshold

Resistors R_4 and R_5, connected to the P_{GTH} pin per Fig. 48, set the power good threshold. The power good assertion threshold with rising output voltage can be calculated as:

$$V_{PG} = \frac{V_{PGTH(R)} \times (R_2 + R_3)}{R_5}$$

The P_{GTH} pin leakage current causes an error in the calculation. It is suggested to set the R_4 / R_5 resistor current 20 times or greater than the leakage current. As shown in the specifications, the P_{GTH} maximum leakage current is 1 µA, and the target V_{OUT} power good is 11.4 V. The R_4 / R_5 resistance should be less than 600 kΩ. First, select R_5 = 10 kΩ, and resolve the equation with R_4 = 95 kΩ. Choose the closest standard resistor value as R_4 = 95.3 kΩ.

Both the EN / UVLO and OVLO pins' maximum leakage currents are 0.1 µA. The R_1, R_2, and R_3 total resistance should be less than 3 MΩ. The design targets $V_{IN(OVLO)}$ of 13.8 V and $V_{IN(UVLO)}$ of 10.2 V, with $V_{OVLO(R)}$ and $V_{UVLO(R)}$ of 1.2 V. First select 510 kΩ for R_1, then resolve equations (1) and (2) with R_2 of 17.74 kΩ and R_3 of 50.26 kΩ. Round to the closest standard values: R_1 = 510 kΩ, R_2 = 17.74 kΩ, and R_3 = 51 kΩ.

Setting Overcurrent / Current Limit Thresholds

The overcurrent threshold (I_{LIM}) can be set up by R_{ILM}, whose value can be calculated by the following equation:

$$R_{LIM} = \frac{0.6}{I_{LIM} \times G_{IMON}} = \frac{0.6\ V}{8\ A \times 105.5\ \mu A/A} = 711\ \Omega$$

G_{IMON} = 105.5 µA/A and the I_{LIM} target is 8 A. Choose the closest standard resistor value of 715 Ω.

Setting the Output Voltage Rise Slew Rate

The output voltage rise slew rate and rise time are set by C_{SS}, which can be calculated using equations (?) and (?). The controller regulates the V_{OUT} to follow 10x the SS pin voltage (V_{SS}). C_{SS} can be set properly to regulate inrush current during start-up into a heavy capacitive load. Due to the high voltage drop across the switch during start-up, the power stress is higher than the steady state when the switch is fully enhanced. The proper choice of output rise time and inrush current with circuit output capacitance will avoid device overheating, which could result in thermal shutdown. It is suggested to set the inrush current below 1/20 of the current limit (I_{LIM}). For protection, the devices have foldback current limits when V_{OUT} is below VFB.

$$C_{SS} = \frac{I_{SS} \times t_{SS} \times 10}{V_{IN}} = \frac{340\ nA \times 25\ ms \times 10}{12\ V} = 7.08\ nF$$

$$I_{INRUSH} = \frac{C_{OUT} \times V_{IN}}{t_{SS}} = \frac{340\ nA \times 12\ V}{25\ ms} = 225.6\ mA$$

Choose the C_{SS} value of 6.8 nF.

Setting Overcurrent Blanking Time (tITIMER)

The overcurrent blanking time is set by the CITIMER capacitor, which can be calculated as:

$$C_{iTIMER} = \frac{I_{iTIMER} \times t_{iTIMER}}{\Delta V_{iTIMER}} = \frac{2\ \mu A \times 2\ ms}{1.55\ V} = 2.6\ nF$$

Choose the closest standard capacitor value of 2.2 nF

Application Circuit Performance

The waveforms below show the behavior of the above-mentioned design example circuit.

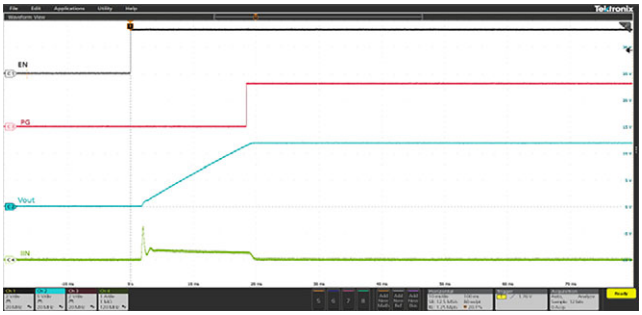


Fig. 49 - Power Start-Up With EN/UVLO

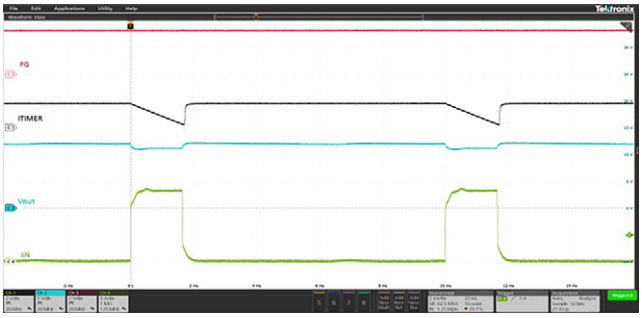


Fig. 51 - Transient Overcurrent, Overcurrent Timer Shorter Than Defined t_{ITIMER}

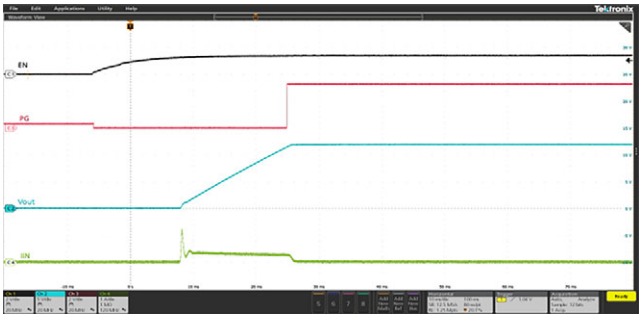


Fig. 50 - Power Start-Up With V_{IN} Ramp

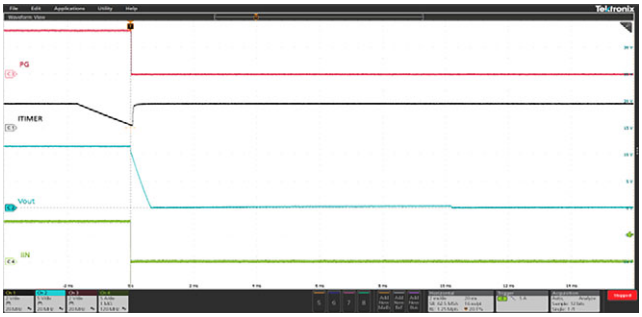


Fig. 52 - Overcurrent Circuit Breaker

Parallel Operation

Two SiP32437x devices can be paralleled for applications that require higher steady state current. The shared current between the parts can be nearly equal. The difference of sharing depends on the part to part switch resistance variation and the PCB trace resistance.

In a parallel circuit configuration, as shown in Fig. 53, the first device starts up initially to provide V_{OUT} slew rate control and V_{OUT} power good indication through P_G. The second device's EN / UVLO pin is connected to the first device's P_G and is turned on upon start-up completion of the first device. The second device's P_G indicates the status of the paralleled circuit.

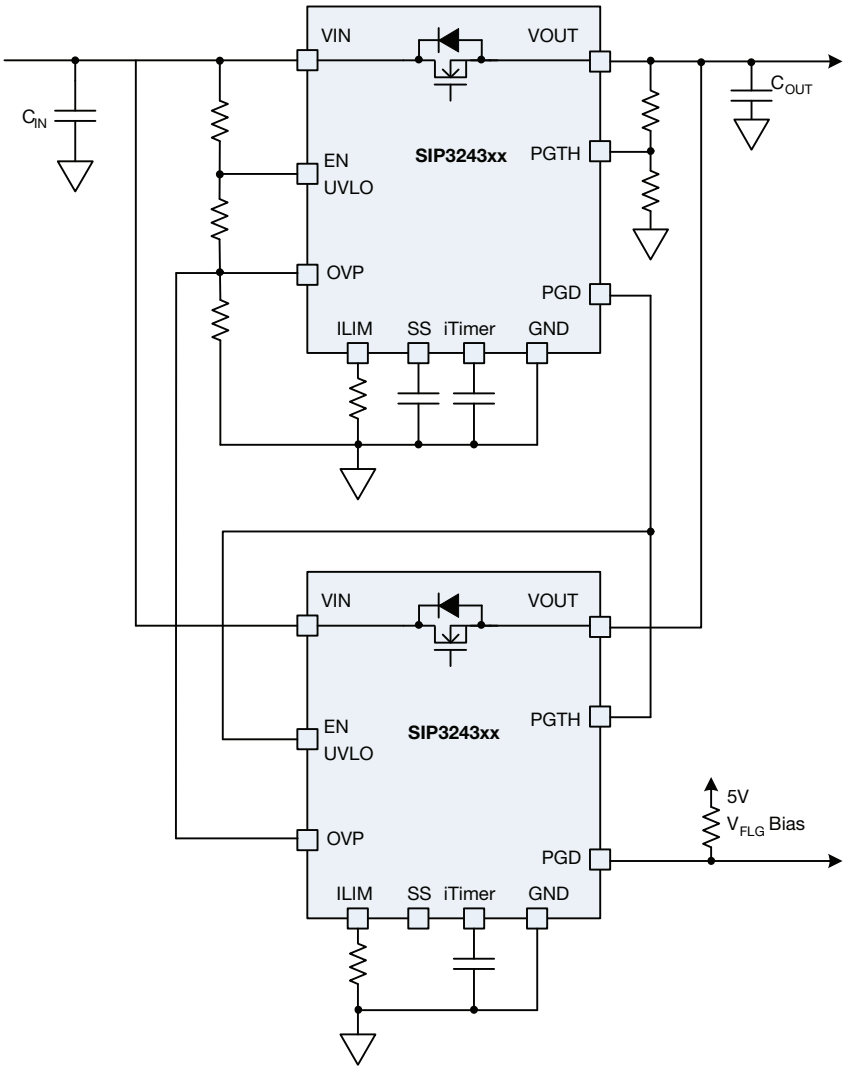


Fig. 53 - Paralleled Two-Device Circuit

Design and Layout

V_{IN}: It is recommended to put a ceramic decoupling capacitor of 0.1 µF or higher between V_{IN} and GND. For the best result, it should be closest to the IN and GND terminals.

V_{OUT}: It is recommended to put a ceramic decoupling capacitor of 1 µF or higher between V_{OUT} and GND. It should be closest to the device to minimize the loop formed by this capacitor.

GND: The GND terminal must be connected to the PCB ground plane with the shortest path. To provide a clean GND for eFuse performance, it is recommended to have a separate GND path for this chip to minimize the GND current.

PCB: The high current path must be as short as possible, and its trace design must accommodate a minimum of 2x the maximum load current.

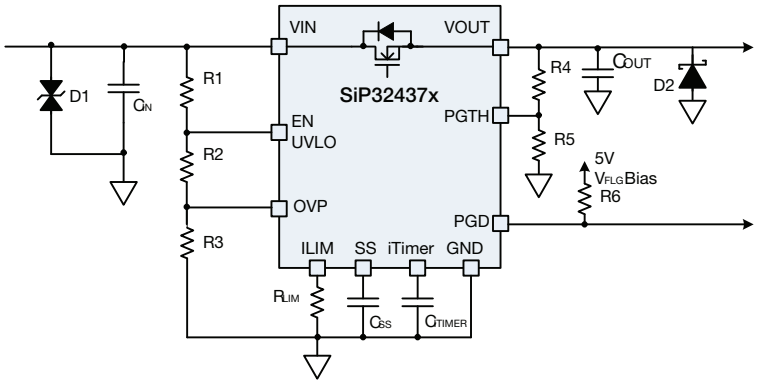


Fig. 54 - Circuit Design With Protection Devices

Thermal: the IN and OUT terminals are the two long leads that provide paths for heat dissipation. Maximize the copper area connected to these pins. The vias can also be implemented to optimize even current distribution and enhance heat dissipation.

Device setting pins: position the eFuse R and C components as close as possible to their related function setting pins with the shortest paths. The other ends of those R and C components are connected to GND. I_{LIM}, SS, and ITIMER are analog signals sensitive to noise. The traces must be short and low noise.

Transient protections: to protect the device from possible over stress during a circuit transient, various protection devices such as TVS, Schottky diodes, snubbers, and capacitors can be placed on the IN and OUT pins. They must be placed as close as possible to the device to minimize parasitic inductance on the power path.

PRODUCT SUMMARY			
Part number	SiP32435	SiP32436	SiP32437
Description	8 A, 2.7 V to 23 V, 9.2 mΩ eFuse With Transient Over Current Blanking, Adjustable OVP, and Active Current Clamping	8 A, 2.7 V to 23 V, 9.2 mΩ eFuse With Transient Over Current Blanking, Selected OVP Clamping, and Active Current Clamping	8 A, 2.7 V to 23 V, 9.2 mΩ eFuse With Transient Over Current Blanking, Adjustable OVP, and Circuit Breaker
Configuration	Single	Single	Single
Slew rate time (µs)	Adjustable	Adjustable	Adjustable
On delay time (µs)	865	655	655
Input voltage min. (V)	2.7	2.7	2.7
Input voltage max. (V)	23	23	23
On-resistance at input voltage min. (mΩ)	14	14	14
On-resistance at input voltage max. (mΩ)	9.5	9.5	9.5
Quiescent current at input voltage min. (µA)	400	400	400
Quiescent current at input voltage max. (µA)	400	400	400
Output discharge (yes / no)	No	No	No
Reverse blocking (yes / no)	No	No	No
Continuous current (A)	8	8	8
Package type	TDFN10-22	TDFN10-22	TDFN10-22
Package size (W, L, H) (mm)	2.0 x 2.0 x 0.75	2.0 x 2.0 x 0.75	2.0 x 2.0 x 0.75
Status code			
Product type	Slew rate, current limit	Slew rate, current limit	Slew rate, current limit
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

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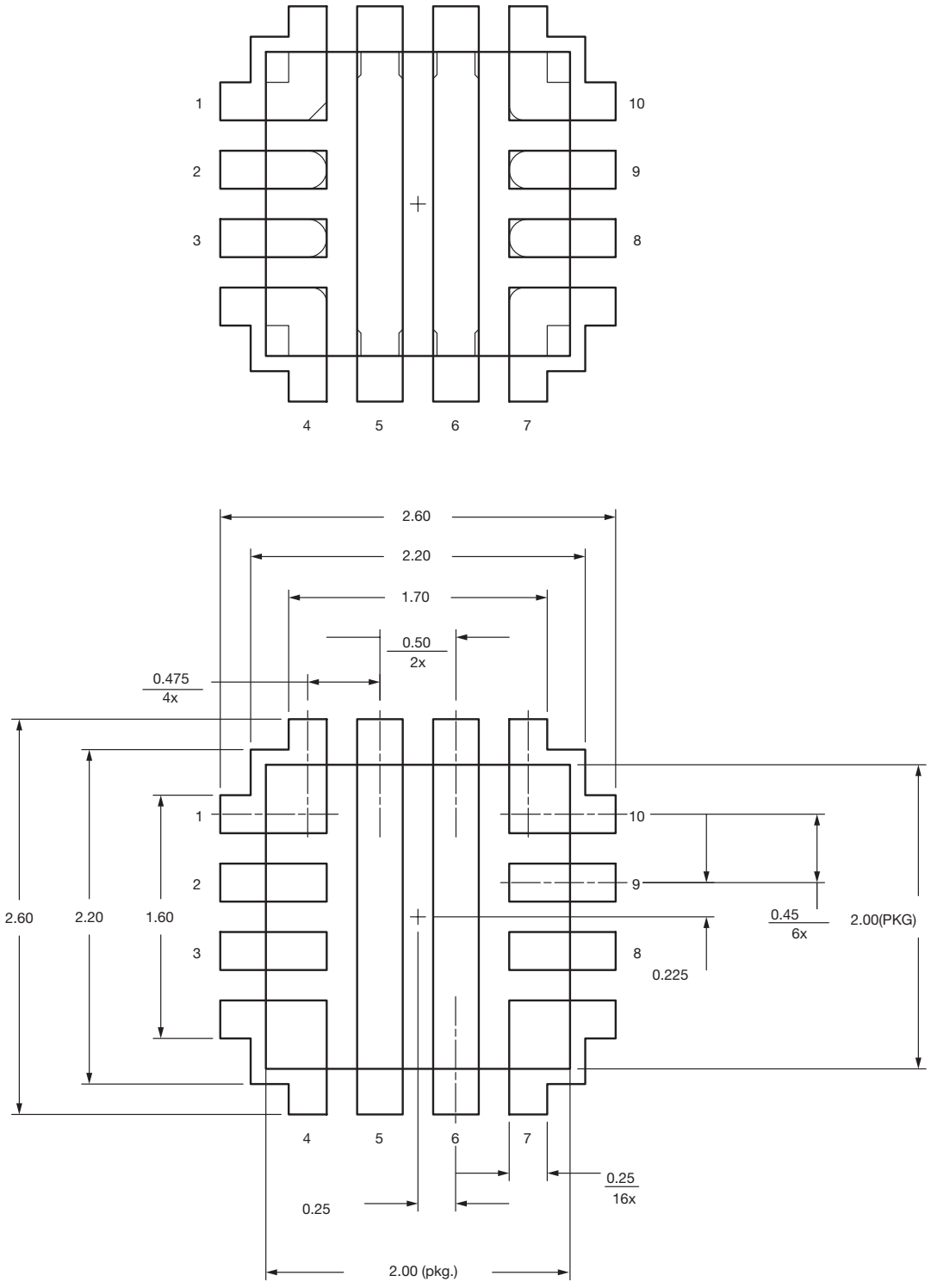
Recommended Land Pattern TDFN10-22



ECN: E24-0247-Rev. A, 26-Aug-2024
DWG: 3029

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