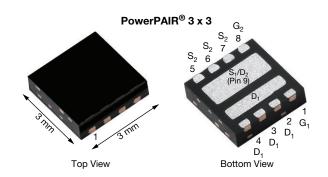


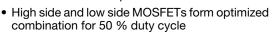
Dual N-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	30				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0092				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0155				
Q _g typ. (nC)	3.7				
I _D (A)	33.6 ^a				
Configuration	Dual				

FEATURES







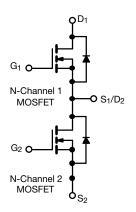
 • Optimized R_{DS} - Q_g and R_{DS} - Q_{gd} FOM elevates efficiency for high frequency switching

HALOGEN FREE

- 100 % R_a and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Synchronous buck
- DC/DC conversion
- Half bridge
- POL



ORDERING INFORMATION	
Package	PowerPAIR 3 x 3
Lead (Pb)-free and halogen-free	SiZ342DDT-T1-GE3

PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	30		
Gate-source voltage		V _{GS}	+20 / -16		
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		33.6		
	T _C = 70 °C		26.9		
	T _A = 25 °C	I _D	15.8 ^{b, c}		
	T _A = 70 °C		12.6 ^{b, c}		
Pulsed drain current (t = 100 µs)		I _{DM}	100	A	
Continuous source current (MOSFET diode conduction)	T _C = 25 °C		13.9		
	T _A = 25 °C	I _S	3.1 b, c		
Single pulse avalanche current	1 0111	I _{AS}	10		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	5	mJ	
Maximum power dissipation	T _C = 25 °C		16.7		
	T _C = 70 °C	5	10.7	\	
	T _A = 25 °C	P _D	3.7 b, c	W	
	T _A = 70 °C		2.4 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		
Soldering recommendations (peak temperature)			260	°C	

Notes

a. $T_C = 25$ °C

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s



Vishay Siliconix

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient a, b	t ≤ 10 s	R_{thJA}	27	34	°C/W	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	6	7.5	G/ VV	

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 69 °C/W

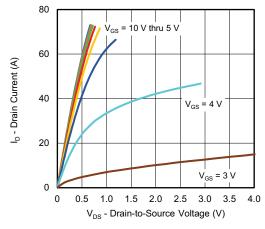
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	-	v	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.1	-	2.4		
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20 \text{ V} / -16 \text{ V}$	-	-	± 100	nA	
Zava mata valtama duain avument	_	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ	
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	-	-	5		
Drain actives on state resistance a	В	V _{GS} = 10 V, I _D = 10 A	=	0.0075	0.0092	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$	-	0.012	0.0155		
Forward transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 10 A	-	23	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	500	-	pF	
Output capacitance	C _{oss}	, , , , , , , , , , , , , , , , , , ,	-	230	-		
Reverse transfer capacitance	C _{rss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	30	-		
C _{rss} /C _{iss} ratio			-	0.062	0.12		
Tatal sate aboves		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 15 A	-	8.4	12.6	nC	
Total gate charge	Q_g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 15 A	-	4	6		
Gate-source charge	Q_{gs}		-	2.2	-		
Gate-drain charge	Q _{gd}		-	1.0	-		
Gate resistance	Rg	f = 1 MHz	0.2	1.2	2	Ω	
Turn-on delay time	t _{d(on)}		-	10	20	-	
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_{I} = 1.5 \Omega, I_{D} \cong 10 \text{ A},$	-	20	40		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	13	25		
Fall time	t _f		-	5	10		
Turn-on delay time	t _{d(on)}		-	12	25	ns	
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_{I} = 1.5 \Omega, I_{D} \cong 10 \text{ A},$	-	100	200	- - -	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	10	20		
Fall time	t _f		-	10	20		
Drain-source Body Diode Characterist	cs			•			
Continuous source-drain diode current	I _S	T _C = 25°C	-	-	13.9	۸	
Pulse diode forward current	I _{SM}	-	-	100	Α		
Body diode voltage	V_{SD}	$I_S = 8 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.83	1.2	V	
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	15	30	ns	
Body diode reverse recovery charge	Q _{rr}		-	4	10	nC	
Reverse recovery fall time	t _a		-	7.5	-		
Reverse recovery rise time	t _b		-	7.5	_	ns	

Notes

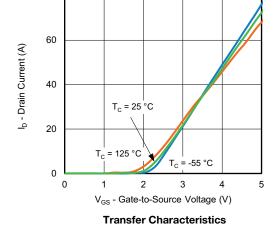
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

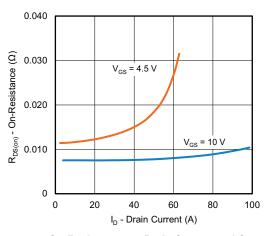




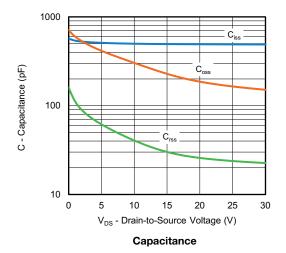
Output Characteristics

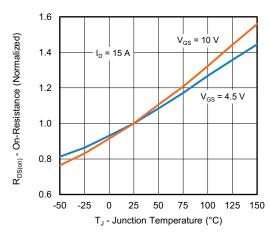


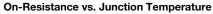
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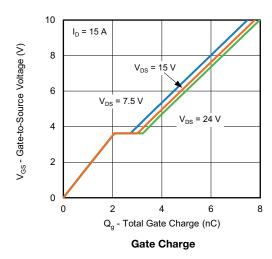


On-Resistance vs. Drain Current and Gate

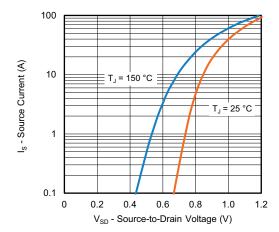




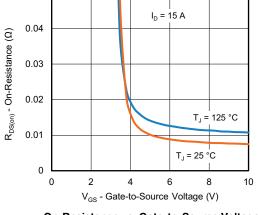






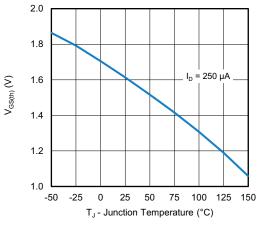


Source-Drain Diode Forward Voltage

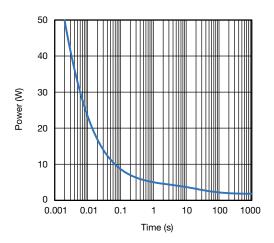


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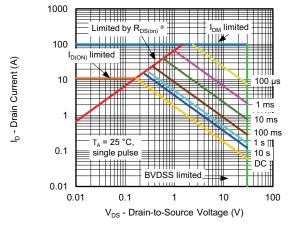
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



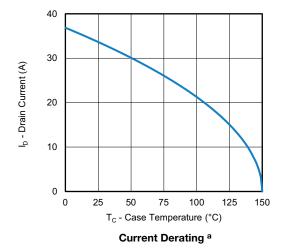
Single Pulse Power



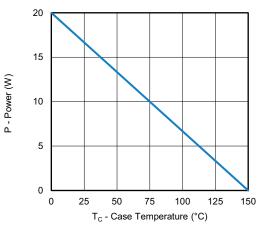
Safe Operating Area, Junction-to-Ambient

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



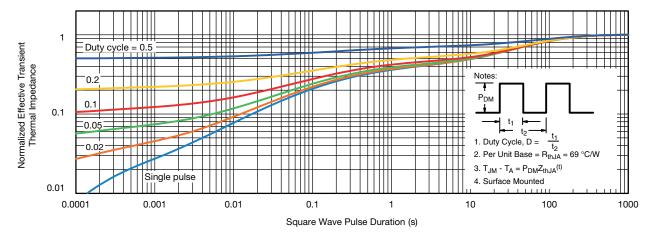
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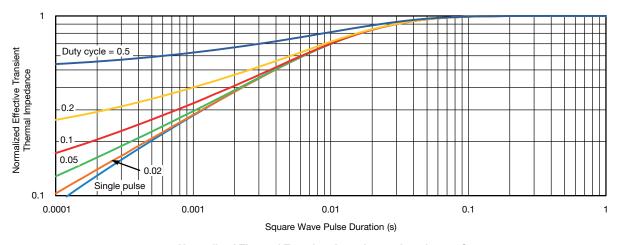
Power, Junction-to-Case

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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