# High Speed Quad SPST CMOS Analog Switch

## DESCRIPTION

The DG201HS is an improved monolithic device containing four independent analog switches. It is designed to provide high speed, low error switching of analog signals. Combining low on-resistance (25 Ω) with high speed ($t_{on}$: 38 ns), the DG201HS is ideally suited for high speed data acquisition requirements.

To achieve high voltage ratings and superior switching performance, the DG201HS is built on a proprietary high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply values, when off.

## BENEFITS

- Faster throughput
- Higher accuracy
- Reduced pedestal error
- Upgrades existing designs
- Simple interfacing
- Replaces HI201HS, ADG201HS
- Space savings (TSSOP)

## FEATURES

Pb-free Available

RoHS* Available

- Fast switching-$t_{on}$: 38 ns
- Low on-resistance: 25 Ω
- Low leakage: 100 pA
- Low charge injection
- TTL/CMOS logic compatible
- Single supply compatibility
- High current rating: -30 mA
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

**Note**

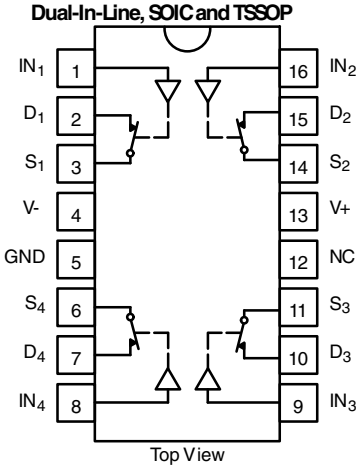
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## APPLICATIONS

- Data acquisition
- Hi-Rel systems
- Sample and hold circuits
- Communication systems
- Automatic test equipment
- Integrator reset circuits
- Choppers
- Gain switching
- Avionics

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line, SOIC and TSSOP




Top View

| TRUTH TABLE | |
|---|---|
| **LOGIC** | **SWITCH** |
| 0 | On |
| 1 | Off |

**Note**

- Logic “0” ≤ 0.8 V; logic “1” ≥ 2.4 V

| ORDERING INFORMATION | | |
|---|---|---|
| **TEMP. RANGE** | **PACKAGE** | **PART NUMBER** |
| -40 °C to +85 °C | 16-pin narrow SOIC | DG201HSDY-E3<br>DG201HSDY-T1-E3 |
| | 16-pin TSSOP | DG201HSDQ-E3<br>DG201HSDQ-T1-E3 |
| | 16-pin plastic DIP | DG201HSDJ-E3 |

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|---|---|
| **PARAMETER** | | **LIMIT** | **UNIT** |
| Voltages referenced, V+ to V- | | 44 | V |
| GND | | 25 | |
| Digital inputs [a], $V_S$, $V_D$ | | (V-) - 4 to (V+) + 4<br>or 30 mA, whichever occurs first | |
| Current (any terminal) | | 30 | mA |
| Peak current S or D (pulsed at 1 ms, 10 % duty cycle max.) | | 100 | |
| Storage temperature | (A suffix) | -65 to +150 | °C |
| | (D suffix) | -65 to +125 | |
| Power dissipation (package) [b] | 16-pin plastic DIP [c] | 470 | mW |
| | 16-pin narrow body SOIC and TSSOP [e] | 600 | |

**Notes**

a. Signals on $S_X$, $D_X$, or $IN_X$ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 6 mW/°C above 75 °C
d. Derate 12 mW/°C above 75 °C
e. Derate 7.6 mW/°C above 75 °C

## SCHEMATIC DIAGRAM (typical channel)

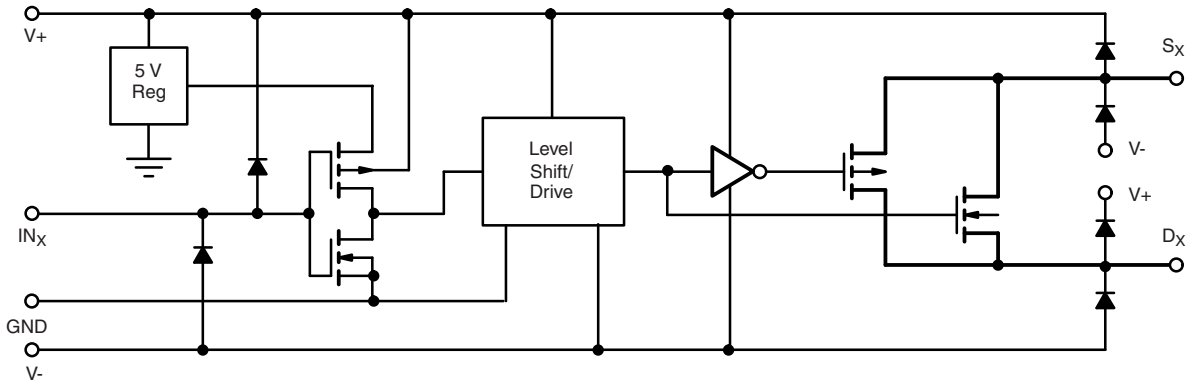



**Fig. 1**

## SPECIFICATIONS [a]

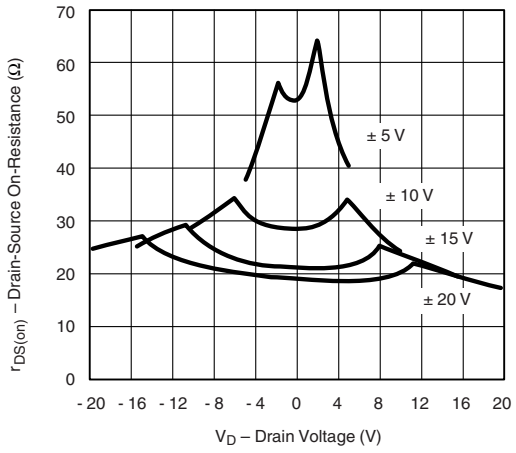
| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS SPECIFIED V+ = 15 V, V- = -15 V $V_{IN}$ = 3 V, 0.8 V [f] | TEMP. [b] | TYP. [c] | A SUFFIX -55 °C to +125 °C | | D SUFFIX -40 °C to +85 °C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. [d] | MAX. [d] | MIN. [d] | MAX. [d] | |
| **Analog Switch** | | | | | | | | | |
| Analog signal range [e] | $V_{ANALOG}$ | | Full | - | V- | V+ | V- | V+ | V |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_D$ = ± 10 V, $I_S$ = 1 mA | Room | 25 | - | 50 | - | 50 | Ω |
| | | | Full | - | - | 75 | - | 75 | |
| $R_{DS(on)}$ match | $\Delta R_{DS(on)}$ | | Room | 3 | - | - | - | - | % |
| Source off leakage current | $I_{S(off)}$ | V+ = 16.5 V, V- = -16.5 V, $V_D$ = ± 15.5 V, $V_S$ = ± 15.5 V | Room | 0.1 | -1 | 1 | -1 | 1 | nA |
| | | | Full | - | -60 | 60 | -20 | 20 | |
| Drain off leakage current | $I_{D(off)}$ | | Room | 0.1 | -1 | 1 | -1 | 1 | |
| | | | Full | - | -60 | 60 | -20 | 20 | |
| Drain on leakage current | $I_{D(on)}$ | V+ = 16.5 V, V- = -16.5 V, $V_S$ = $V_D$ = ± 15.5 V | Room | 0.1 | -1 | 1 | -1 | 1 | |
| | | | Full | - | -60 | 60 | -20 | 20 | |
| **Digital Control** | | | | | | | | | |
| Input voltage high | $V_{INH}$ | | Full | - | 2.4 | - | 2.4 | - | V |
| Input voltage low | $V_{INL}$ | | Full | - | - | 0.8 | - | 0.8 | |
| Input current | $I_{INH}$ or $I_{INL}$ | $V_{IN}$ under test = 0.8 V, 3 V | Full | - | -1 | 1 | -1 | 1 | µA |
| Input capacitance | $C_{IN}$ | | Full | 5 | - | - | - | - | pF |
| **Dynamic Characteristics** | | | | | | | | | |
| Turn-on time | $t_{on}$ | $R_L$ = 1 kΩ, $C_L$ = 35 pF, $V_S$ = ± 10 V, $V_{INH}$ = 3 V, see Fig. 2 | Room | 48 | - | 60 | - | 60 | ns |
| | | | Full | - | - | 75 | - | 75 | |
| Turn-off time | $t_{off1}$ | | Room | 30 | - | 50 | - | 50 | |
| | | | Full | - | - | 70 | - | 70 | |
| | $t_{off2}$ | | Room | 150 | - | - | - | - | |
| Output setting time to 0.1 % | $t_S$ | | Room | 180 | - | - | - | - | |
| Charge injection | Q | $C_L$ = 1 nF, $V_S$ = 0 V, $V_{GEN}$ = 0 V, $R_{gen}$ = 0 Ω | Room | -5 | - | - | - | - | pC |
| Source-off capacitance | $C_{S(off)}$ | $V_S$ = $V_D$ = 0 V, f = 1 MHz | Room | 8 | - | - | - | - | pF |
| Drain-off capacitance | $C_{D(off)}$ | | Room | 8 | - | - | - | - | |
| Channel on capacitance | $C_{D(on)}$ | | Room | 30 | - | - | - | - | |
| Drain to source capacitance | $C_{DS(off)}$ | | Room | 0.5 | - | - | - | - | |
| Off isolation | OIRR | $C_L$ = 10 pF, $R_L$ = 1 kΩ, f = 100 kHz | Room | 85 | - | - | - | - | dB |
| Channel-to-channel crosstalk | $X_{TALK}$ | Any other channel switches, $C_L$ = 10 pF, $R_L$ = 1 kΩ, f = 100 kHz | Room | 100 | - | - | - | - | |
| **Power Supply** | | | | | | | | | |
| Positive supply current | I+ | V+ = 15 V, V- = -15 V, $V_{IN}$ = 0 V or 5 V | Room | 4.5 | - | - | - | - | mA |
| | | | Full | - | - | 10 | - | 10 | |
| Negative supply current | I- | | Room | 3.5 | - | - | - | - | |
| | | | Full | - | -6 | - | -6 | - | |
| Power consumption [c] | $P_C$ | | Full | - | - | 240 | - | 240 | mW |

**Notes**

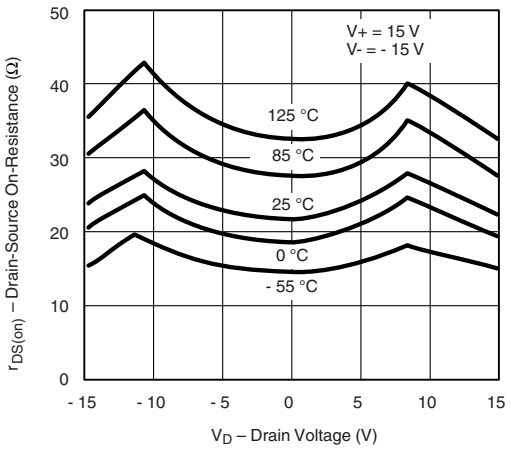
a. Refer to “Process Option Flowchart”
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for “Design Aid Only”, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. $V_{IN}$ = input voltage to perform proper function

*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

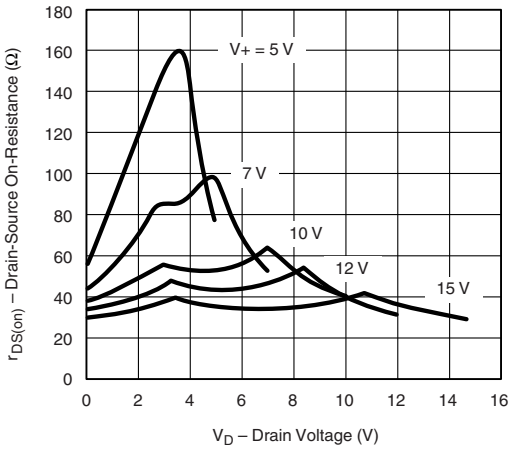
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



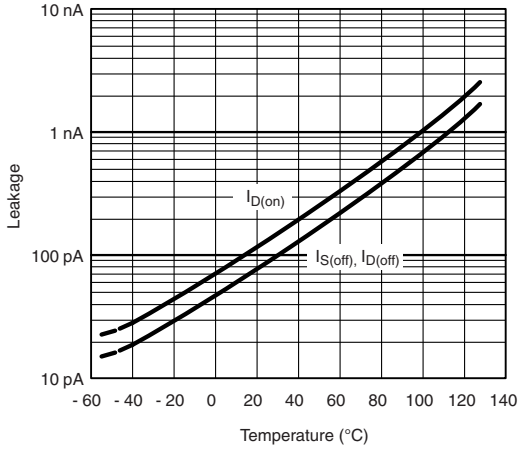

**$R_{DS(on)}$ vs. $V_D$ and Power Supply Voltages**



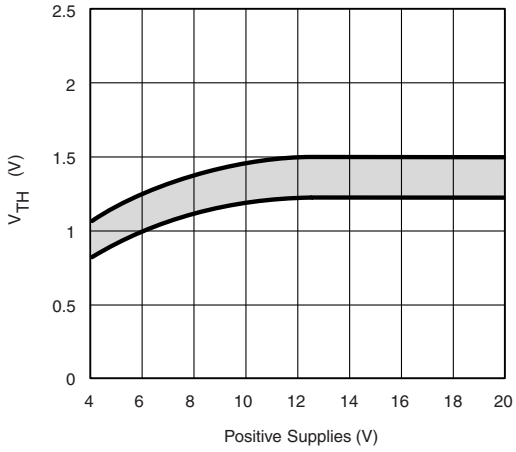

**$R_{DS(on)}$ vs. $V_D$ and Temperature**



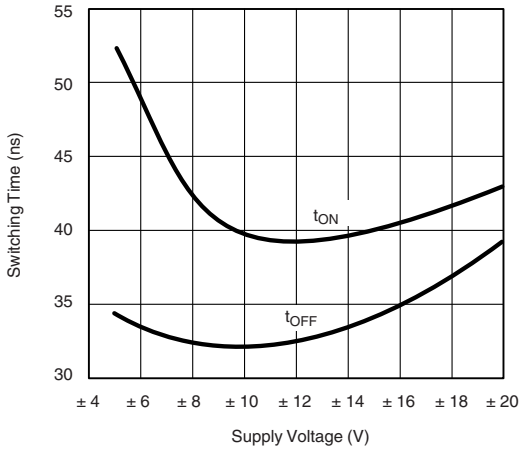

**$R_{DS(on)}$ vs. $V_D$ and Single Power Supply Voltages**




**Leakage Currents vs. Temperature**

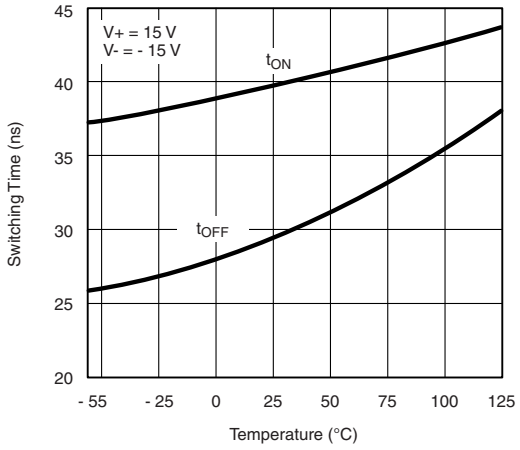



**Input Switching Threshold vs. Supply Voltage**

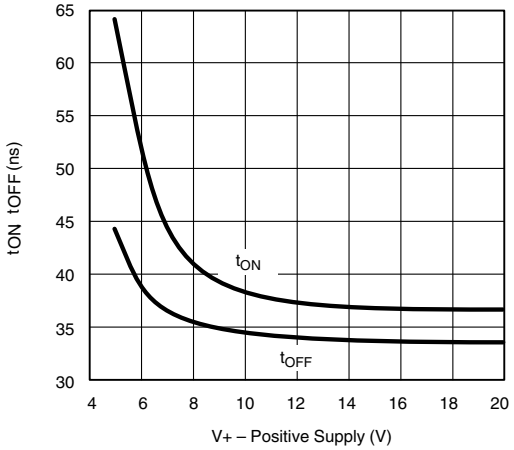



**Switching Time vs. Power Supply Voltage**

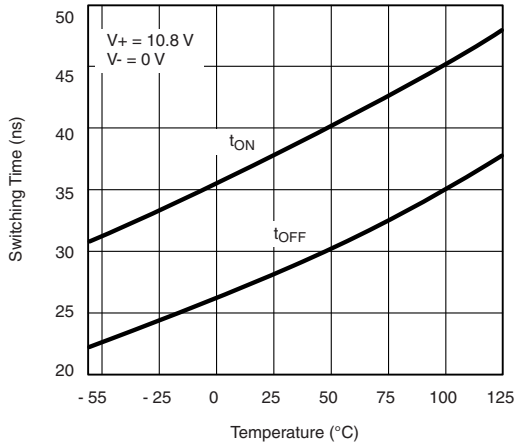
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



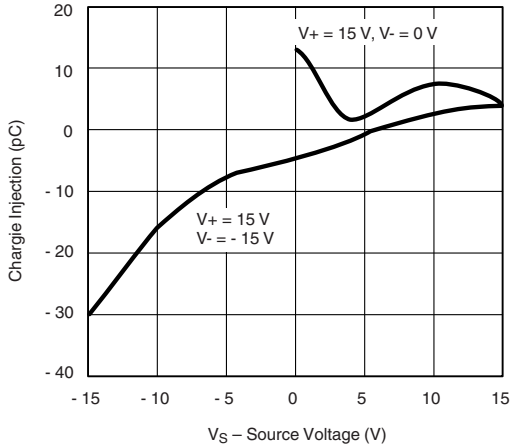

**Switching Times vs. Temperature**



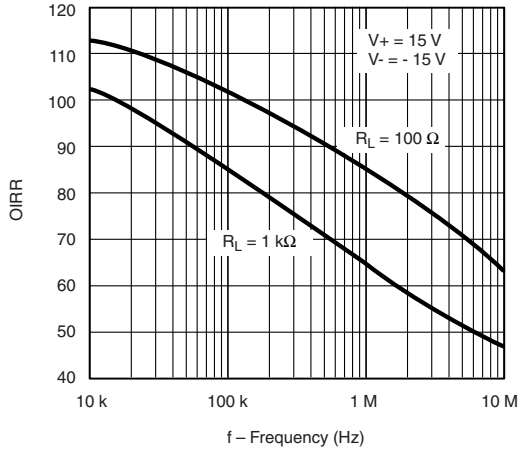

**Switching Times vs. Temperature**




**Switching Times vs. Temperature**




**Charge Injection vs. Source Voltage**




**Off Isolation vs. Frequency**

## TEST CIRCUITS

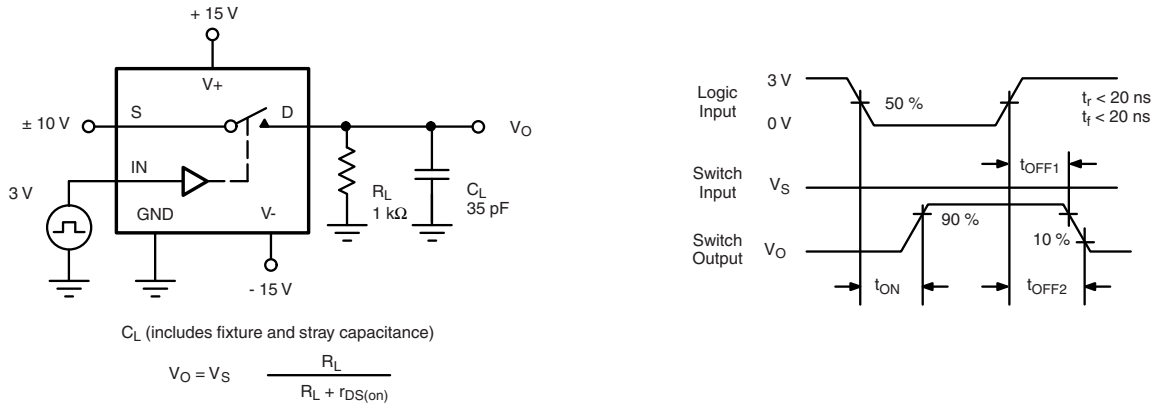



**Fig. 2 - Switching Time**


**Fig. 3 - Charge Injection**

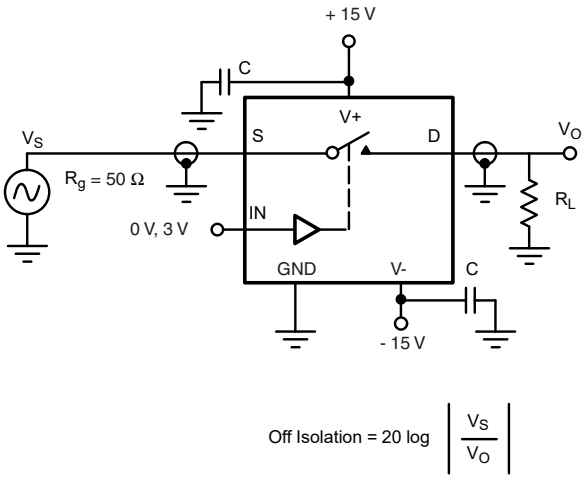



**Fig. 4 - Off Isolation**

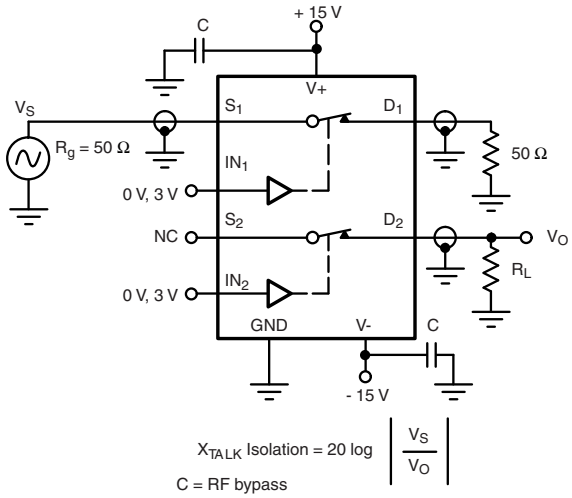
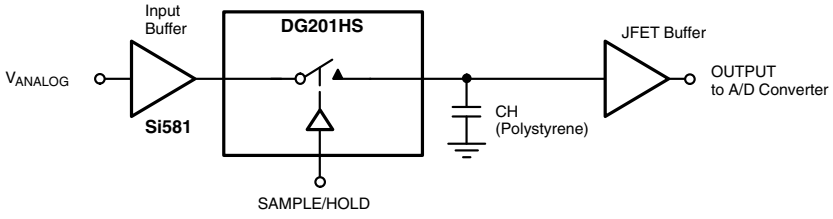



**Fig. 5 - Crosstalk**

## APPLICATIONS

A high-speed, low-glitch analog switch such as Vishay Siliconix's DG201HS improves the accuracy and shortens the acquisition and settling times of a sample-and-hold circuit.



| PRODUCT SUMMARY | | | |
|---|---|---|---|
| Part number | DG201HS | DG201HS | DG201HS |
| Status code | 2 | 2 | 2 |
| Configuration | SPST x 4, NC | SPST x 4, NC | SPST x 4, NC |
| Single supply min. (V) | 5 | 5 | 5 |
| Single supply max. (V) | 36 | 36 | 36 |
| Dual supply min. (V) | 5 | 5 | 5 |
| Dual supply max. (V) | 22 | 22 | 22 |
| On-resistance (Ω) | 25 | 25 | 25 |
| Charge injection (pC) | -5 | -5 | -5 |
| Source on capacitance (pF) | - | - | - |
| Source off capacitance (pF) | 8 | 8 | 8 |
| Leakage switch on typ. (nA) | 0.1 | 0.1 | 0.1 |
| Leakage switch off max. (nA) | 1 | 1 | 1 |
| -3 dB bandwidth (MHz) | - | - | - |
| Package | TSSOP-16 | SO-16 (narrow) AS | Plastic DIP-16 |
| Functional circuit / applications | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare |
| Interface | Parallel | Parallel | Parallel |
| Single supply operation | Yes | Yes | Yes |
| Dual supply operation | Yes | Yes | Yes |
| Turn on time max. (ns) | 50 | 50 | 50 |
| Crosstalk and off isolation | -85 | -85 | -85 |

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