DG213



Quad Complementary CMOS Analog Switch

FEATURES

• ± 22 V supply voltage rating

Low leakage - I_{D(on)}: 20 pA

Extended temperature range

Low charge injection - Q: 1 pC

please see www.vishay.com/doc?99912

• Fast switching - ton: 85 ns

Industrial instrumentation

Communications systems

Computer peripherals

Portable instruments

· Sample-and-hold circuits

APPLICATIONS

Test equipment

Disk drives

TTL and CMOS compatible logic

Low on-resistance - R_{DS(on)}: 45 Ω

Single supply operation possible

DESCRIPTION

The versatile DG213 analog switch has two NC and two NO switches. It can be used in various configurations, including four single-pole single-throw (SPST), two single-pole double-throw (SPDT), one "T" switch, one DPDT, etc. This device is fabricated in a Vishay Siliconix' proprietary high-voltage silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

This analog switch was designed for a wide variety of general purpose applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. These switches can handle up to \pm 22 V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All switches feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

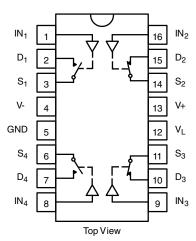
For additional information, please refer to Application Note AN208 (<u>www.vishay.com/doc?70606</u>).

BENEFITS

- Wide analog signal range
- Simple logic interface
- Higher accuracy
- Minimum transients
- Reduced power consumption
- Low cost

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG213 Dual-In-Line. SOIC and TSSOP



TRUTH TABLE						
LOGIC	SW1, SW4	SW2, SW3				
0	Off	On				
1	On	Off				

· Material categorization: for definitions of compliance

Note

 Logic "0" ≤ 0.8 V Logic "1" ≥ 2.4 V







ORDERING INFORMATION				
TEMP. RANGE	PACKAGE	PART NUMBER		
-40 °C to +85 °C	16-pin narrow SOIC	DG213DY-E3 DG213DY-T1-E3		
	16-pin TSSOP	DG213DQ-E3 DG213DQ-T1-E3		
	16-pin plastic DIP	DG213DJ-E3		

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)					
PARAMETER		LIMIT	UNIT		
Voltages referenced, V+ to V-		44			
GND		25	v		
Digital inputs ^a , V _S , V _D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first			
Current (any terminal)		30			
Peak current, S or D (pulsed at 1 m	ns, 10 % duty cycle max.)	100	mA		
Storage temperature		-65 to +125	°C		
	16 pin plastic DIP ^c	470			
Power dissipation (package) ^b	16 pin narrow SOIC ^d	640	mW		
	16 pin narrow TSSOP ^d	500			

Notes

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings

b. All leads welded or soldered to PC board

c. Derate 6.5 mW/°C above 75 °C

d. Derate 7.6 mW/°C above 75 °C

SCHEMATIC DIAGRAM (typical channel)

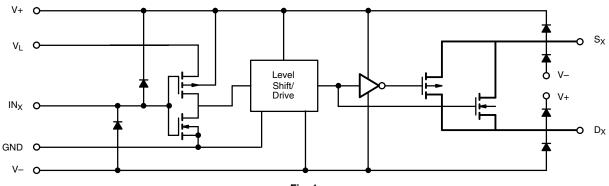


Fig. 1



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DG213

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SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP. ^a	D SUFFIX -40 °C to +85 °C			UNIT
	STWIDOL	V+ = 15 V, V- = -15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V $^{\rm e}$		MIN. °	TYP. ^b	MAX. c	onn
Analog Switch							
Analog signal range ^d	VANALOG		Full	V-	-	V+	V
Drain-source on-resistance	R _{DS(on)}		Room	-	45	60	
	US(on)	$V_{D} = \pm 10 \text{ V}, \text{ I}_{S} = 1 \text{ mA}$	Full	-	-	85	Ω
R _{DS(on)} match	$\Delta R_{DS(on)}$		Room	-	1	2	
Source off leakage current	I _{S(off)}	$V_{S} = \pm 14 \text{ V}, V_{D} = \pm 14 \text{ V}$	Room	-0.5	± 0.01	0.5	
	[•] S(оп)		Full	-5	-	5	
Drain off leakage current	I _{D(off)}	$V_{D} = \pm 14 \text{ V}, \text{ V}_{S} = \pm 14 \text{ V}$	Room	-0.5	± 0.01	0.5	nA
	·D(011)	$v_D = \pm 1 + v, v_S = \pm 1 + v$	Full	-5	-	5	10 (
Drain on leakage current	I _{D(on)}	$V_{S} = V_{D} = \pm 14 V$	Room	-0.5	± 0.02	0.5	
<u> </u>	יD(on)	vs = vD = ± 1+ v	Full	-10	-	10	
Digital Control							
Input voltage high	V _{INH}		Full	2.4	-	-	V
Input voltage low	V _{INL}		Full	-	-	0.8	v
Input current	$I_{\rm INH}$ or $I_{\rm INL}$	V _{INH} or V _{INL}	Full	-1	-	1	μA
Input capacitance	C _{IN}		Room	-	5	-	pF
Dynamic Characteristics							
Turn-on time	t _{on}	V _S = 10 V, see Fig. 9	Room	-	85	130	
Turn-off time	t _{off}		Room	-	55	100	ns
Turn-off time	t _D	$V_S = 10 V$, see Fig. 10	Room	15	25	-	
Charge injection	Q	C_{L} = 1000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-	1	-	рС
Source-off capacitance	C _{S(off)}	$V_{S} = 0 V, f = 1 MHz$	Room	-	5	-	
Drain-off capacitance	C _{D(off)}	vs = 0 v, 1 = 1 10112	Room	-	5	-	pF
Channel-on capacitance	C _{D(on)}	$V_D = V_S = 0 V$, f = 1 MHz	Room	-	16	-	
Off isolation	O _{IRR}	$C_{L} = 15 \text{ pF}, \text{ R}_{L} = 50 \Omega,$	Room	-	90	-	dB
Channel to channel crosstalk	X _{TALK}	$V_{\rm S}$ = 1 $V_{\rm RMS}$, f = 100 kHz	Room	-	95	-	чъ
Power Supply							
Positive supply current	l+		Room	-	-	1	
Negative supply current		$V_{IN} = 0 V \text{ or } 5 V$	Full	-	-	5	μA
	-		Room	-1	-	-	
			Full	-5	-	-	
Logic supply current	١L		Room	-	-	1	
Logio oupply outfold	۲ <u>ـ</u>		Full	-	-	5	
Power supply range for continuous operation	V _{OP}		Full	± 3	-	± 22	V

Notes

a. Room = 25 °C, full = as determined by the operating temperature suffix

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet

d. Guaranteed by design, not subject to production test

e. V_{IN} = input voltage to perform proper function



SPECIFICATIONS (for Single Supply)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP. ^a	D SUFFIX -40 °C to +85 °C			UNIT
		V+ = 12 V, V- = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V $^{\rm e}$		MIN. °	TYP. ^b	MAX. °	
Analog Switch							
Analog signal range ^d	V _{ANALOG}		Full	V-	-	V+	V
Drain-source on-resistance	P	$V_{\rm D} = 3 \text{ V}, \text{ I}_{\rm S} = 1 \text{ mA}$	Room	-	90	110	Ω
Drain-source on-resistance	R _{DS(on)}	$v_D = 3 v, i_S = 1 \text{ IIIA}$	Full	-	-	140	52
Dynamic Characteristics							
Turn-on time	t _{on}	See Fig. 9	Room	-	125	200	
Turn-off time	t _{off}	See Fig. 9	Room	-	45	100	ns
Break-before-make time delay	t _D	$V_S = 8 V$, see Fig. 10	Room	50	80	-	
Charge injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	-	4	-	рС
Power Supply							
Positive supply current	I+	$V_{IN} = 0 V \text{ or } 5 V$	Room	-	-	1	
Fositive supply current			Full	-	-	5	
Negative supply surrent	I-		Room	-1	-	-	
Negative supply current			Full	-5	-	-	μA
			Room	-	-	1	
Logic supply current	١L		Full	-	-	5	
Power supply range for continuous operation	V _{OP}		Full	+ 3	-	+ 40	V

Notes

a. Room = 25 °C, full = as determined by the operating temperature suffix

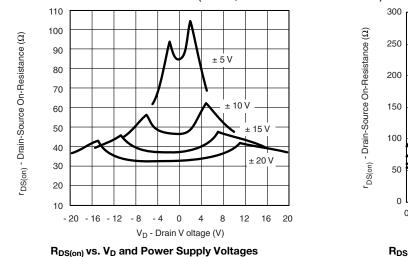
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing

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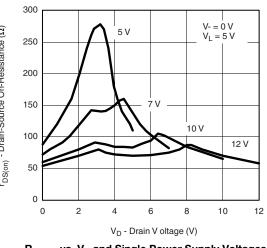
d. Guaranteed by design, not subject to production test

e. V_{IN} = input voltage to perform proper function

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.







R_{DS(on)} vs. V_D and Single Power Supply Voltages

E24-0428-Rev. A, 02-Sep-2024

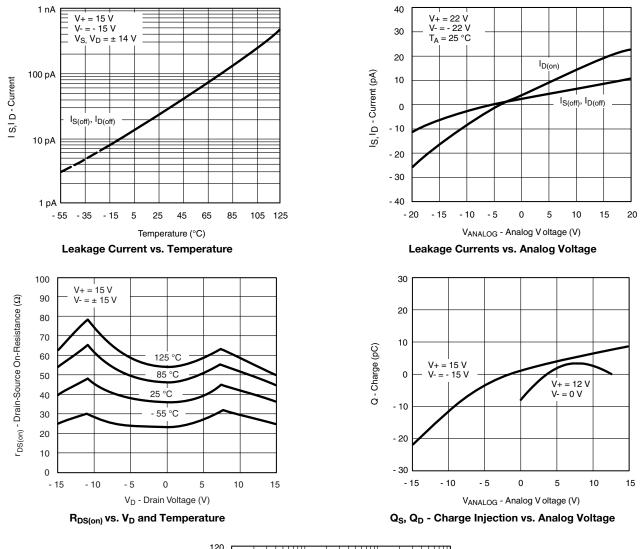
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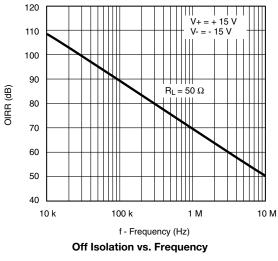
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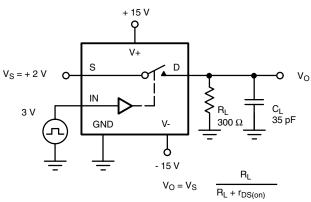
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



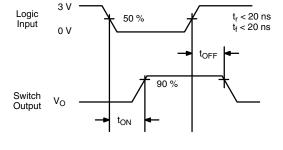


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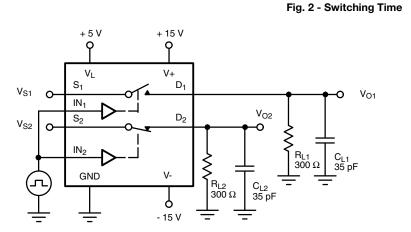
TEST CIRCUITS



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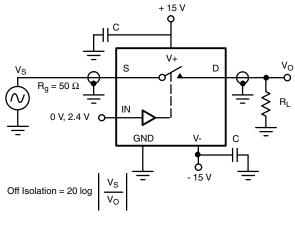
Logic Input



3 V 50 % 0 V V_{S1} V_{O1} 90 % Switch 0 V Output V_{S2} V₀₂ 90 % 0 V Switch t_D Output







+ 15 V С 0 V+ S. D1 $R_{g} = 50$ 50 IN₁ 0 V, 2.4 V C D_2 ٧o S_2 NC O റ IN_2 0 V, 2.4 V O GND V-С C = RF bypass ٧s P X_{TALK} Isolation = 20 log vo - 15 V

Fig. 5 - Channel-to-Channel Crosstalk

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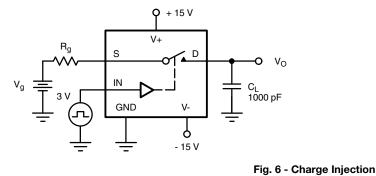
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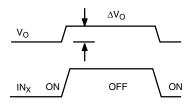
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TEST CIRCUITS





 ΔV_O = measured voltage error due to charge injection The charge injection in coulombs is Q = C_L x ΔV_O

APPLICATIONS

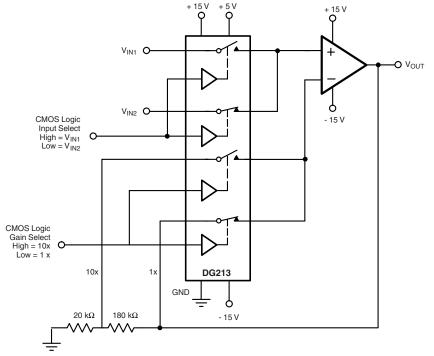


Fig. 7 - Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain



PRODUCT SUMMARY			
Part number	DG213	DG213	DG213
Status code	2	2	2
Configuration	SPST x 4, comp	SPST x 4, comp	SPST x 4, comp
Single supply min. (V)	5	5	5
Single supply max. (V)	36	36	36
Dual supply min. (V)	5	5	5
Dual supply max. (V)	22	22	22
On-resistance (Ω)	45	45	45
Charge injection (pC)	1	1	1
Source on capacitance (pF)	-	-	-
Source off capacitance (pF)	5	5	5
Leakage switch on typ. (nA)	0.02	0.02	0.02
Leakage switch off max. (nA)	0.5	0.5	0.5
-3 dB bandwidth (MHz)	-	-	-
Package	TSSOP-16	SO-16 (narrow) AS	Plastic DIP-16
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes
Turn on time max. (ns)	130	130	130
Crosstalk and off isolation	-90	-90	-90

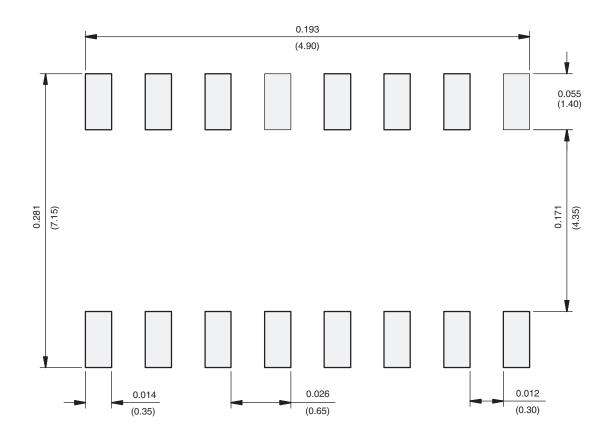
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PAD Pattern

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RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads Dimensions in inches (mm)

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads Dimensions in Inches/(mm)

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Revision: 01-Jan-2025