Low-Power, High Speed CMOS Analog Switches

DESCRIPTION

The DG401, DG403, DG405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35 µW, typ.) with high speed (t_{ON}: 75 ns, typ.), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Vishay Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ± 15 V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

FEATURES

- 44 V supply max. rating
- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 30 W
- Low leakage - $I_{D(on)}$: 40 pA
- Fast switching - t_{ON}: 75 ns
- Ultra low power requirements - P_D: 0.35 µW
- TTL, CMOS compatible
- Single supply capability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS*
Available

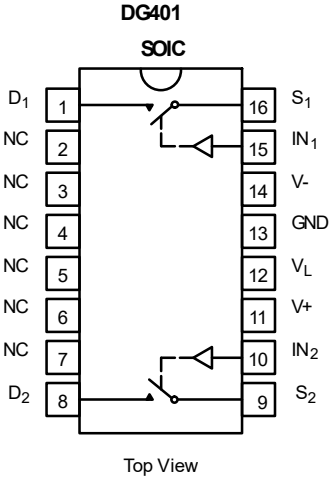
BENEFITS

- Wide dynamic range
- Break-before-make switching action
- Simple interfacing

APPLICATIONS

- Audio and video switching
- Sample-and-hold circuits
- Battery operation
- Test equipment
- Communications systems
- PBX, PABX

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

Two SPST switches per package

TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

Note

- Pb containing terminations are not RoHS compliant, exemptions may apply

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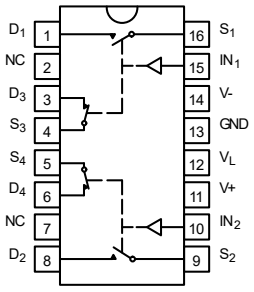
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG403
SOIC



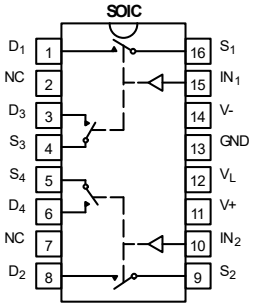
Top View

Two SPDT Switches per Package

TRUTH TABLE		
LOGIC	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

DG405
SOIC



Top View

Two SPDT Switches per Package

TRUTH TABLE	
LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
DG401		
- 40 °C to 85 °C	16-Pin Narrow SOIC	DG401DY-E3 DG401DY-T1-E3
DG403		
- 40 °C to 85 °C	16-Pin Narrow SOIC	DG403DY-E3 DG403DY-T1-E3
DG405		
- 40 °C to 85 °C	16-Pin Narrow SOIC	DG405DY-E3 DG405DY-T1-E3

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
V+ to V-		44	V
GND to V-		25	
VL		(GND - 0.3) to (V+) + 0.3	
Digital inputs [a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current (any terminal) continuous		30	mA
Current, S or D (pulsed 1 ms, 10 % Duty)		100	
Storage temperature	(DY Suffix)	-65 to +125	°C
Power dissipation (package) [b]	16-Pin SOIC [d]	600	mW

Note

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 6 mW/°C above 75 °C
d. Derate 7.6 mW/°C above 75 °C

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SPECIFICATIONS [a]

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [f]	TEMP.[b]	TYP. [c]	D SUFFIX - 40 °C TO 85 °C MIN. [d]	D SUFFIX - 40 °C TO 85 °C MAX. [d]	UNIT
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	-	-15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = ± 10 V V+ = 13.5 V, V- = -13.5 V	Room Full	30	-	45 55	Ω
D Drain-Source On-Resistance	$\Delta R_{DS(on)}$	I_S = - 10 mA, V_D = ± 5 V, 0 V V+ = 16.5 V, V- = -16.5 V	Room Full	3	-	3 5	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V- = -16.5 V V_D = ± 15.5 V, VS = ± 15.5 V	Room Hot	-0.01	-0.5 -5	0.5 5	nA
	$I_{D(off)}$		Room Hot	-0.01	-0.5 -5	0.5 5	nA
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V- = - 16.5 V V_S = V_D = ± 15.5 V	Room Hot	-0.04	-1 -10	1 10	nA
Digital Control							
Input Current VIN Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V	Full	0.005	-1	1	µA
Input Current VIN High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V	Full	0.005	-1	1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room	75	-	150	ns
Turn-Off Time	t_{OFF}		Room	30	-	100	ns
Break-Before-Make Time Delay (DG403)	t_D	R_L = 300 Ω, C_L = 35 pF	Room	35	5	-	ns
Charge Injection	Q	C_L = 10 nF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	60	-	-	pC
Off Isolation Reject Ratio	O_{IRR}	R_L = 100 Ω, C_L = 5 pF f = 1 MHz	Room	72	-	-	dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	90	-	-	dB
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room	12	-	-	pF
Drain Off Capacitance	$CD_{(off)}$		Room	12	-	-	pF
Channel On Capacitance	C_D, $C_{S(on)}$		Room	39	-	-	pF
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 or 5 V	Room Full	0.01	-	1 5	µA
Negative Supply Current	I-		Room Full	-0.01	-1 -5	-	µA
Logic Supply Current	I_L		Room Full	0.01	-	1 5	µA
Ground Current	I_{GND}		Room Full	-0.01	-1 -5	-	µA

Note

a. Refer to PROCESS OPTION FLOWCHART
b. Room = 25 °C, Full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. V_{IN} = input voltage to perform proper function

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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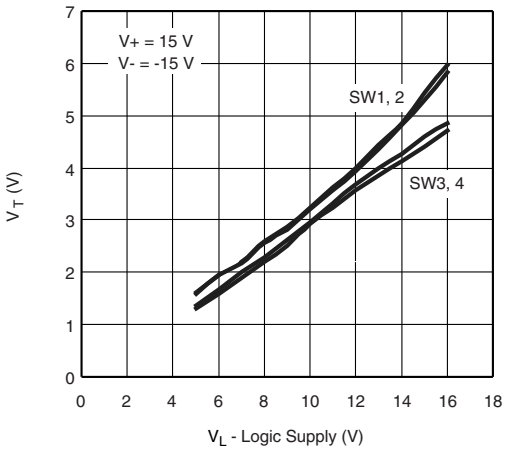
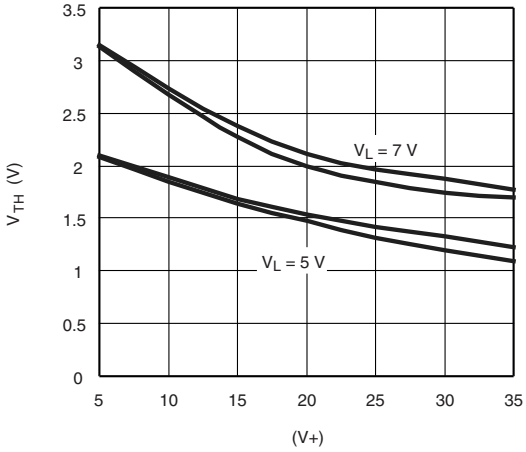
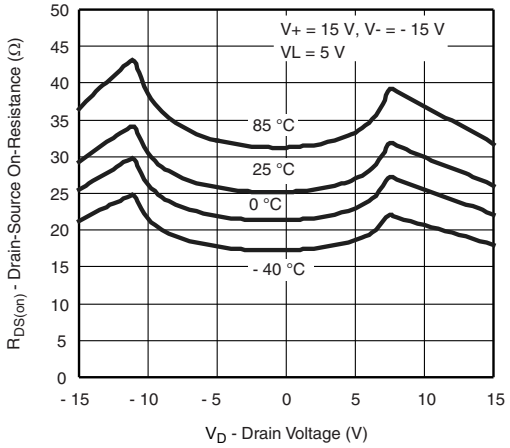


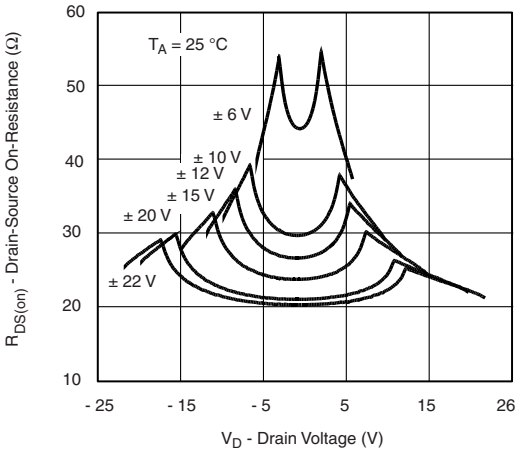
Input Switching Threshold vs. Logic Supply Voltage



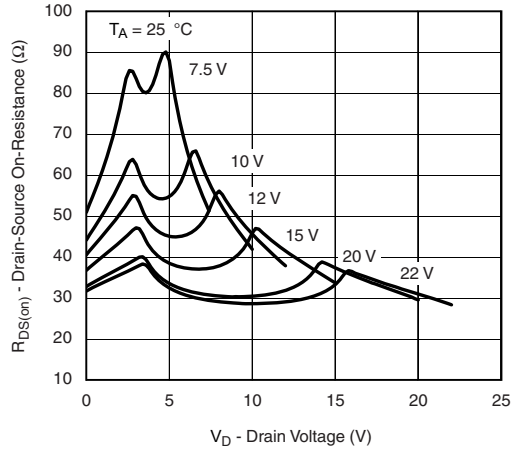
Input Switching Threshold vs. Supply Voltages



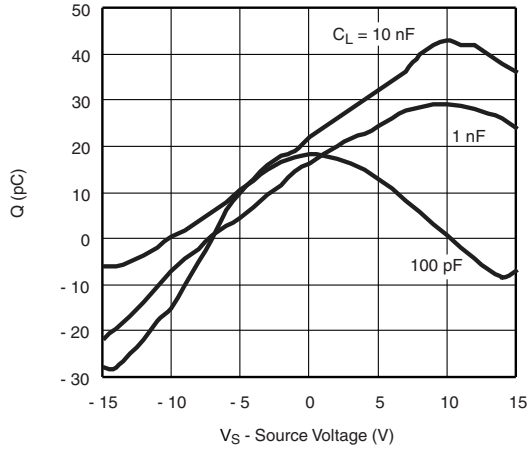
$R_{DS(on)}$ vs. V_D and Temperature



$R_{DS(on)}$ vs. V_D and Power Supply Voltage



$R_{DS(on)}$ vs. V_D and Power Supply Voltage (V- = 0 V)



Charge Injection vs. Analog Voltage

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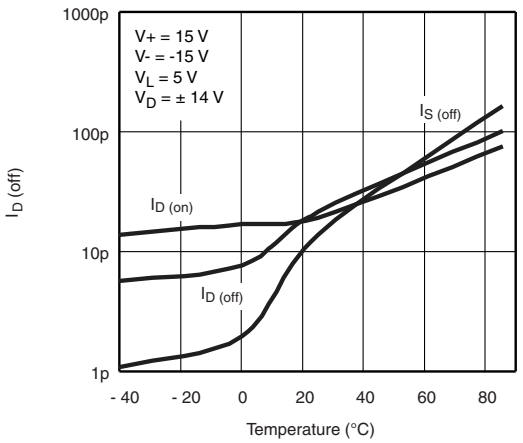
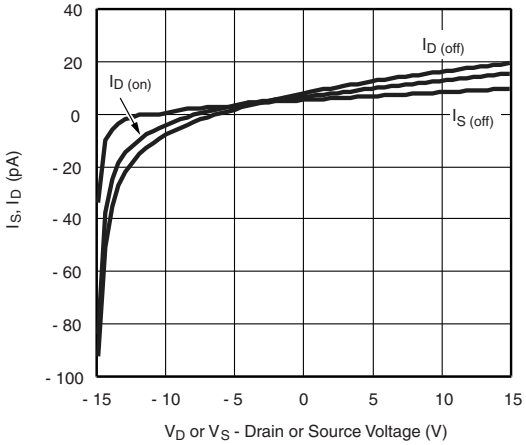
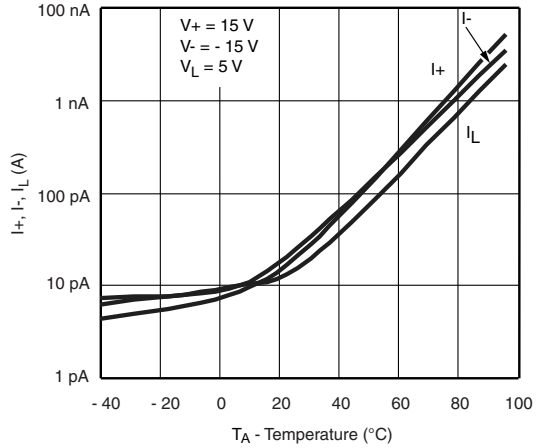


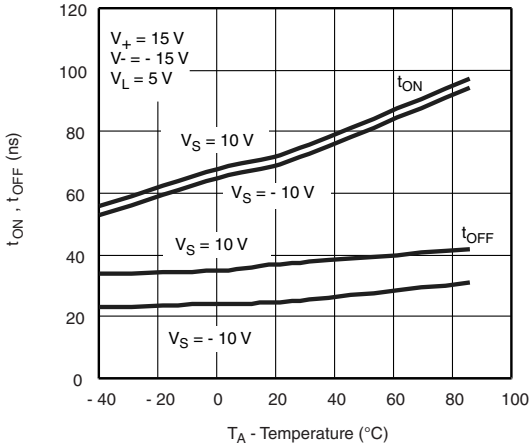
Leakage Current vs. Temperature



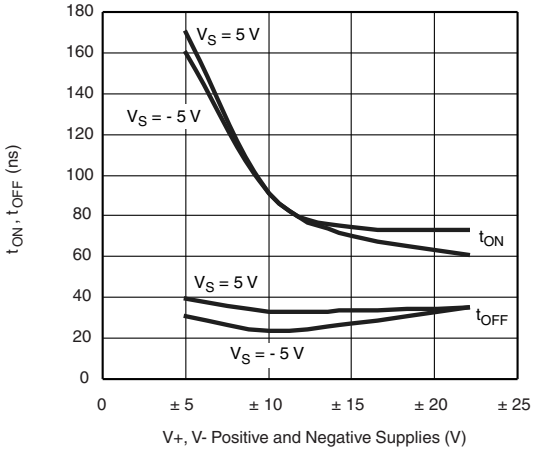
Leakage Current vs. Analog Voltage



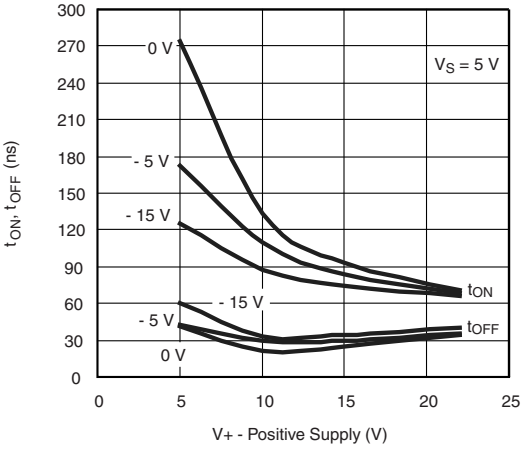
Supply Current vs. Temperature



Switching Time vs. Temperature [a]



Switching Time vs. Power Supply Voltage [a]



Switching Time vs. Positive Supply Voltage [a]

Note

a. Refer to Figure 2 for test conditions

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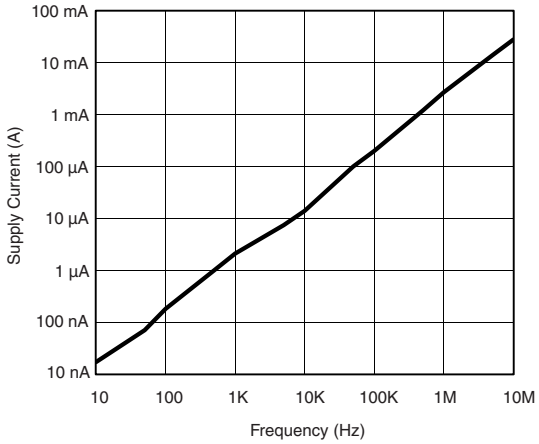

Supply Current vs. Switching Frequency

SCHEMATIC DIAGRAM Typical Channel

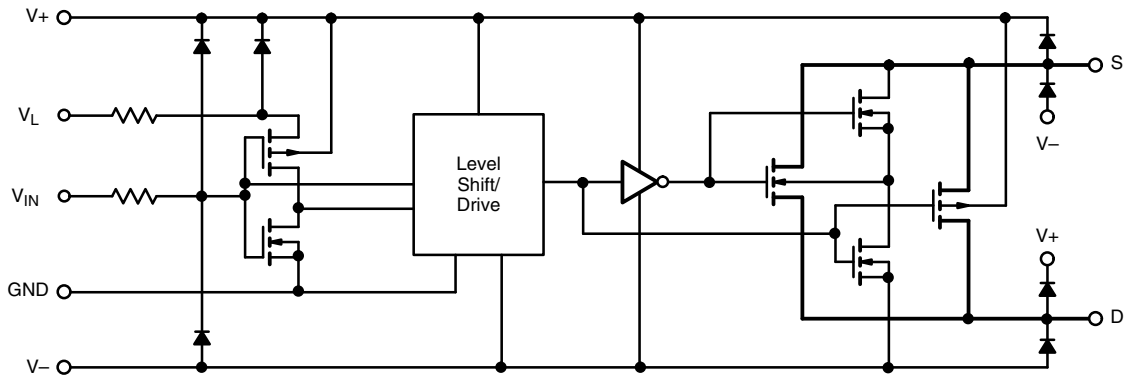

Fig. 1 - Schematic Diagram

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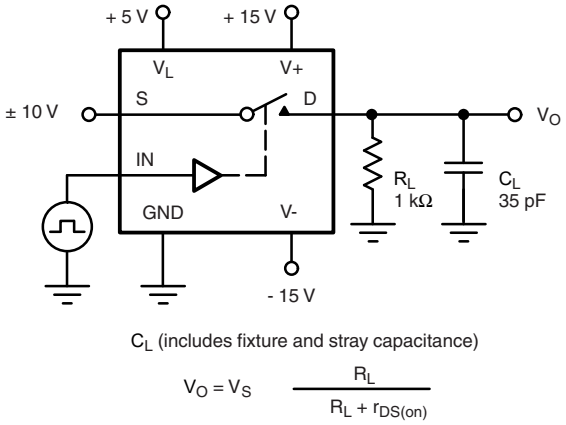
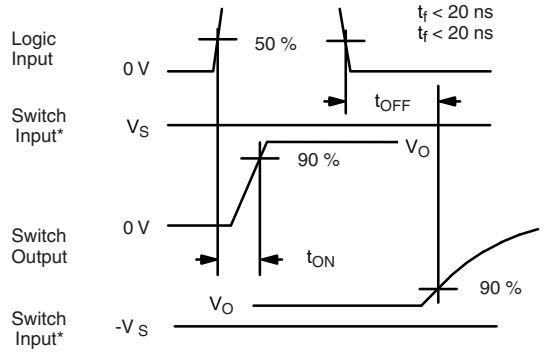
TEST CIRCUITS

VO is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



C_L (includes fixture and stray capacitance)

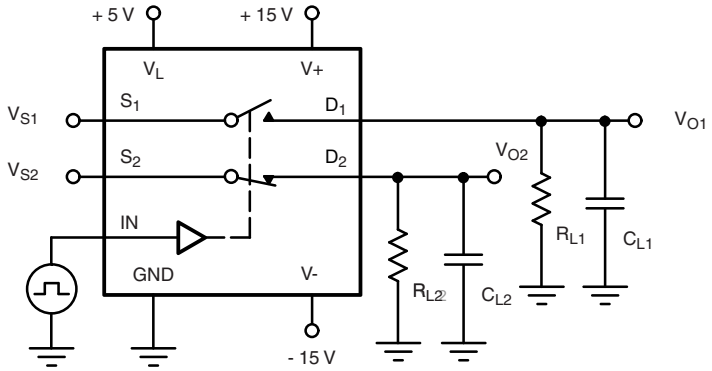
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



* V_S = 10 V for t_{ON}, V_S = - 10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 2 - Switching Time



C_L (includes fixture and stray capacitance)

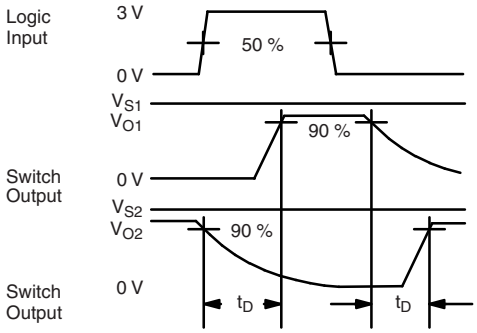
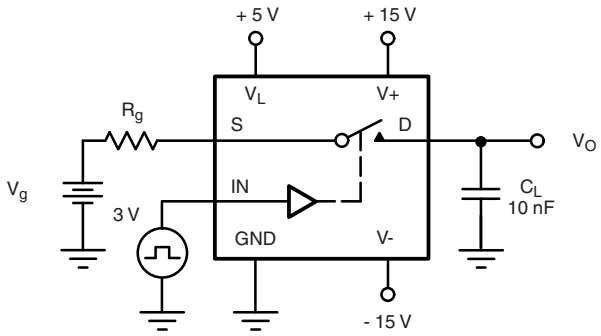


Fig. 3 - Break-Before-Make



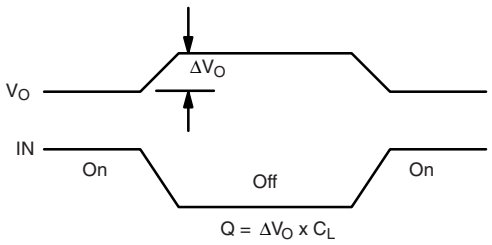


Fig. 4 - Charge Injection

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TEST CIRCUITS

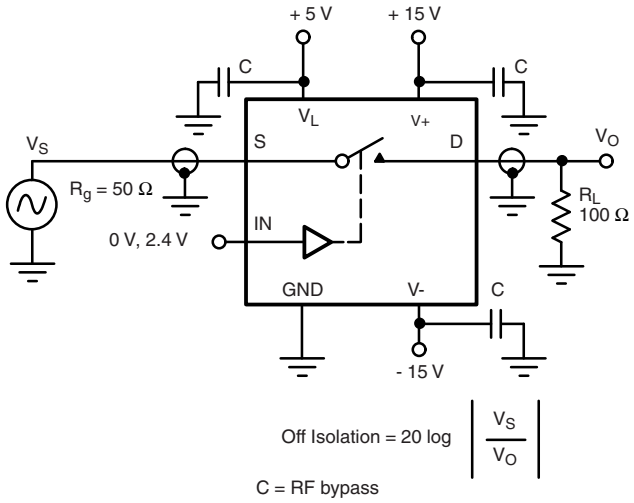

Fig. 5 - Off Isolation

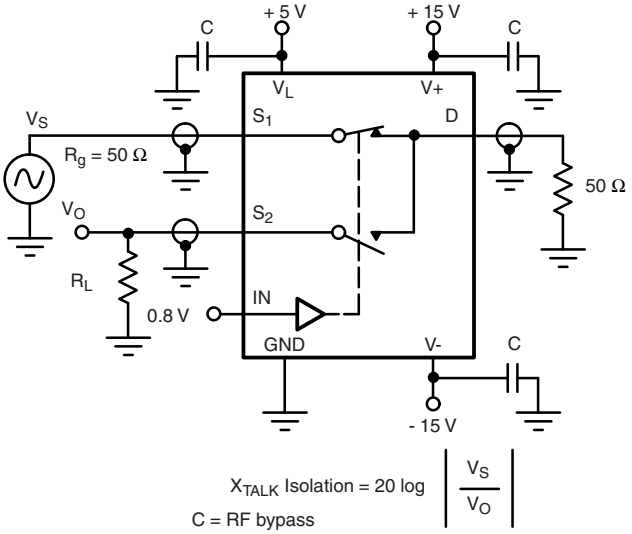

Fig. 7 - Crosstalk

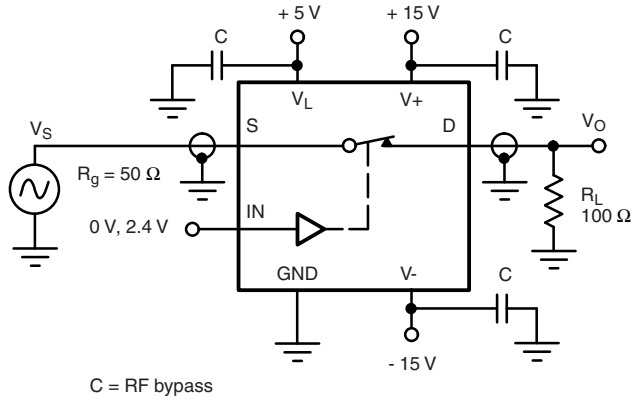

Fig. 6 - Insertion Loss

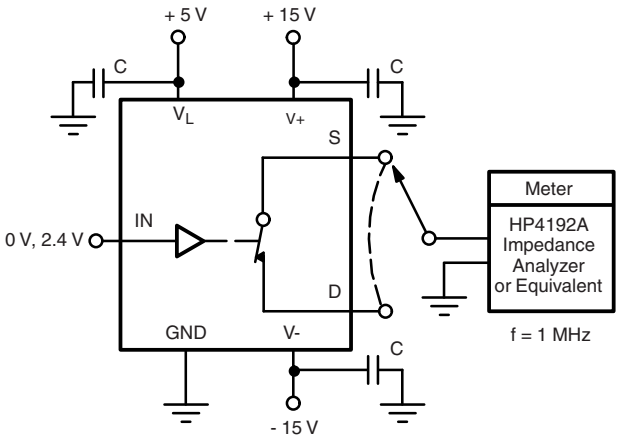

Fig. 8 - Capacitances

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APPLICATIONS

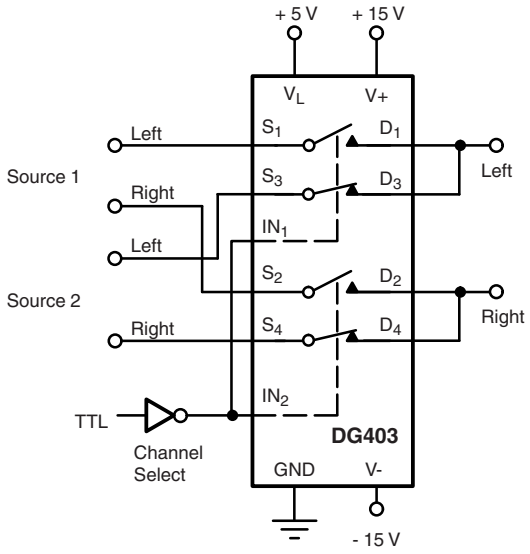

Fig. 9 - Stereo Source Selector

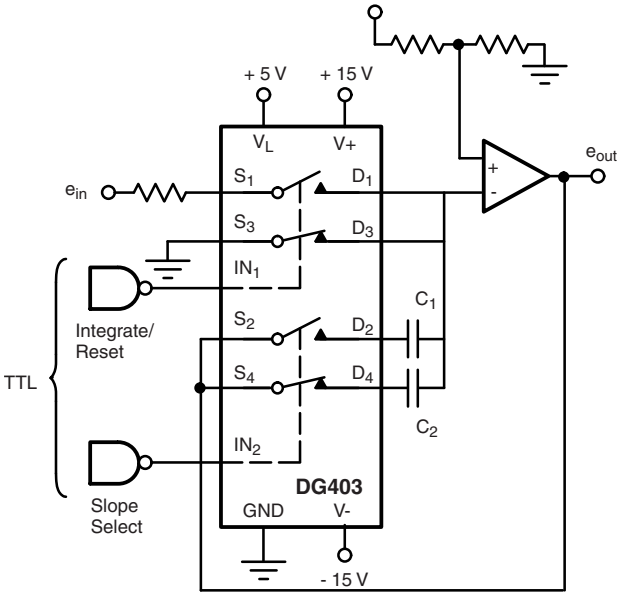

Fig. 10 - Dual Slope Integrator

Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C1 or C2. Another one selects ein or discharges the capacitor in preparation for the next integration cycle.

Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

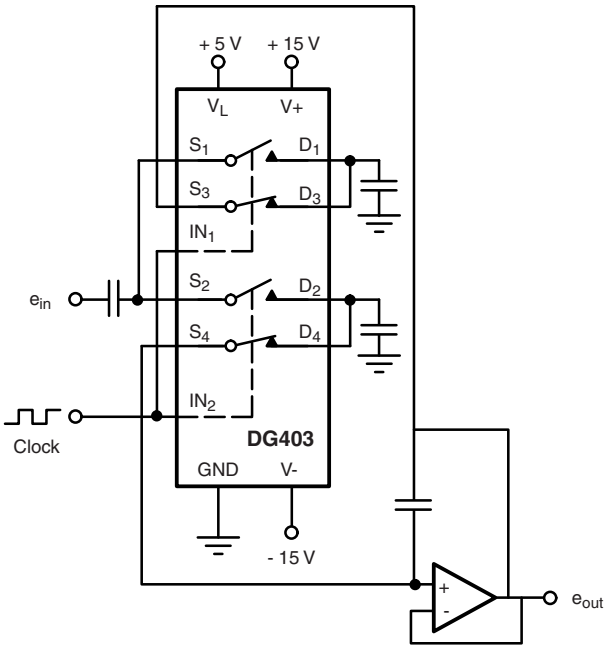

Fig. 11 - Band-Pass Switched Capacitor Filter

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APPLICATIONS

Peak Detector:

A3 acting as a comparator provides the logic drive for operating SW1. The output of A2 is fed back to A3 and compared to the analog input ein. If ein > eout the output of A3 is high keeping SW1 closed. This allows C1 to charge up to the analog input voltage. When ein goes below eout A3 goes negative, turning SW1 off. The system will therefore store the most positive analog input experienced.

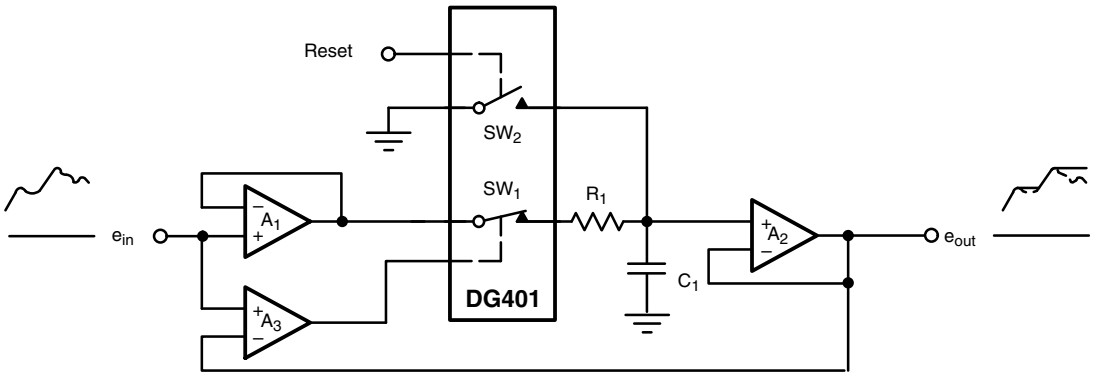

Fig. 12 - Positive Peak Detector

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PRODUCT SUMMARY			
Part number	DG401	DG403	DG405
Status code	2	2	2
Configuration	SPST x 2, NO	SPST x 4, Comp, two pairs	SPST x 4, NO, two pairs
Single supply min. (V)	7	7	7
Single supply max. (V)	36	36	36
Dual supply min. (V)	7	7	7
Dual supply max. (V)	22	22	22
On-resistance (Ω)	30	30	30
Charge injection (pC)	60	60	60
Source on capacitance (pF)	39	39	39
Source off capacitance (pF)	12	12	12
Leakage switch on typ. (nA)	0.04	0.04	0.04
Leakage switch off max. (nA)	0.5	0.5	0.5
-3 dB bandwidth (MHz)	-	-	-
Package	SO-16 (Narrow) AS	SO-16 (Narrow) AS	SO-16 (Narrow) AS
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel
Single supply operation	yes	yes	yes
Dual supply operation	yes	yes	yes
Turn on time max. (ns)	150	150	150
Crosstalk and off isolation	-72	-72	-72

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