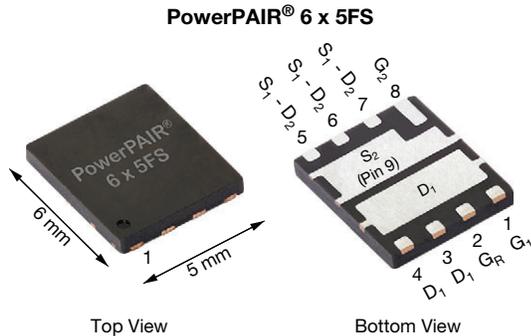


## Symmetric Dual N-Channel 80 V (D-S) MOSFET



### FEATURES

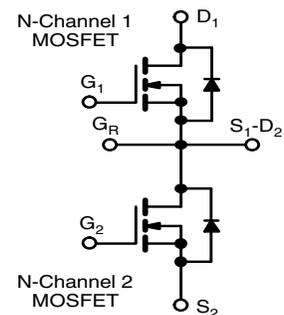
- TrenchFET® Gen IV power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Symmetric dual N-channel
- Flip chip technology optimal thermal design
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Buck-boost
- Half-bridge synchronous rectification
- Telecom DC/DC
- Motor drive control



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	80
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 10 V	0.0055
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 4.5 V	0.0065
Q <sub>g</sub> typ. (nC)	25
I <sub>D</sub> (A) <sup>a</sup>	72
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAIR 6 x 5FS
Lead (Pb)-free and halogen-free	SiZF680LDT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V <sub>DS</sub>	80	V	
Gate-source voltage	V <sub>GS</sub>	± 20		
Continuous drain current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	72	
		T <sub>C</sub> = 70 °C	57.5	
		T <sub>A</sub> = 25 °C	18.6 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	15 <sup>b, c</sup>	
Pulsed drain current (t = 100 μs)	I <sub>DM</sub>	200	A	
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C		57
		T <sub>A</sub> = 25 °C		3.8 <sup>b, c</sup>
Single pulse avalanche current	I <sub>AS</sub>	37	mJ	
Single pulse avalanche energy	E <sub>AS</sub>	69		
Maximum power dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	62.5	
		T <sub>C</sub> = 70 °C	40	
		T <sub>A</sub> = 25 °C	4.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	2.7 <sup>b, c</sup>	
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d, e</sup>		260		

### Notes

- T<sub>C</sub> = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	24	30	°C/W
Maximum junction-to-case (source)	Steady state	$R_{thJC}$	1.6	2.0	

**Notes**

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 60 °C/W for channel-1 and channel-2

SPECIFICATIONS ( $T_J = 25$ °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	80	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10$ mA	-	56	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250$ $\mu$ A	-	-5.8	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	1	-	2.4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 80$ V, $V_{GS} = 0$ V	-	-	1	$\mu$ A
		$V_{DS} = 80$ V, $V_{GS} = 0$ V, $T_J = 70$ °C	-	-	10	
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 15$ A	-	0.0039	0.0055	$\Omega$
		$V_{GS} = 4.5$ V, $I_D = 10$ A	-	0.0046	0.0065	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15$ V, $I_D = 30$ A	-	170	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{ISS}$	$V_{DS} = 40$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	4260	-	pF
Output capacitance	$C_{OSS}$		-	375	-	
Reverse transfer capacitance	$C_{RSS}$		-	21	-	
Total gate charge	$Q_g$	$V_{DS} = 40$ V, $V_{GS} = 10$ V, $I_D = 15$ A	-	55	85	nC
Gate-source charge	$Q_{gs}$	$V_{DS} = 40$ V, $V_{GS} = 4.5$ V, $I_D = 15$ A	-	25	38	
Gate-drain charge	$Q_{gd}$		-	12	-	
Output charge	$Q_{oss}$		$V_{DS} = 40$ V, $V_{GS} = 0$ V	-	5.6	
Gate resistance	$R_g$	$f = 1$ MHz	0.26	1.3	2.6	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 40$ V, $R_L = 4$ $\Omega$ , $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$	-	15	30	ns
Rise time	$t_r$		-	6	15	
Turn-off delay time	$t_{d(off)}$		-	43	90	
Fall time	$t_f$		-	7	15	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 40$ V, $R_L = 4$ $\Omega$ , $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ $\Omega$	-	32	65	
Rise time	$t_r$		-	125	250	
Turn-off delay time	$t_{d(off)}$		-	40	80	
Fall time	$t_f$		-	13	30	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	-	-	57	A
Pulse diode forward current	$I_{SM}$		-	-	200	
Body diode voltage	$V_{SD}$	$I_S = 10$ A, $V_{GS} = 0$ V	-	0.76	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C	-	41	80	ns
Body diode reverse recovery charge	$Q_{rr}$		-	61	120	nC
Reverse recovery fall time	$t_a$		-	32	-	ns
Reverse recovery rise time	$t_b$		-	9	-	

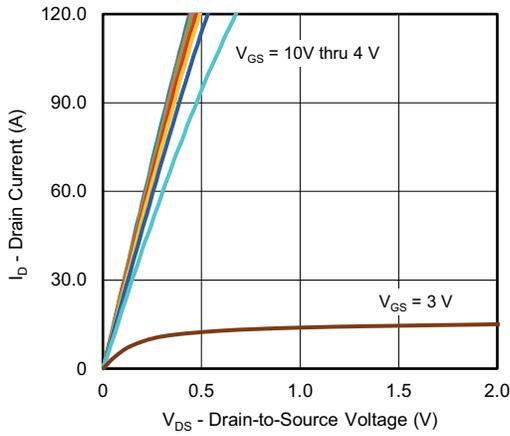
**Notes**

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- b. Guaranteed by design, not subject to production testing

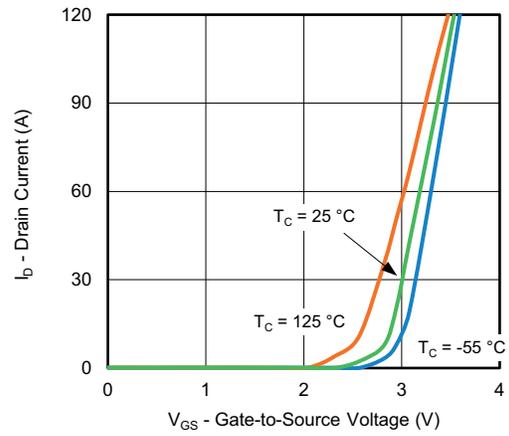
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



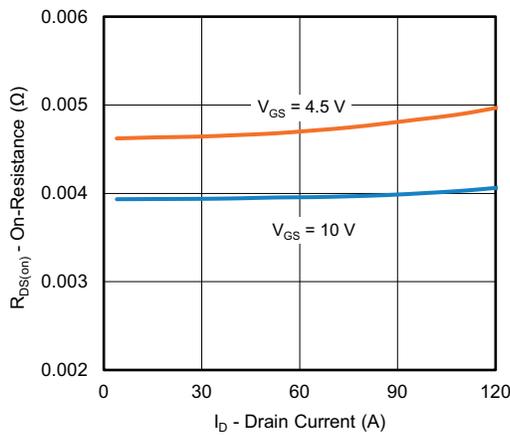
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



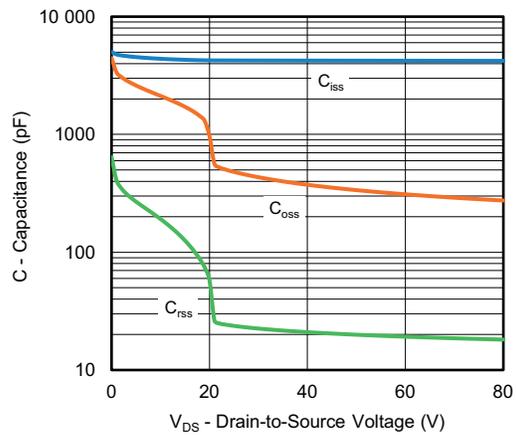
Output Characteristics



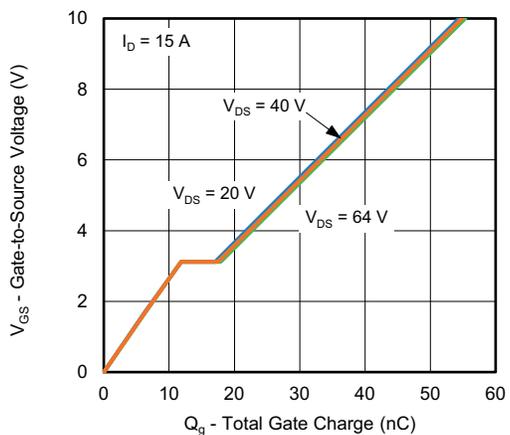
Transfer Characteristics



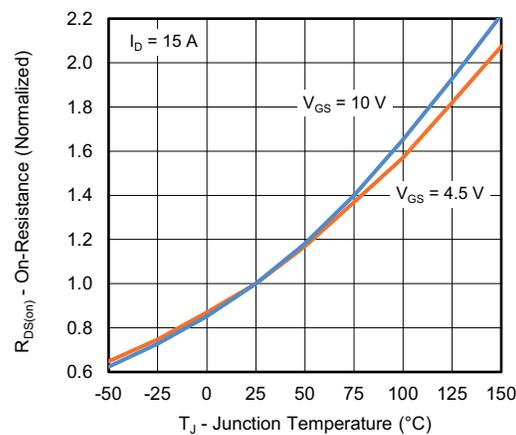
On-Resistance vs. Drain Current



Capacitance

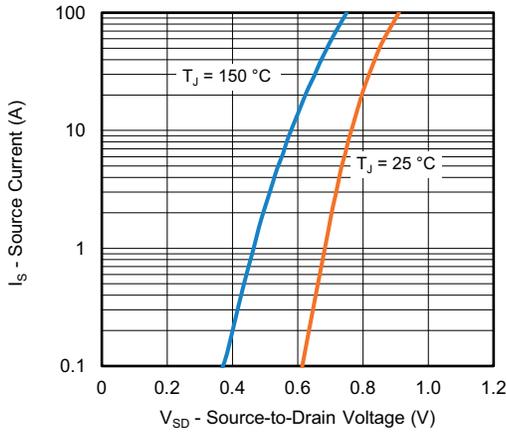


Gate Charge

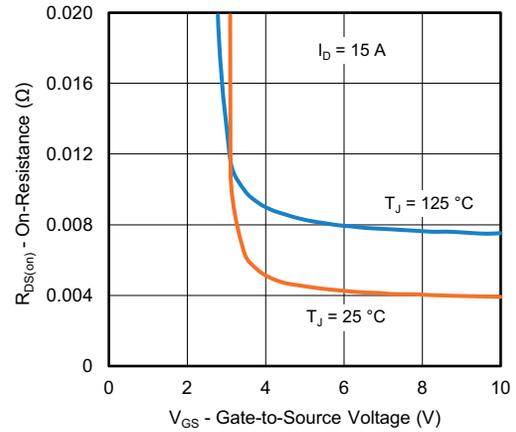


On-Resistance vs. Junction Temperature

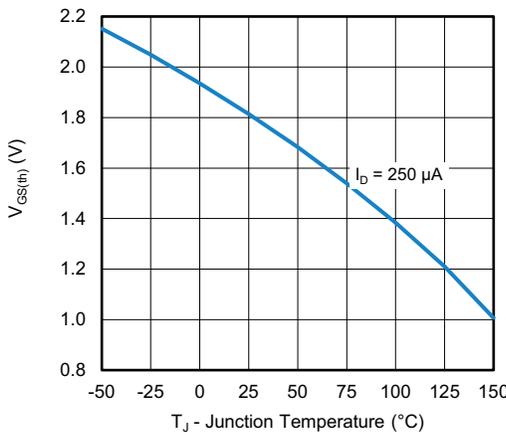
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



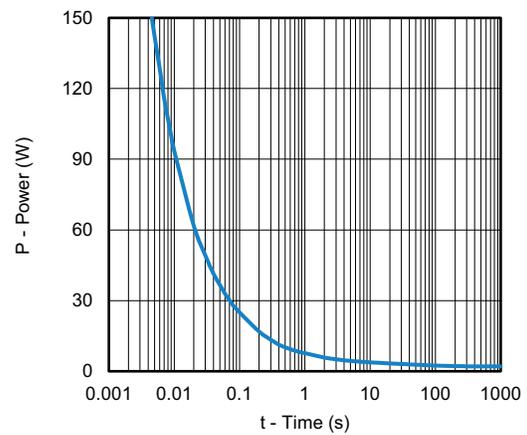
**Source-Drain Diode Forward Voltage**



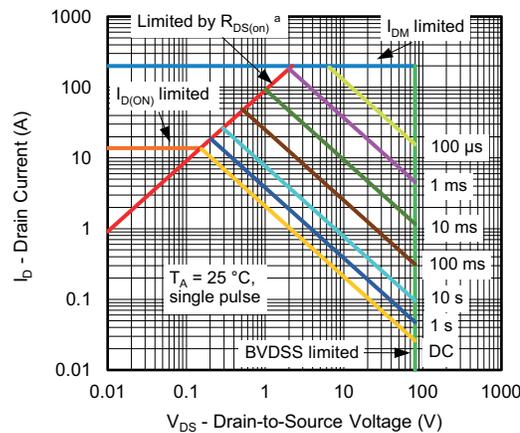
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



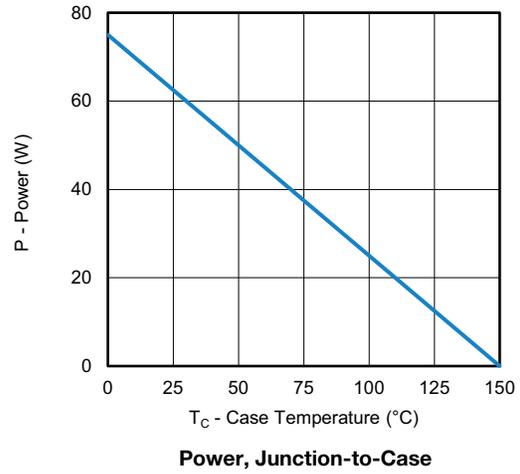
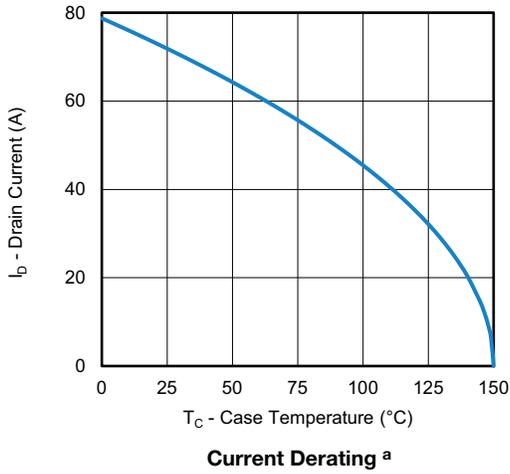
**Safe Operating Area, Junction-to-Ambient**

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

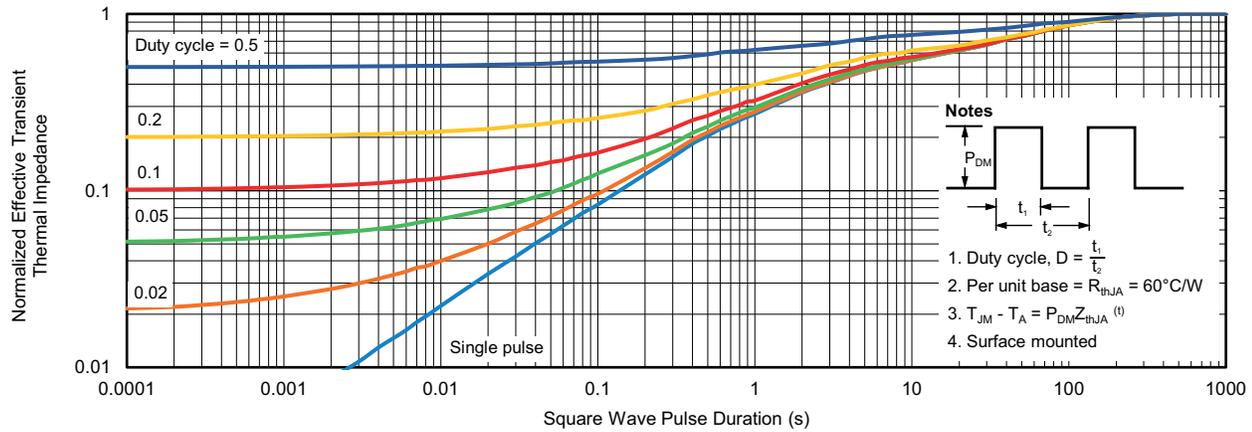


**Note**

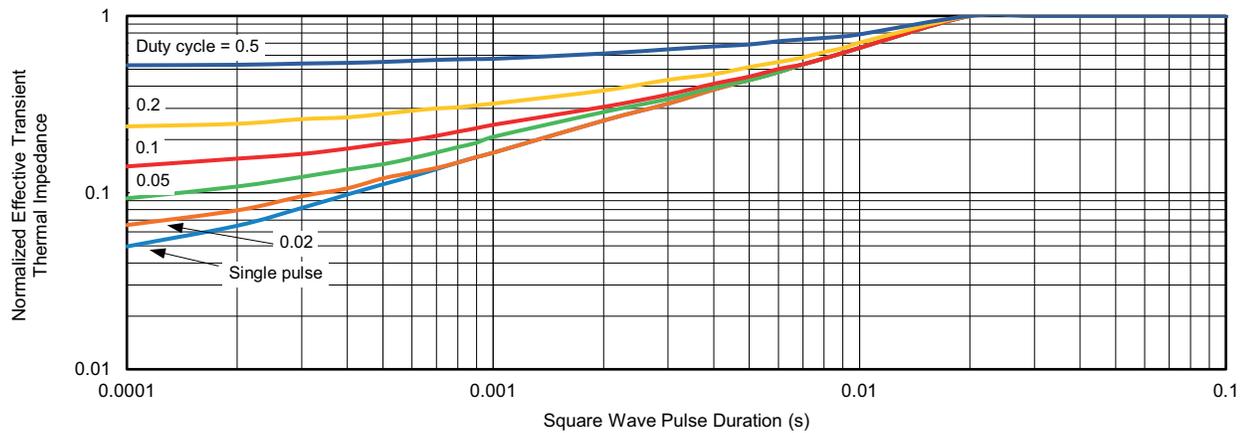
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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