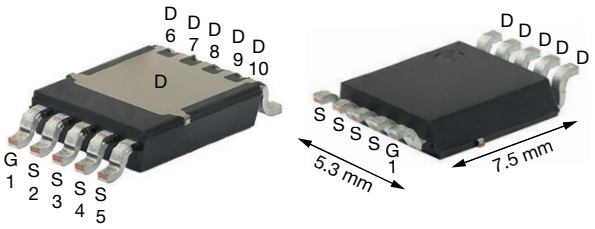
Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SO-10LR



Top View Bottom View

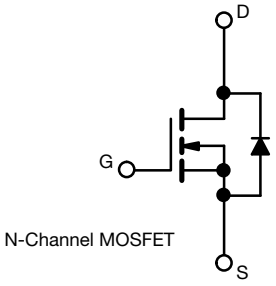
FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.00106
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.00142
I_D (A) [d]	396
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-10LR
Lead (Pb)-free and halogen-free	SQJ134ELR (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current [d]	T_C = 25 °C	I_D	396	A
	T_C = 125 °C		229	
Continuous source current (diode conduction) [d]		I_S	290	
Pulsed drain current [d]		I_{DM}	889	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	61	
Single pulse avalanche energy		E_{AS}	186	mJ
Maximum power dissipation	T_C = 25 °C	P_D	319	W
	T_C = 125 °C		106	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [b]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient [c]	PCB mount [a]	R_{thJA}	42	°C/W
Junction-to-case (drain)		R_{thJC}	0.5	

Notes

a. When mounted on 1" square PCB (FR4 material)
b. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
c. Using thermal characterization methods based on JESD51-14
d. Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.2	1.7	2.2	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	-	-	10	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	250	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 15 A	-	0.00082	0.00106	Ω
		V_{GS} = 4.5 V	I_D = 15 A	-	0.00114	0.00142	Ω
		V_{GS} = 10 V	I_D = 15 A, T_J = 125 °C	-	-	0.0018	
		V_{GS} = 10 V	I_D = 15 A, T_J = 175 °C	-	-	0.0021	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 60 A		-	135	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	7981	11 174	pF
Output capacitance	C_{oss}			-	2105	2947	
Reverse transfer capacitance	C_{rss}			-	137	192	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 40 A	-	131	197	nC
Gate-source charge [c]	Q_{gs}			-	28	-	
Gate-drain charge [c]	Q_{gd}			-	20	-	
Gate resistance	R_g	f = 1 MHz		0.3	1.2	2.3	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.5 Ω I_D ≅ 40 A, V_{GEN} = 10 V, R_g = 1 Ω		-	17	26	ns
Rise time [c]	t_r			-	9	14	
Turn-off delay time [c]	$t_{d(off)}$			-	54	81	
Fall time [c]	t_f			-	12	18	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	889	A
Forward voltage	V_{SD}	I_F = 15 A, V_{GS} = 0 V		-	-	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 10 A, di/dt = 100 A/µs		-	67	134	ns
Body diode reverse recovery charge	Q_{rr}			-	121	242	nC
Reverse recovery fall time	t_a			-	40	-	ns
Reverse recovery rise time	t_b			-	28	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-3.1	-	A

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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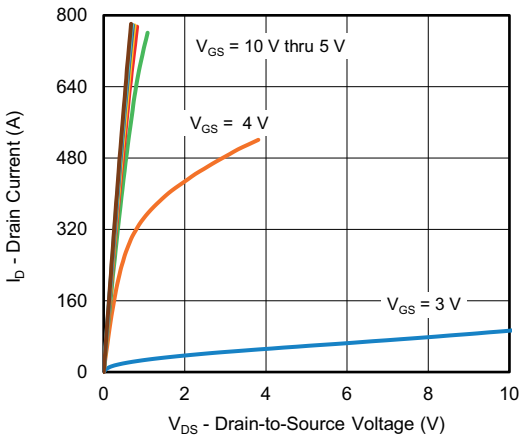
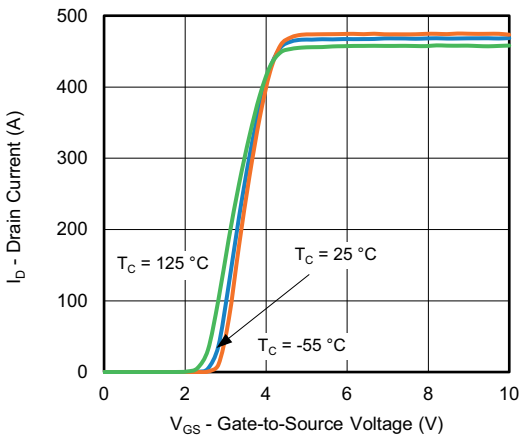
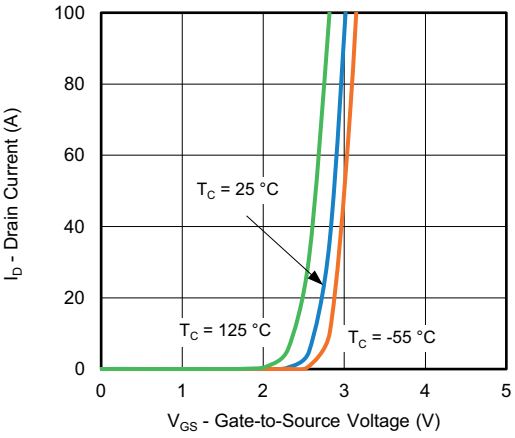
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



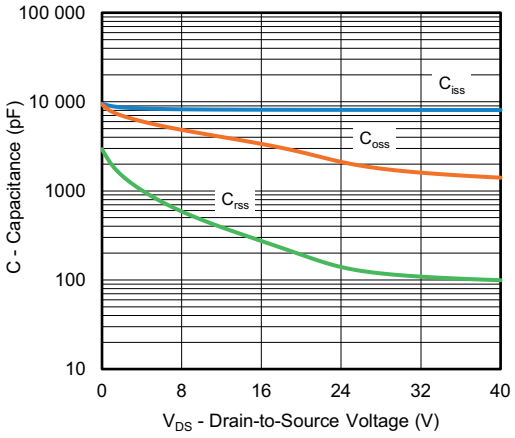
Output Characteristics



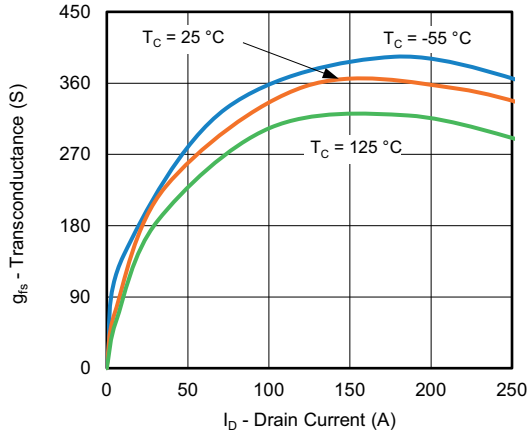
Transfer Characteristics



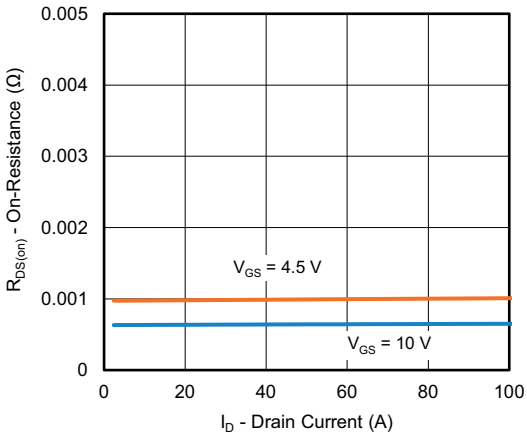
Transfer Characteristics



Capacitance



Transconductance



On-Resistance vs. Drain Current

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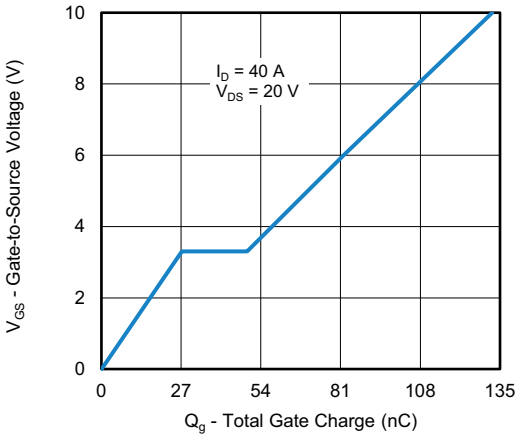
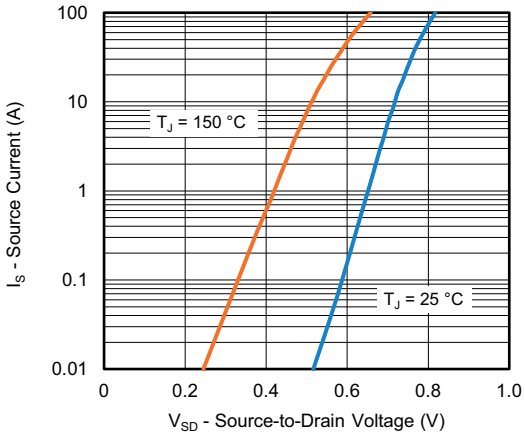
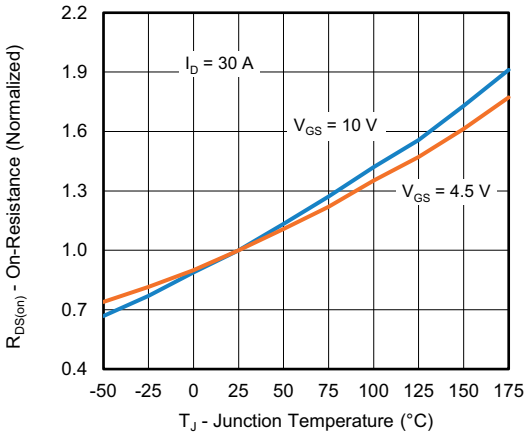


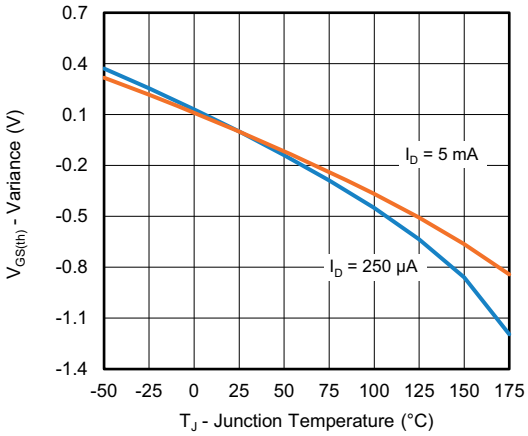
Gate Charge



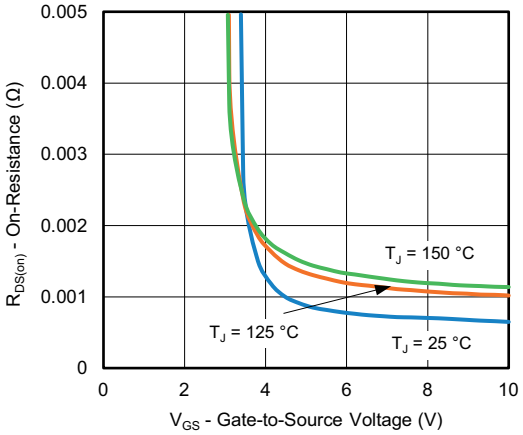
Source Drain Diode Forward Voltage



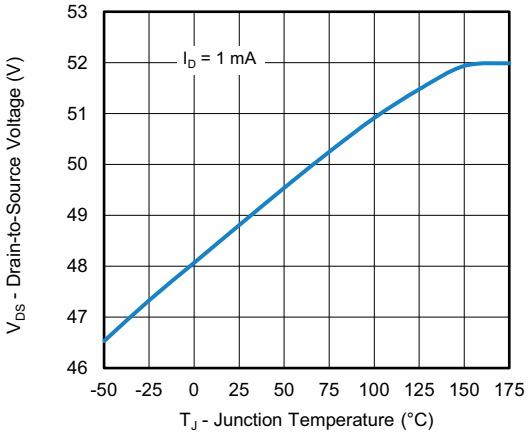
On-Resistance vs. Junction Temperature



Threshold Voltage



On-Resistance vs. Gate-to Source Voltage



Drain Source Breakdown vs. Junction Temperature

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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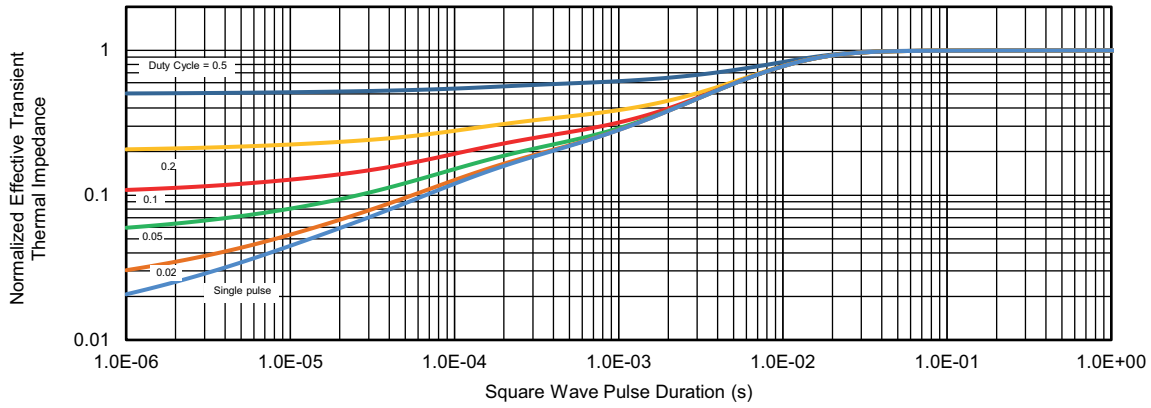
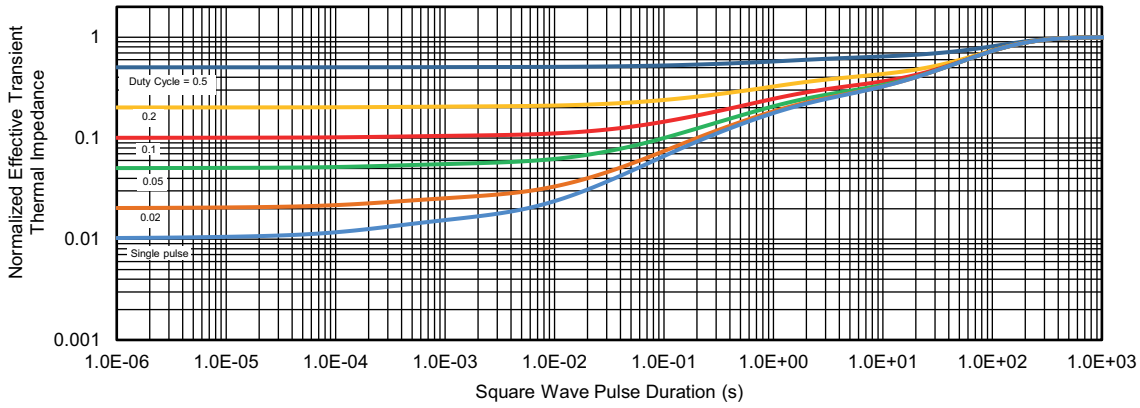


Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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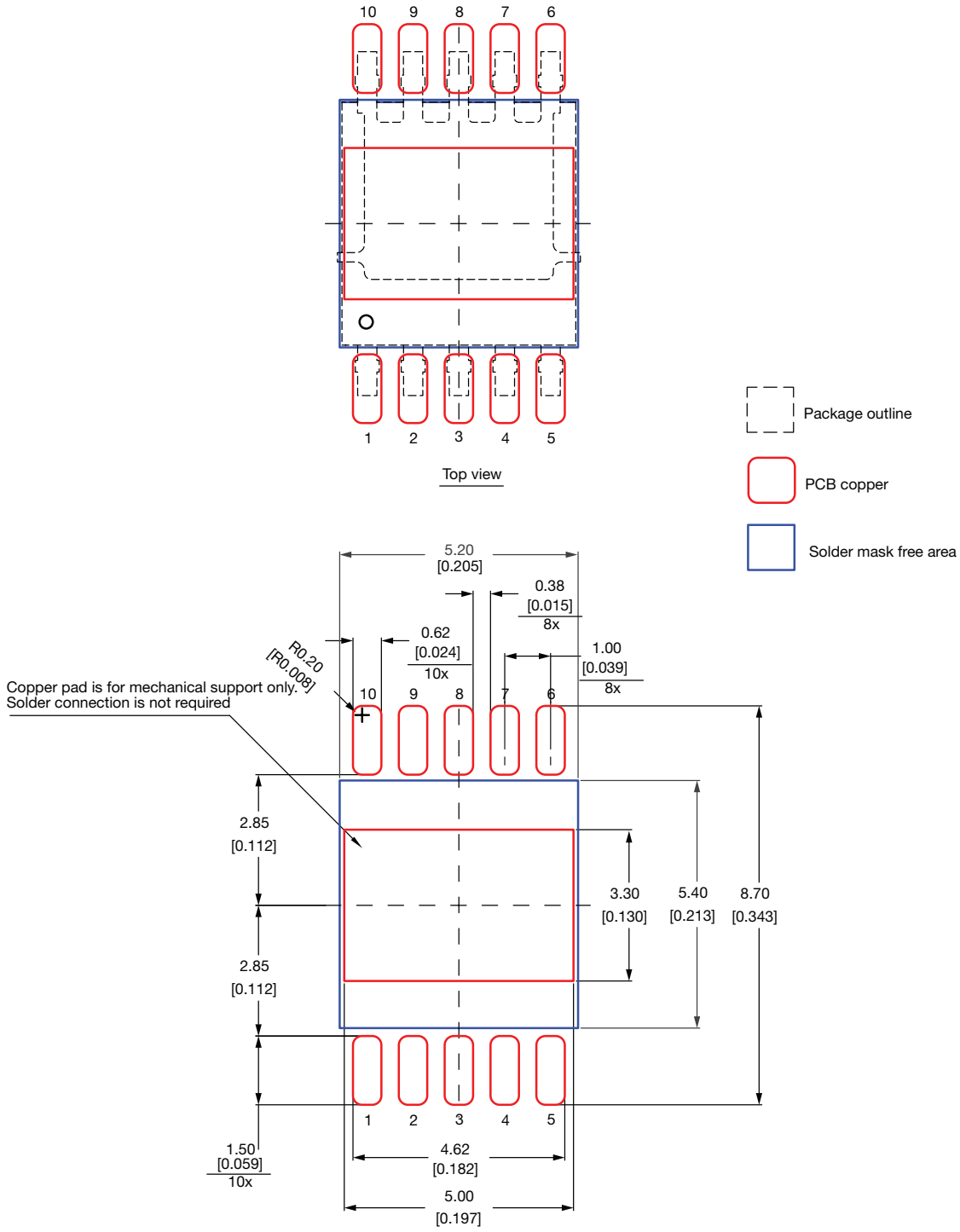
Recommended Land Pattern
PowerPAK® SO-10LR BWL (PKSO10LRWL)



Note

- Dimensions in mm [inch]
- This land pattern is for reference

ECN: C23-1310-Rev. A, 11-Dec-2023
DWG: 3021

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