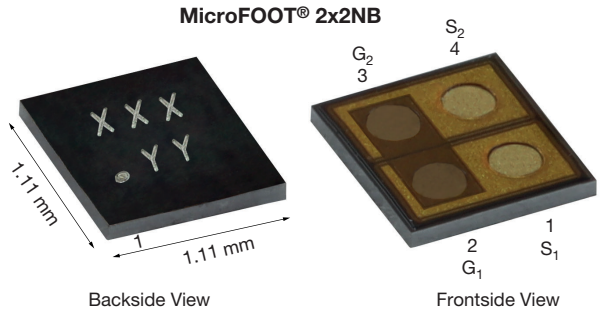
Common Drain Dual N-Channel 20 V (S1-S2) MOSFET



Marking code: XXX = Date/lot traceability code
YY = AA

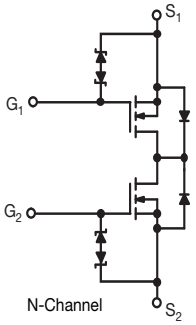
FEATURES

- TrenchFET® power MOSFET
- Ultra small 1.1 mm x 1.1 mm outline
- Ultra thin 0.13 mm max. height
- Typical ESD protection 2500 V (HBM)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Battery protection switch
- Bi-directional switch
- Load switch



PRODUCT SUMMARY	
V_{S1S2} (V)	20
$R_{S1S2(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.075
$R_{S1S2(on)}$ max. (Ω) at V_{GS} = 3.8 V	0.082
$R_{S1S2(on)}$ max. (Ω) at V_{GS} = 3.1 V	0.095
$R_{S1S2(on)}$ max. (Ω) at V_{GS} = 2.5 V	0.115
Q_g typ. (nC)	2.7
I_{S1S2} (A) [a]	2.5
Configuration	Common drain

ORDERING INFORMATION	
Package	MicroFOOT® 2x2NB
Lead (Pb)-free and halogen-free	Si8916EDB-T5-E1

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{S1S2}	20	V
Gate-source voltage		V_{GS}	± 12	
Continuous drain current (T_J = 150 °C)	T_A = 25 °C	I_{S1S2}	2.5 [a]	A
	T_A = 70 °C		2.0 [a]	
Pulsed drain current (V_{GS} = 4.5 V, t = 100 µs)		I_{S1S2}	20	
Maximum power dissipation	T_A = 25 °C	P_D	0.77 [a]	W
	T_A = 70 °C		0.49 [a]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum junction-to-ambient [a, d]	t ≤ 5 s	R_{thJA}	121	162	°C/W

Notes

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s
b. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering
c. Maximum under steady state conditions is 202 °C/W

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-source breakdown voltage	V_{S1S2}	V_{GS} = 0 V, I_{S1S2} = 250 µA	20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{S1S2}/T_J$	I_{S1S2}= 250 µA	-	17	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-3.2	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{S1S2}= 250 µA	0.6	-	1.4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V	-	-	± 0.1	µA
		V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 15	
Zero gate voltage drain current	I_{S1S2}	V_{S1S2}= 20 V, V_{GS} = 0 V	-	-	1	
		V_{S1S2}= 20 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
Drain-source on-state resistance [a]	R_{S1S2}	V_{GS} = 4.5 V, I_D = 3 A	-	0.061	0.075	Ω
		V_{GS} = 3.8 V, I_{S1S2} = 3 A	-	0.066	0.082	
		V_{GS} = 3.1 V, I_{S1S2} = 2 A	-	0.073	0.095	
		V_{GS} = 2.5 V, I_{S1S2} = 1 A	-	0.086	0.115	
Forward transconductance [a]	g_{fs}	V_{S1S2}= 10 V, I_{S1S2} = 6 A	-	15	-	S
Dynamic [b, c]						
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	-	220	-	pF
Output capacitance	C_{oss}		-	55	-	
Reverse transfer capacitance	C_{rss}		-	35	-	
Total gate charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 5 A	-	5.6	11	nC
		V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 5 A	-	2.7	5.4	
Gate-source charge	Q_{gs}		-	0.65	-	
Gate-drain charge	Q_{gd}		-	0.8	-	
Gate resistance	R_g	f = 1 MHz	0.6	3	6	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	10	20	ns
Rise time	t_r		-	40	80	
Turn-off delay time	$t_{d(off)}$		-	20	40	
Fall time	t_f		-	15	30	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	-	5	10	
Rise time	t_r		-	20	40	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	t_f		-	5	10	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_{S1S2}	T_C = 25 °C	-	-	0.38	A
Pulse diode forward current	I_{S1S2}		-	-	20	
Body diode reverse recovery time	t_{rr}	I_F = 5 A, di/dt = 100 A/µs, T_J = 25 °C	-	10	20	ns
Body diode reverse recovery charge	Q_{rr}		-	2.5	5	nC
Reverse recovery fall time	t_a		-	4	-	ns
Reverse recovery rise time	t_b		-	6	-	

Note

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. For single MOSFET only

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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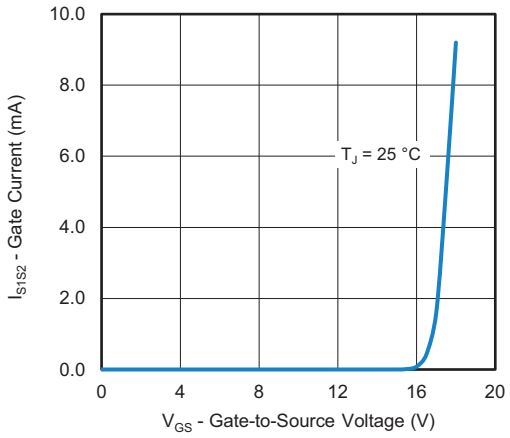
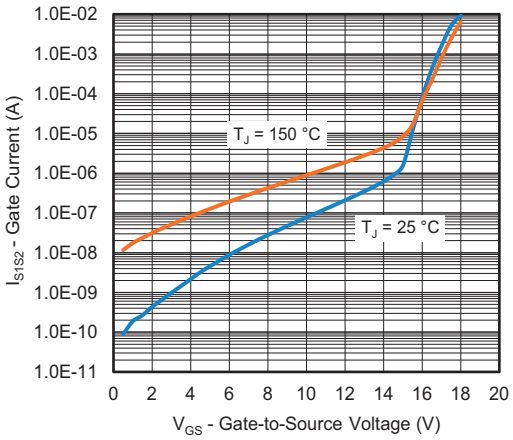
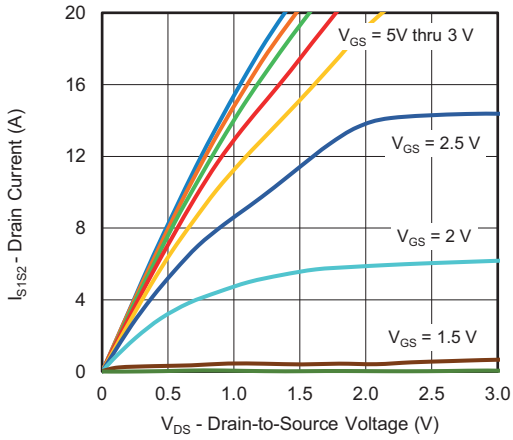


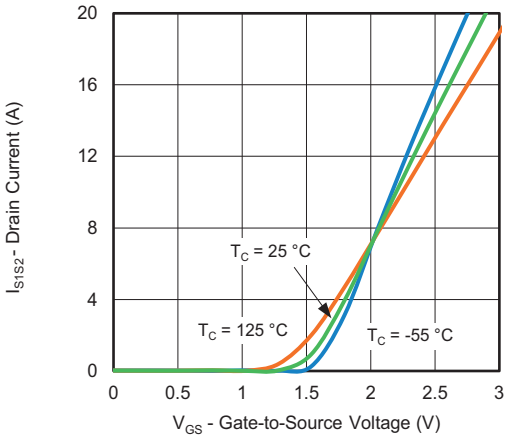
Gate Current vs. Gate-Source Voltage



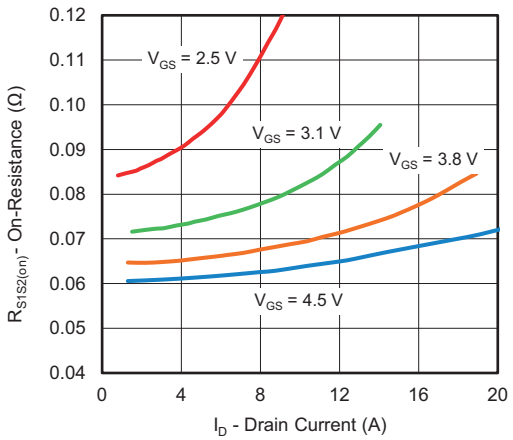
Gate Current vs. Gate-Source Voltage



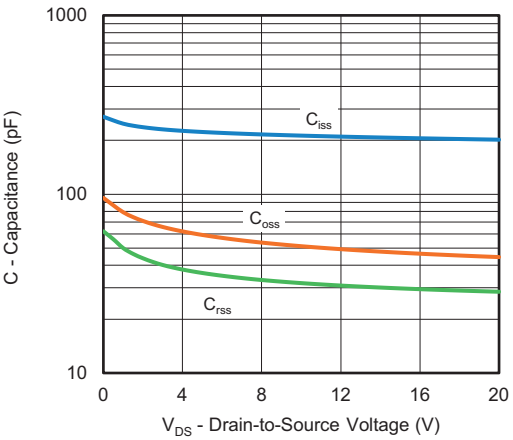
Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current



Capacitance vs. Drain-to-Source Voltage

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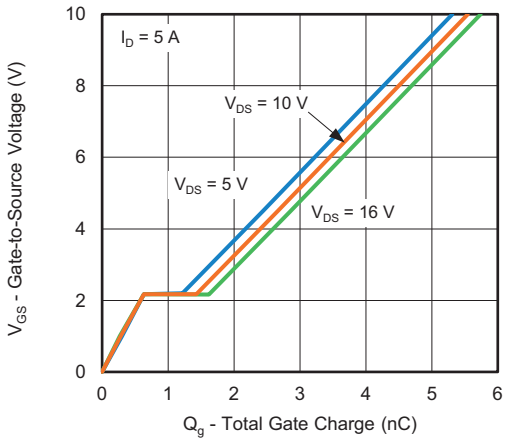
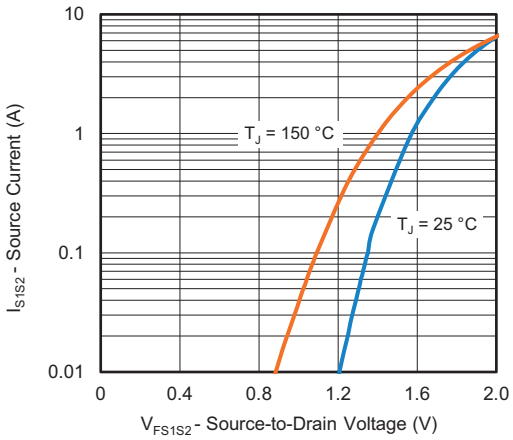
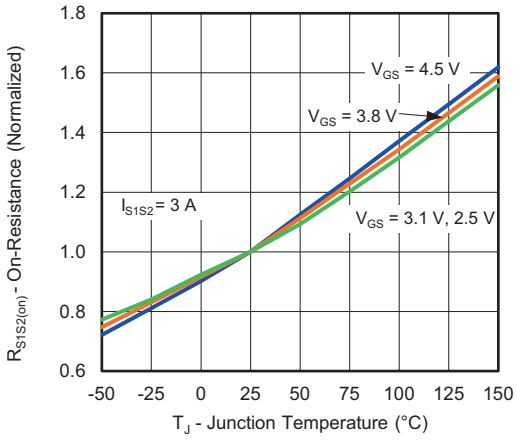


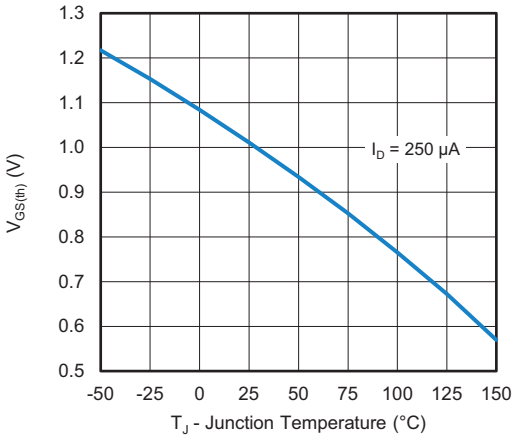
Gate Charge



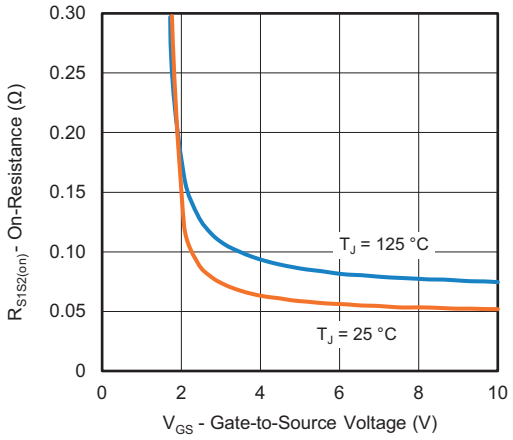
Source-Drain Diode Forward Voltage



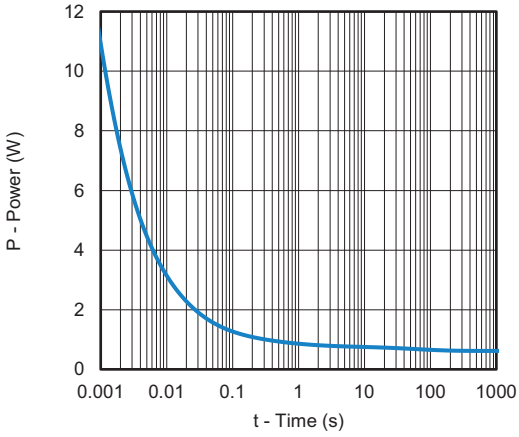
On-Resistance vs. Junction Temperature



Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient [a]

Note

a. When Mounted on 1" x 1" FR4 with full copper

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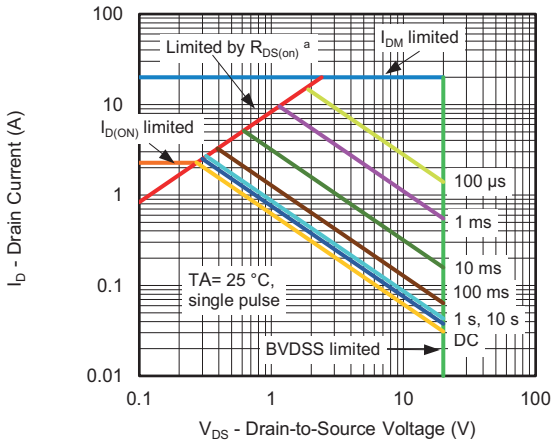
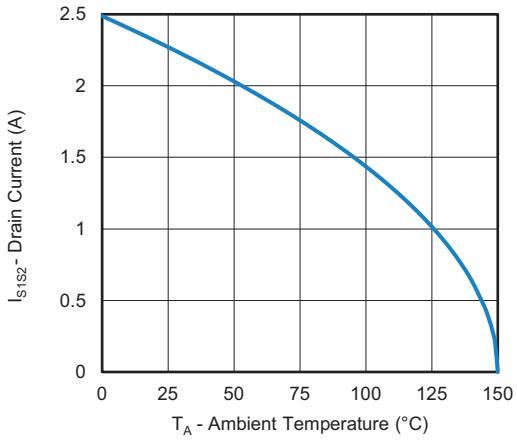
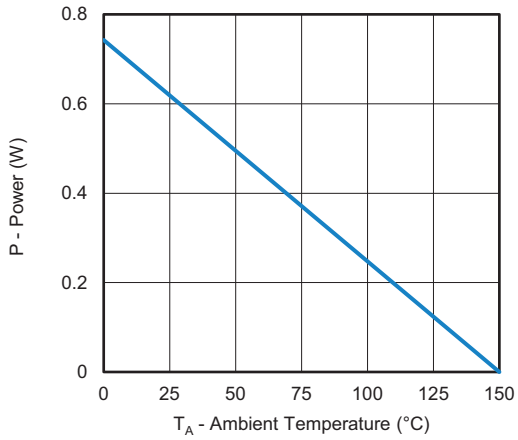


Safe Operating Area, Junction-to-Ambient b



Current Derating a, b



Power Derating b

Notes

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

b. When mounted on 1" x 1" FR4 with full copper

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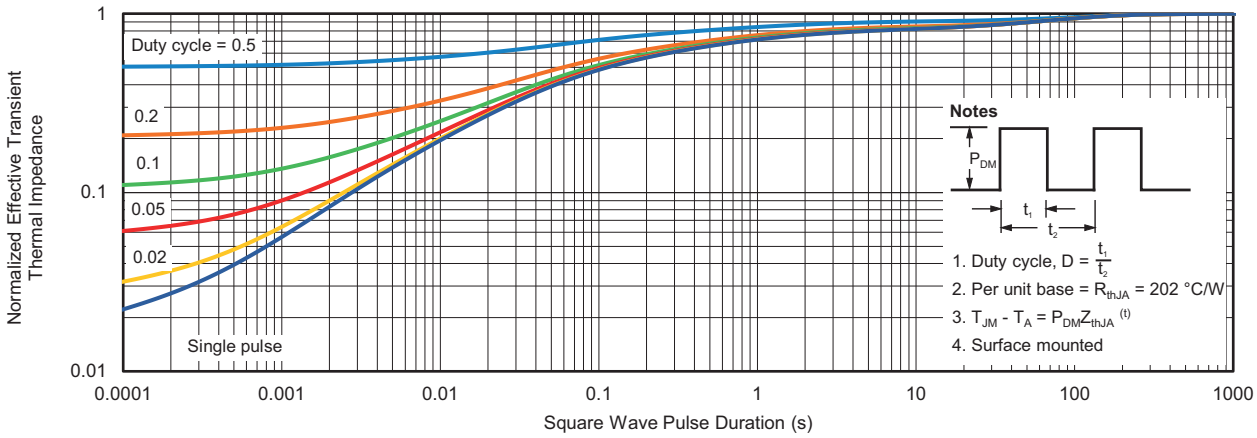

Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Maximum Copper)

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