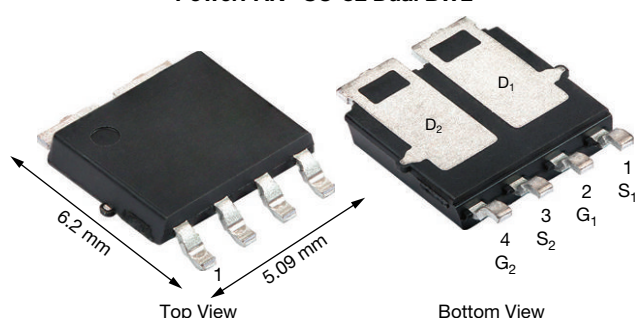


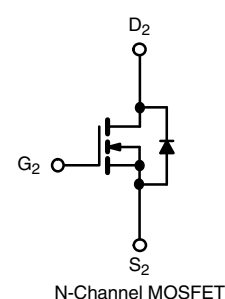
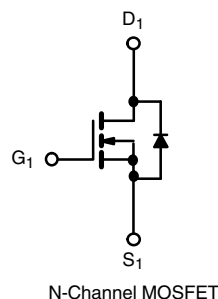
Automotive Dual N-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Dual BWL


FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


PRODUCT SUMMARY

V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0106
I_D (A) per leg ^e	62
Configuration	Dual

ORDERING INFORMATION

Package	PowerPAK® SO-8L
Lead (Pb)-free and halogen-free	SQJ710EP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	100	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current ^e	T _C = 25 °C ^a	I _D	62	A
	T _C = 125 °C		36	
Continuous Source Current (Diode conduction) ^e		I _S	54	
Pulsed Drain Current ^{b, e}		I _{DM}	134	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	35	
Single Pulse Avalanche Energy		E _{AS}	30	mJ
Maximum Power Dissipation ^{b, e}	T _C = 25 °C	P _D	90	W
	T _C = 125 °C		30	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	42	°C/W
Junction-to-Case (Drain) ^d	R_{thJC}	1.7	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per JESD51-14
- Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

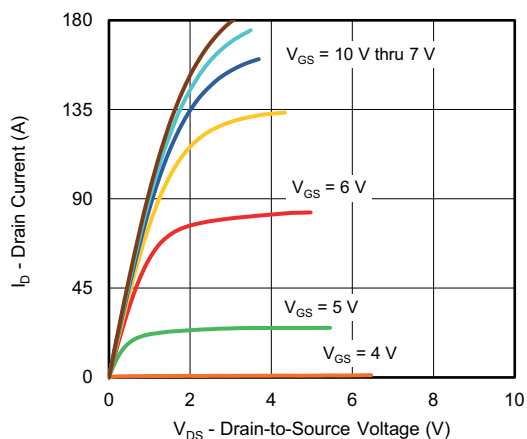
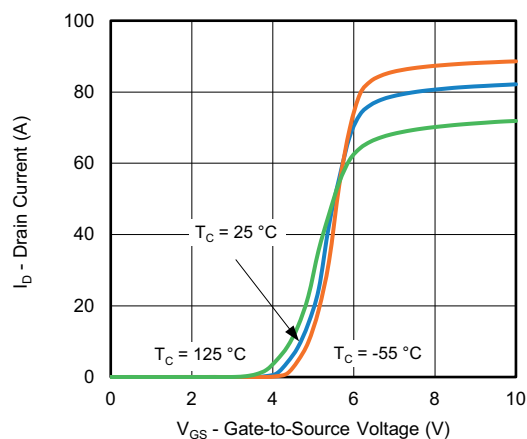
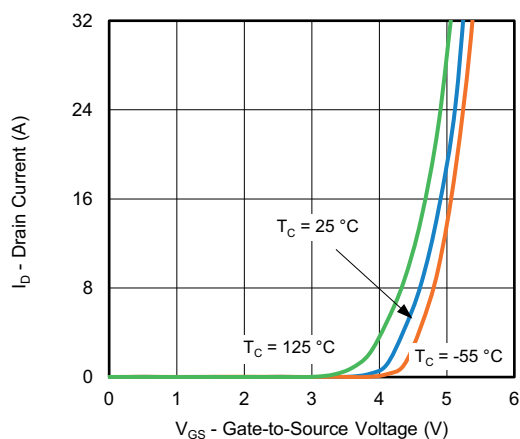
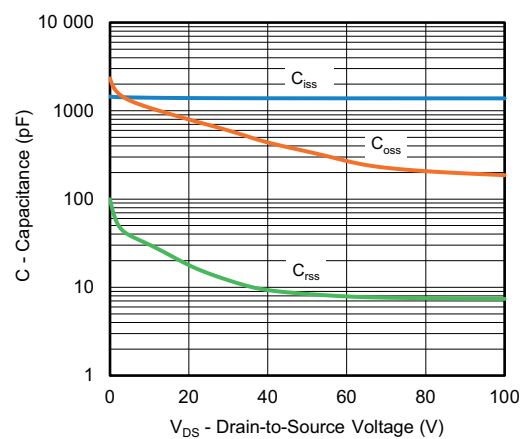
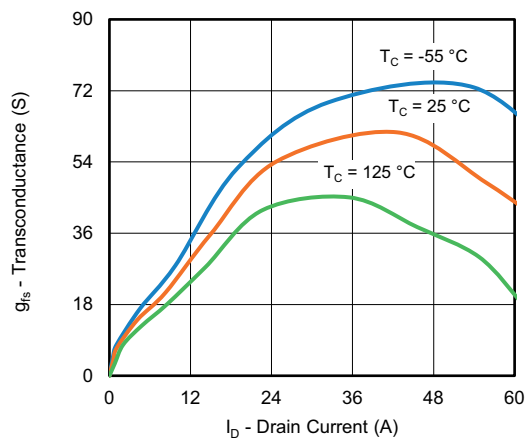
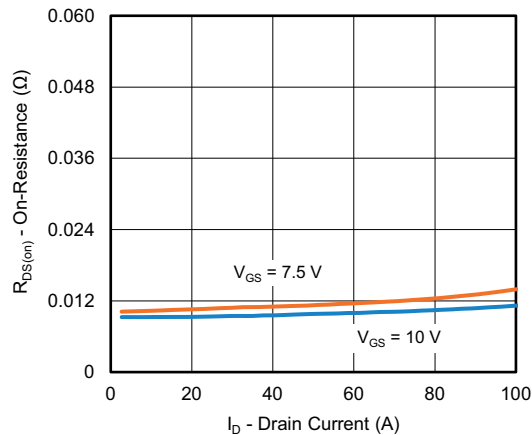


SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		100	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	3.0	4.0	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 100 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	10	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.00883	0.01060	Ω
		V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.0185	
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0236	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 15 A		-	35	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 50 V, f = 1 MHz	-	1385	2100	pF
Output Capacitance	C _{oss}			-	346	550	
Reverse Transfer Capacitance	C _{rss}			-	9	20	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 50 V, I _D = 5 A	-	17	26	nC
Gate-Source Charge ^c	Q _{gs}			-	7	-	
Gate-Drain Charge ^c	Q _{gd}			-	2	-	
Gate Resistance	R _g	f = 1 MHz		0.5	1.1	1.7	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 10 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω		-	12	25	ns
Rise Time ^c	t _r			-	5	10	
Turn-Off Delay Time ^c	t _{d(off)}			-	17	35	
Fall Time ^c	t _f			-	7	15	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	134	A
Forward Voltage	V _{SD}	I _F = 7 A, V _{GS} = 0 V		-	0.88	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 5 A, di/dt = 100A/us		-	45	90	ns
Body diode reverse recovery charge	Q _{rr}			-	56	115	nC
Reverse recovery fall time	t _a			-	27	-	ns
Reverse recovery rise time	t _b			-	18	-	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-2.2	-	A

Notes

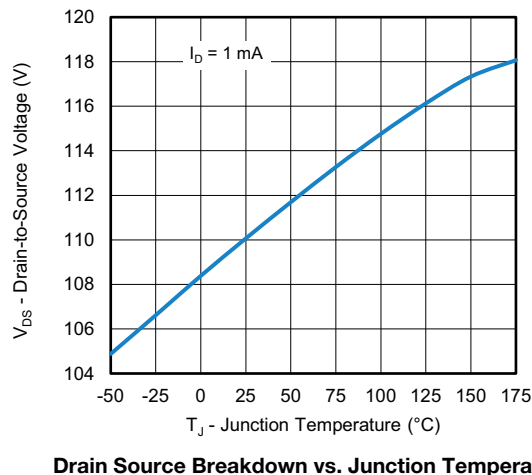
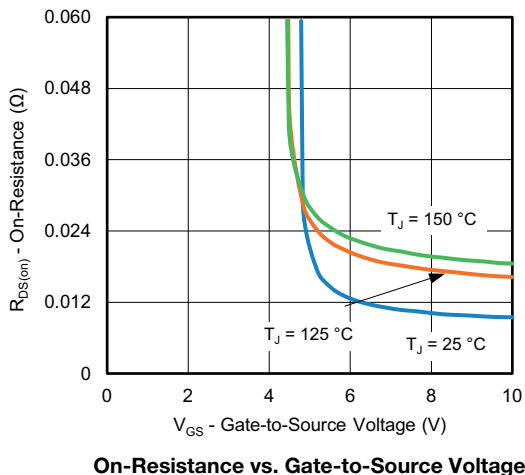
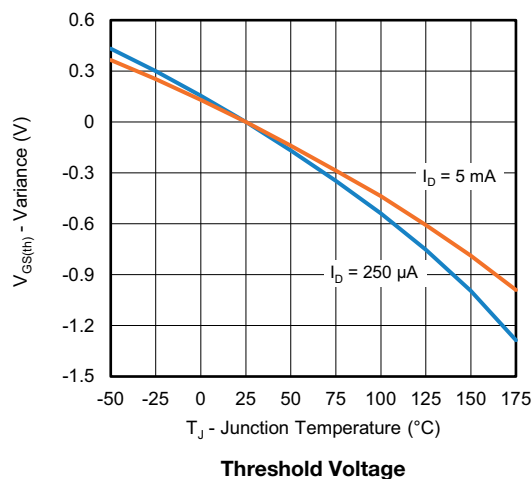
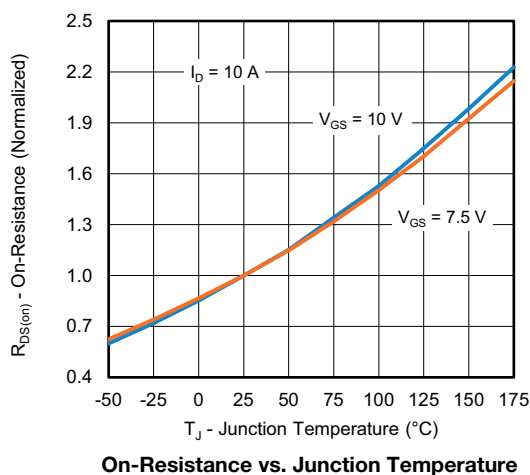
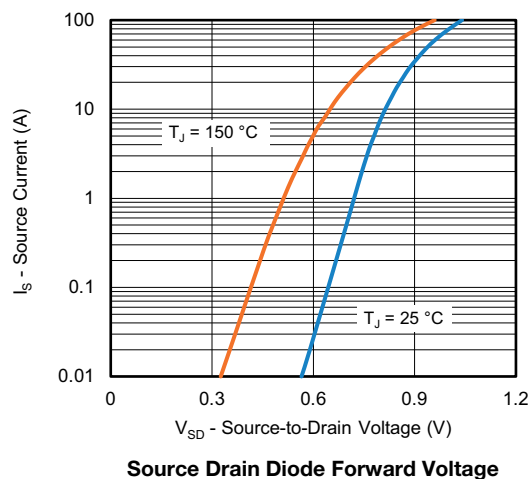
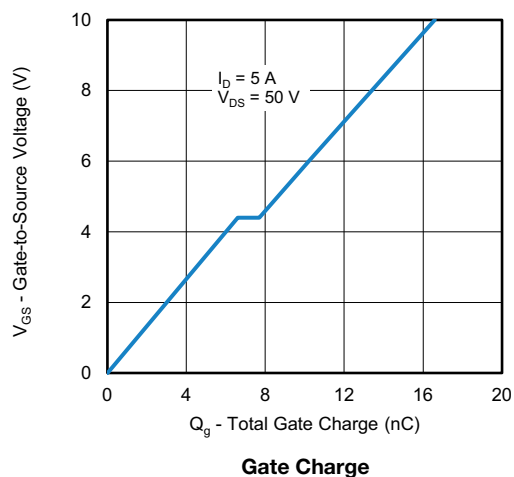
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Capacitance

Transconductance

On-Resistance vs. Drain Current

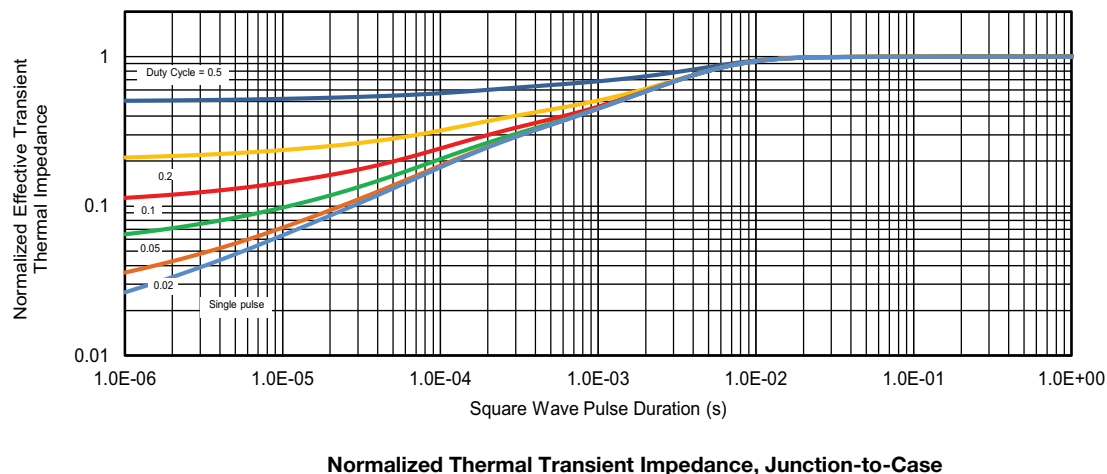


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



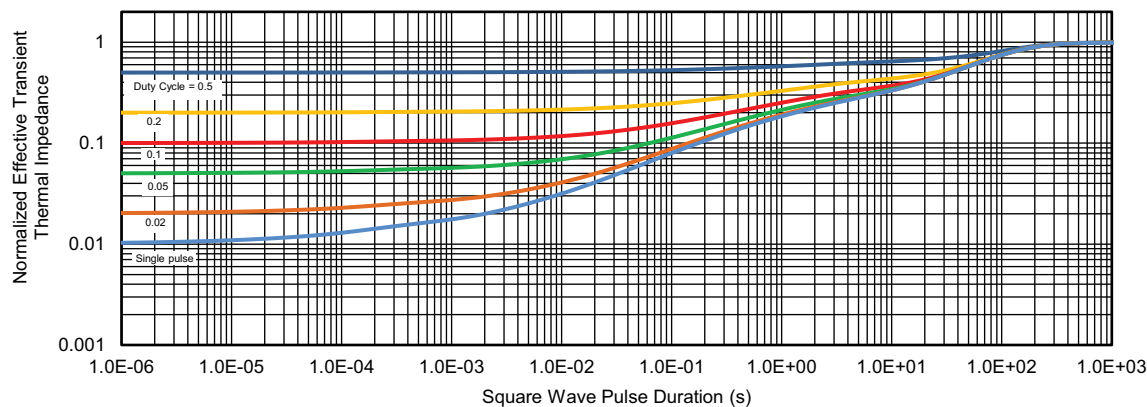


THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)





THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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