18 V, 30 A, 1.2 mΩ $R_{DS(on)}$ Hot-Swap eFuse Switch

DESCRIPTION

This SiC32305 and SiC32306 are a programmable hot swap e-fuses for high current applications such as servers, data storage, and communication products. It contains a high-side MOSFET and other control circuitry that enables it to work as stand-alone device, or to be controlled by a hot-swap controller. SiC32305, SiC32306 drive up to 30 A of continuous current per device.

The SiC32305, SiC32306 limit the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop.

The device offers many features to simplify system designs. It provides an integrated solution for monitoring output current and die temperature, eliminating the need for an external current sensing shunt resistor, power MOSFET, and thermal sensing device.

The SiC32305, SiC32306 detect the power FET gate, source, and drain short conditions, in addition to feedback to the controller trough PGD pin. The parts are available in a PowerPAK MLP28S-44

FEATURES

- 4.5 V to 18 V operating input range
- 25 V guaranteed maximum input tolerance
- 2.3 ms moderate OCP blanking time
- Maximum 30 A continuous output current
- Integrated switch with lower $R_{DS(on)}$ of 1.2 mΩ
- Built-in MOSFET driver
- Integrated current sensing with sense output
- Separate current sensing output used to program over-current value
- Built-in soft start and insertion delay
- Output short-circuit protection
- Over-temperature protection
- Built-in fuse health diagnostics
- Fault status report
- Analog temperature report
- Available in a PowerPAK MLP28S-44 package
- Auto-retry, 1s after fault is removed (SiC32306).

APPLICATIONS

- Hot swap
- PC cards
- Disk drives
- Servers
- Networking

TYPICAL APPLICATION CIRCUIT

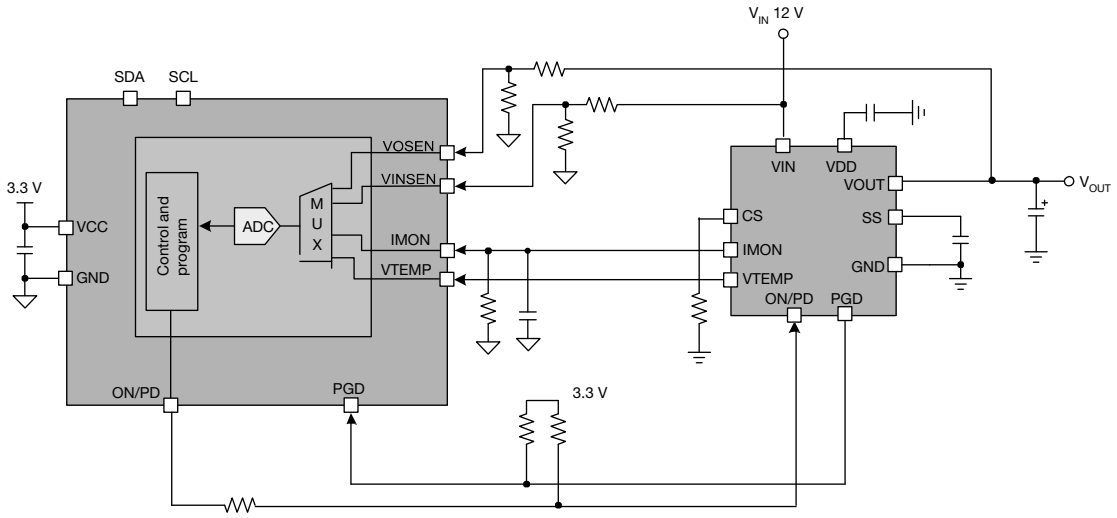


Fig. 1 - Typical Application Circuit

PINOUT CONFIGURATION

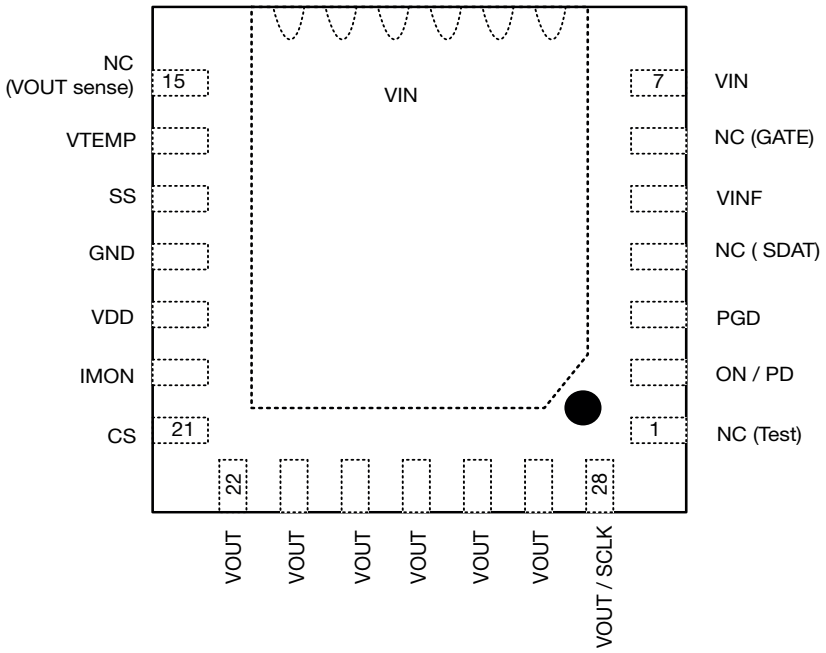
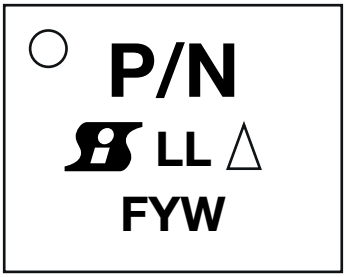


Fig. 2 - Pins Out Configuration (Top View)

ORDERING INFORMATION				
PART NUMBER	**PACKAGE**	**FAULT RESPONSE**	**ALERT PINS**	**MARKING CODE**
SiC32305CD-T5E3	PowerPAK MLP28S-44	Switch off, and latch upon fault event	PGD	32305
SiC32306CD-T5E3	PowerPAK MLP28S-44	Switch off, and auto retry after latch for 1 s upon fault event	PGD	32306
SiC32305EVB	Reference board			
SiC32306EVB	Reference board			

PIN DESCRIPTION		
PIN	**NAME**	**FUNCTION**
1	NC	Can be connected to VOUT, GND, or leave floating (internal test SDAT))
2	ON/PD	Switch on / off control and VOUT pull-down mode control during switch off state. Drive ON / PD high to turn on and low to off the power FET. Setting ON / PD to 1.1 V, the device will be off, and 2ms later, a 500 Ω discharge path to GND is on.
3	PGD	Digital output of Power Good indication. At the initial stage, PGD is set to low by an open Drain output. When VOUT reaches 95 % of VIN, PGD pin will turn high. There is a 5% hysteresis. PGD is hold low at soft start stage. If a fault is detected. PGD is pulled low. This pin has an internal 2 ìA pull-up current to artificially pull the signal high in case the external pull-up resistor is missing. The faults include TJ over temperature, switch health check fault, severe over current, measured current greater than the CS programmed limit for 2.3 ms, and 200 ms soft-start timer expires/soft start failure
4	NC	Connect to GND or leave floating (internal SDAT)
5	VINF	This pin is the power source of the control circuit. It must be connected to VIN. Optionally an appropriate RC filter can be added to the input of this pin to filter noise from the power rail.
6	NC	Leaves floating. Power FET Gate pin.
7	VIN	Input power
8 - 14	VIN	Input power
15	NC (VOUT Sense)	VOUT sense voltage
16	VTEMP	Junction temperature sense output. The output temperature equals 200 mV + 10 mV/C° x T_J°
17	SS	The SS pin is the ramping control for soft-start ramping rate. An internal fixed current source charges an external capacitor in linear fashion. The VOUT voltage soft-starts at a rate that tracks the soft-start capacitor. If soft-start has not completed within 200ms, a fault is declared. In the event that the soft-start ramp is too fast and causes in-rush current to charge VOUT with too much current, the internal soft start current limit reference will override (slow down) the soft-start ramp rate. The ramping voltage on the SS pin will equal 10 % of the VOUT voltage during ramping.
18	GND	Signal ground.
19	VDD	Internal 5 V LDO output. Place a 4.7 µF (minimum 2.2 µF) decoupling capacitor close to VDD and GND.
20	IMON	Current monitor output. The output current is proportional to the current flowing through the power device. The IMON/IOUT gain is 20uA/A.
21	CS	Current sense output. CS requires an external resistor. The VCS voltage is compared with an internal current limit reference voltage to determine the current limit.
22 - 27	VOUT	Output voltage controlled by the IC. OUT is connected to the source of the integrated MOSFET
28	NC	Can be connected to VOUT, GND, or leave floating (internal test SCLK)

MARKING CODE



Format:
- Line 1: part number
- Line 2: Siliconix logo, lot code, and ESD logo
- Line 3: factory code, year code, work week code

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input voltage	V_{IN}, V_{INF}	-0.3	+25	V
Output voltage (DC)	V_{OUT}	-0.3	+25	V
Output negative voltage (10 µs)		-3	-	V
Output negative voltage (500 µs)		-1	-	V
Internal 5 V LDO output	V_{DD}	-0.3	-0.3 to +6	V
All other pins		-0.3	-0.3 to V_{DD} + 0.3	V
Operating junction temperature range	T_J	-40	+150	°C
Lead temperature	T_{SLD}	-	260	°C
Storage temperature	T_{STG}	-65	+150	°C
Pin 8 ''V_{OUT} Sense'' voltage range		Internally limited		
Pin 4, gate voltage range (V_{GATE} - V_{OUT})		-20	20	V
Maximum continuous switch current		-	30	A
Electronstatic discharge, human body model (per EIA/JESD22-A114)	ESD_{HBM}	-	2	kV
Electronstatic discharge, charge device model (per EIA/JESD22-A115)	ESD_{CDM}	-	1.5	kV
Maximum latch-up current limit (per JESD78 class II)	I_{LU}	-	100	mA
Moisture sensitivity level	MSL	Level 1		
Storage	T_{STG}	-55	+125	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

PARAMETER	MIN.	TYP.	MAX.	UNIT
Input voltage (V_{IN})	4.5	-	18	V
Maximum continuous output current	-	-	30	A
V_{DD} output capacitance range	2.2	-	10	µF
Operation junction temperature	-40	-	+125	°C

THERMAL CHARACTERISTICS

THERMAL PARAMETER	SYMBOL	VALUE	UNIT
Thermal resistance, junction to ambient	$R_{\theta JA}$	17	°C/W
Thermal resistance, junction to case, V_{OUT} lead	$R_{\theta JCL}$	1.9	°C/W
Thermal resistance, junction to case, center of exposed pad	$R_{\theta JCB}$	1	°C/W

Note

- Thermal resistances are obtained by measurement with part mounted on evaluation board

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS V_{IN} = V_{INF} = 12 V, ON / PD = 3.3 V, CVINF = 0.1 µF, CVDSS = 4 µF, CVTEMP = 0.1 µF, RVTEMP = 1 kΩ, CSS = 100 nF, MIN. / MAX. LIMITS ARE OVER THE JUNCTION TEMPERATURE RANGE OF -40 °C TO +125 °C UNLESS SPECIFIED OTHERWISE, TYP. VALUES AT T_A = 25 °C	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Supplies Current						
Quiescent current	I_Q	V_{ONPD} = 3 V, no load	-	3	-	mA
		Fault latch off	-	6.3	-	mA
		V_{ONPD} = 0 V	-	6	-	mA
V_{DD} Regulator and UVLO						
Regulator output voltage	V_{VDD}	I_{VDD} = 0 mA, V_{INF} = 6 V	-5%	5	5%	V
V_{DD} current limit			-	70	-	mA
V_{DD} drop out voltage		V_{INF} = V_{IN} = 4.5 V, I = 20 mA	-	200	-	mV
UVLO threshold, rising			-	4.2	-	V
UVLO threshold hysteresis			-	73	-	mV
V_{IN} Under Voltage						
V_{IN} under voltage lockout threshold rising	V_{VIN_THR}		-	4.2	-	V
V_{IN} under-voltage lockout hysteresis	V_{VIN_THF}		-	105	-	mV
ON / PD						
Internal current source	I_{ON_PD}		3	4.2	5	µA
FET on insertion delay time	t_{ON_DLY}	**Note:** 1 ms timer begins after ON_PD pin transitions above 1.4 V	-	1	-	ms
FET on high-level input voltage	V_{ON_Hi}		1.7	-	-	V
FET on-state hysteresis	V_{ON_Hyst}		-	350	-	mV
PD mode pull-down resistor	R_{PL_DN}	Internal resistor from V_{OUT} to ground through PD controlled functionality	-	650	-	Ω
PD mode pull-down delay time	$t_{PL\_DN\_DLY}$	**Note:** This 2.08 ms is the summation of the 80 µs recognition time and 2 ms delay time	-	2.05	-	ms
Soft-Start						
Pull-up current	I_{SS}	T_J = 25 °C	4.5	5	5.5	µA
Gain to V_{OUT}	AVSS	-	8.3	10	12.4	V/V
SS pulldown voltage	V_{OL_SS}	0.1 mA into pin during ON delay	-	5.9	-	mV
Auto-retry delay (SiC32306)	t_{DLY_RETRY}	Auto elay from power-down to retry of startup	-	1	-	S
PGD Output						
Output low current capability	I_{PGD_ACTIVE}	V_{PGD} = 0.2 V	18	32	-	mA
PGD off-state leakage current	I_{PGD_LKG}	V_{PGD} = 5 V **Note:** There is an intentional internal 2 MΩ pull down resistor	-	2.7	-	µA

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS V_{IN} = V_{INF} = 12 V, ON / PD = 3.3 V, CVINF = 0.1 µF, CVDSS = 4.7 µF, CVTEMP = 0.1 µF, RVTEMP = 1 kΩ, CSS = 100 nF, T_J = 25 °C	LIMITS			UNIT
			MIN.	TYP.	MAX.	
I_{MON}						
Sense gain			-	20	-	µA/A
I_{MON} accuracy (1)	I_{MON_ACC}	0.25 A ≤ I_{OUT} ≤ 3 A, T_J = 25 °C	I_{OUT} - 0.5	-	I_{OUT} + 0.5	A
		I_{OUT} = 3 A, T_J = 25 °C	-3	-	+3	%
		I_{OUT} = 10 A, T_J = 25 °C	-3	-	+3	%
		I_{OUT} = 30 A, T_J = 25 °C	-3	-	+3	%
		3 A ≤ I_{OUT} ≤ 30 A, T_J = 0 to 85 °C	-5	-	+5	%
Short - Circuit Protection						
Short-circuit current trip point (1)	I_{SC}		-	100	-	A
Response time (1)	t_{SC}		-	200	-	ns
Over Current Protection						
Internal CLRef voltage			-	1.6	-	V
OCP blanking time			-	2.3	-	ms

Notes

(1) Guaranteed by design and characterization
(2) Typical limits are established by characterization and are not production tested
(3) Min. and Max. Parameters are not 100% production tested

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS V_{IN} = 12 V, V_{DD}, = 5.0 V, T_J = 25 °C, unless otherwise noted	LIMITS MIN. (3)	LIMITS TYP. (2)	LIMITS MAX. (3)	UNIT
VTEMP						
Sense Gain		Sense range 0 °C to 140 °C	-	10	-	mV / °C
Sense Offset		T_J = 25 °C (V_{TEMP} = 200 mV + T_J x 10 mV/C°)	-	450	-	mV
Thermal Shutdown						
Thermal shutdown temperature	T_{THDN}	PGD pulls low	-	142	-	°C
Power MOSFET						
On resistance	$R_{DS(on)}$		-	1.08	1.6	mΩ
		T_J = 85 °C	-	1.25	-	mΩ
FET Health Diagnostic (Fault Detection)						
FET VDS short threshold	V_{SCTH_DS}	Startup postponed if V_{OUT} > V_{SCTH_DS} anytime after postponed **(Note: this is a non-latching fault)**	-	80	-	%
FET VDS short release threshold. (short flag removed threshold)	V_{DS_OK}	Startup resumed if V_{OUT} < V_{DS_OK} anytime after postponed	-	70	-	%
FET gate to drain short threshold	V_{SCTH_DG}	Startup postponed if V_G is less than V_{SCDG_TH} at V_{ON} > V_{ON_HI} transition. It will resume once it is below V_{DG_OK} **(Note: this is a non-latching fault)**	-	2.7	-	V
FET gate to drain short OK threshold	V_{DG_OK}	Startup resumed if V_G < V_{DG_OK} anytime after postponed	-	2.6	-	V
VG low threshold	V_{G_TH}	Restart / latch if V_{GD} < V_{G_TH} after t_{SS_MAX}. During normal operation, it will be a flag and triggers restart / latch	-	7	-	V
V_{OUT} low threshold	V_{OUTL_TH}		-	90	-	%
FET maximum gate fault timer	t_{gf_max}	After ON / PD goes high, if V_{GS} remains low for longer than 200 ms **(Note: this fault causes PGD to latch)**	-	200	-	ms
Maximum soft-start time	t_{SS_MAX}	After ON / PD goes high, if V_{OUT} < 90 % V_{IN} within 200 ms, or if V_{GS} remains less than 1.5 V below internal charge pump voltage (indication of fuse not fully on) within 200 ms **(Note: this fault causes PGD to latch)**	-	200	-	ms

Notes

(1) Guaranteed by design and characterization

(2) Typical limits are established by characterization and are not production tested

(3) Min. and Max. Parameters are not 100% production tested

FUNCTIONAL BLOCK DIAGRAM

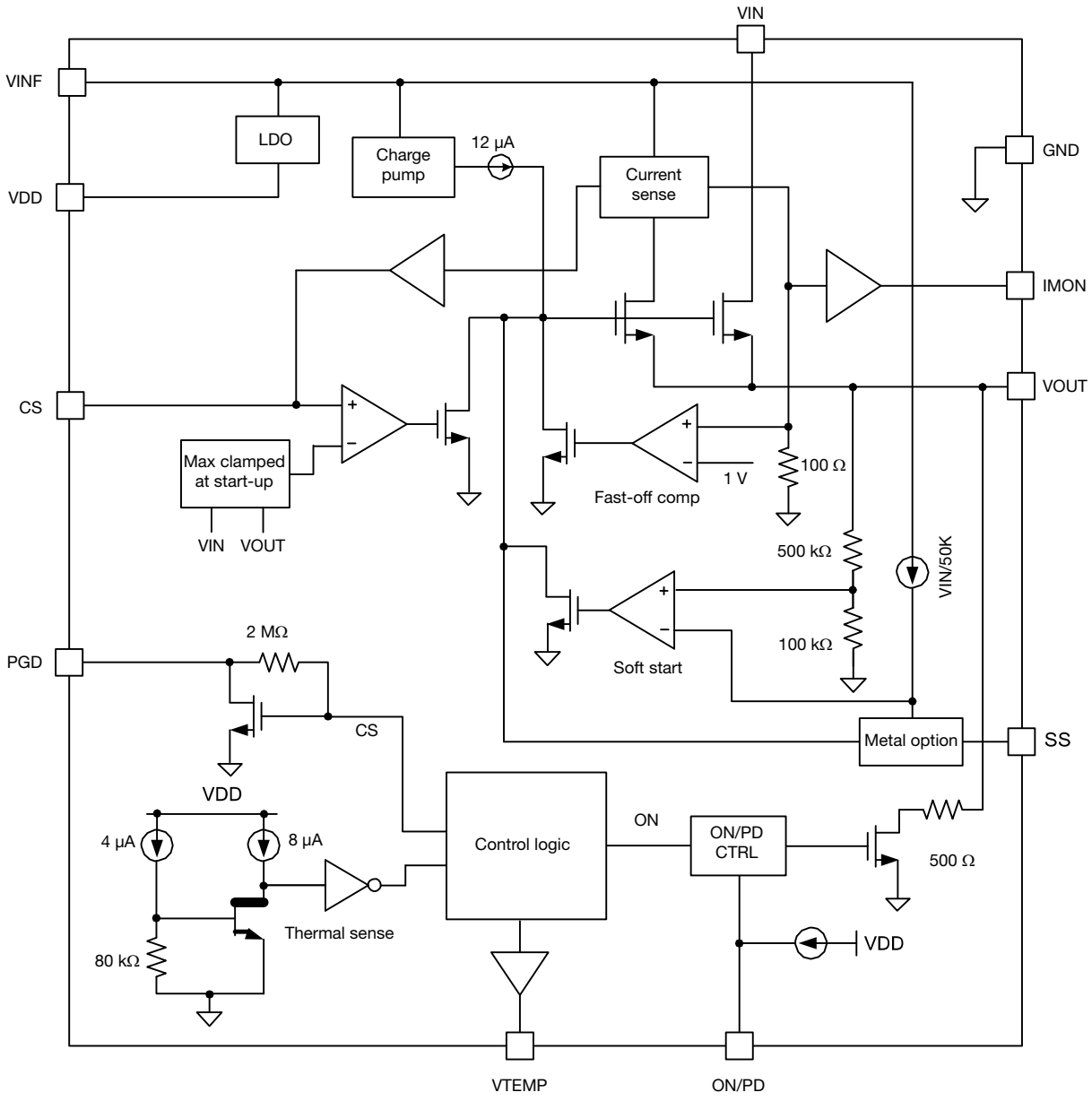


Fig. 3 - Functional Block Diagram

TYPICAL CHARACTERISTICS (Test conditions: V_{IN} = 12 V, C_{SS} = 220 nF, RCS = 2 kΩ, RCLREF = 120 kΩ, RCS = 2 kΩ, RIMON = 2 kΩ, T_A = 25 °C, unless otherwise specified)

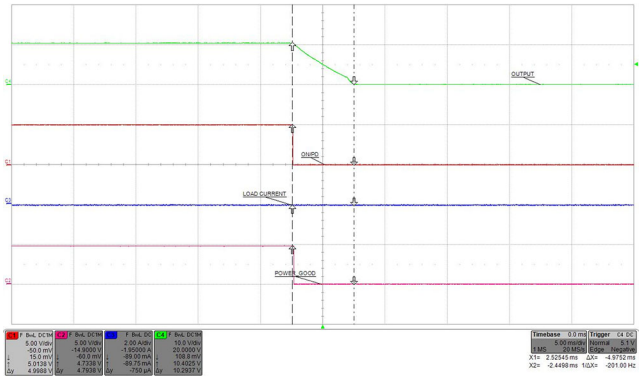


Fig. 4 - Shut down by EN (I_{OUT} = 0 A), Time: 5 ms/Div

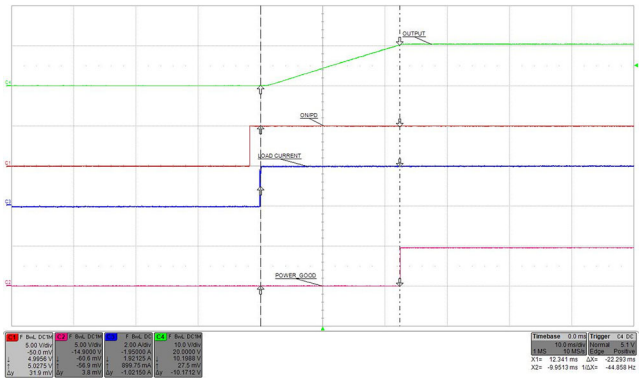


Fig. 7 - Start Up by EN (IOUT = 0 A), Time: 10 ms/Div

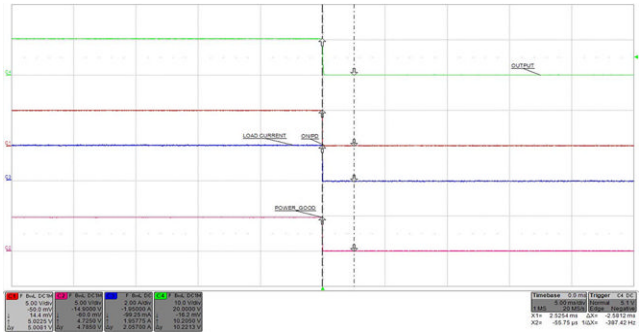


Fig. 5 - Shut down by EN (I_{OUT} = 2 A), Time: 5 ms/Div

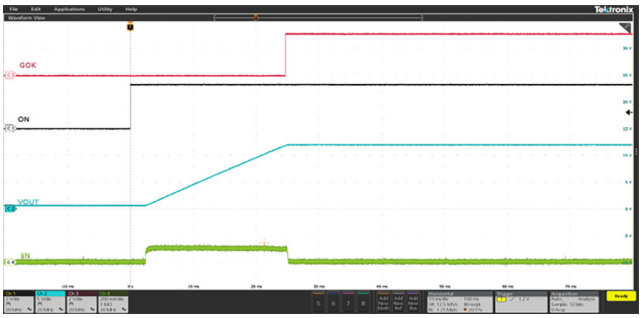


Fig. 8 - Power Up With ON-PD Control (COUT = 2 x 220 µF), Time: 10 ms/Div.

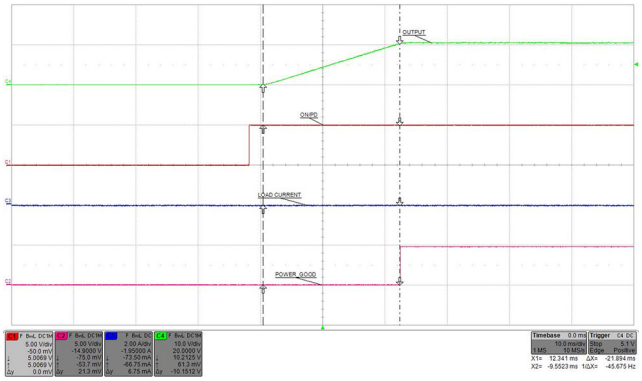


Fig. 6 - Start Up by EN (I_{OUT} = 0 A), Time: 10 ms/Div

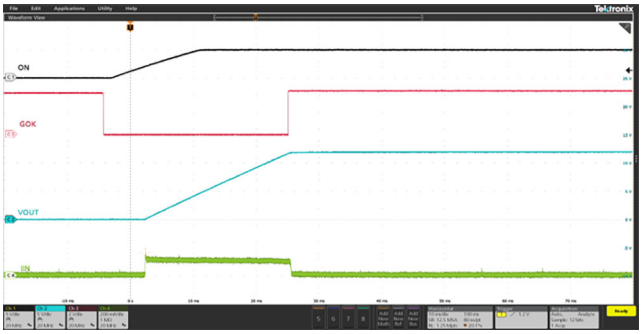


Fig. 9 - Power Up With V_{IN} (COUT = 2 x 220 µF), Time: 10 ms/Div.

TYPICAL CHARACTERISTICS (Test conditions: V_{IN} = 12 V, C_{SS} = 220 nF, RCS = 2 kΩ, RCLREF = 120 kΩ, RCS = 2 kΩ, RIMON = 2 kΩ, T_A = 25 °C, unless otherwise specified)

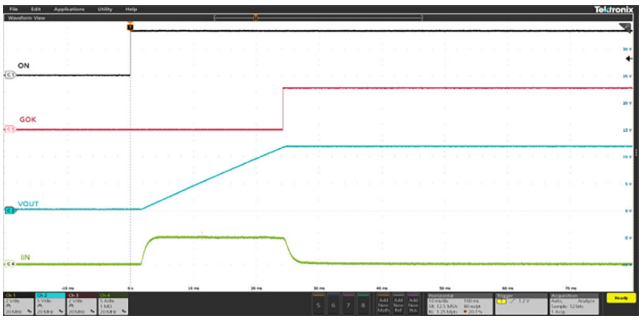


Fig. 10 - Power Up With ON/PD Control (COUT = 10 mF), Time: 10 ms/Div.

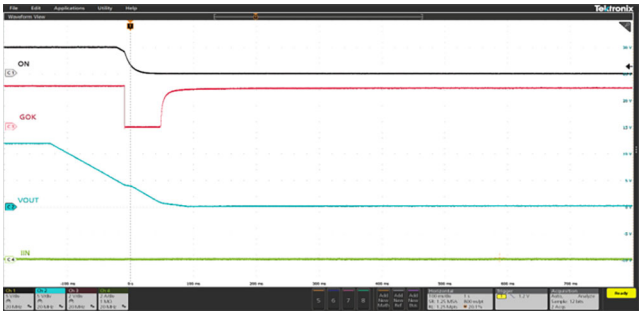


Fig. 13 - Power Down With V_{IN} (COUT = 2 x 220 µF), Time: 10 ms/Div.

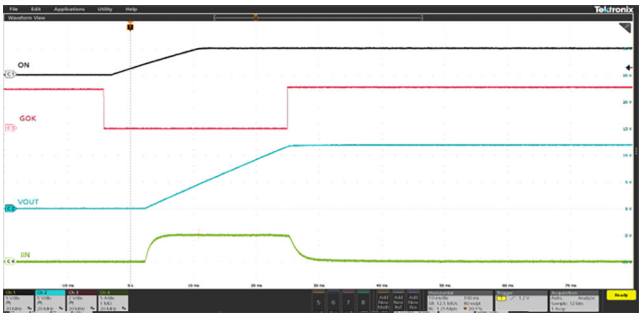


Fig. 11 - Power Up With V_{IN} (COUT = 10 mF), Time: 10 ms/Div.

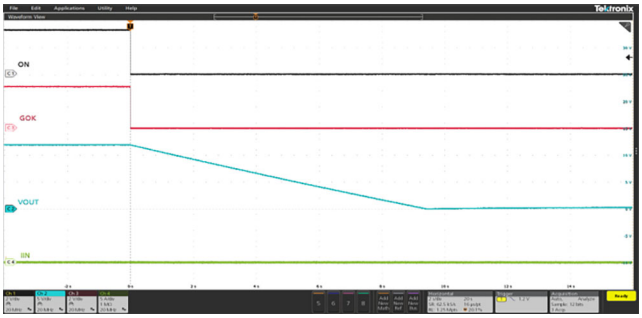


Fig. 14 - Power Down With ON/PD Control (COUT = 10 mF), Time: 2 ms/Div

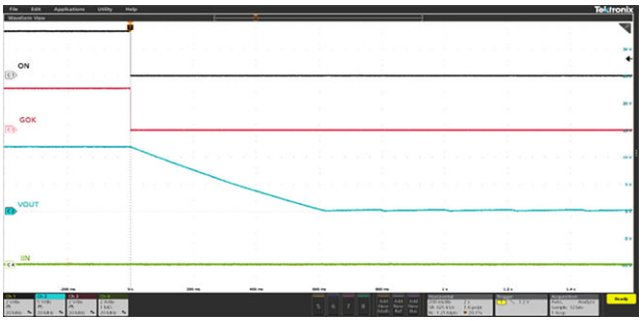


Fig. 12 - Power Down With ON/PD Control (COUT = 2 x 220 µF), Time: 10 ms/Div.

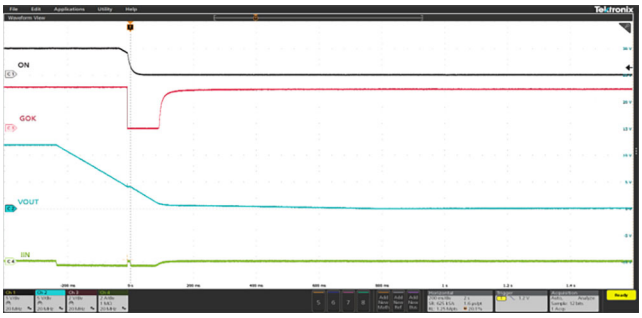


Fig. 15 - Power Down With V_{IN} (COUT = 10 mF), Time: 2 ms/Div

TYPICAL CHARACTERISTICS (Test conditions: V_{IN} = 12 V, C_{SS} = 220 nF, RCS = 2 kΩ, RCLREF = 120 kΩ, RCS = 2 kΩ, RIMON = 2 kΩ, T_A = 25 °C, unless otherwise specified)

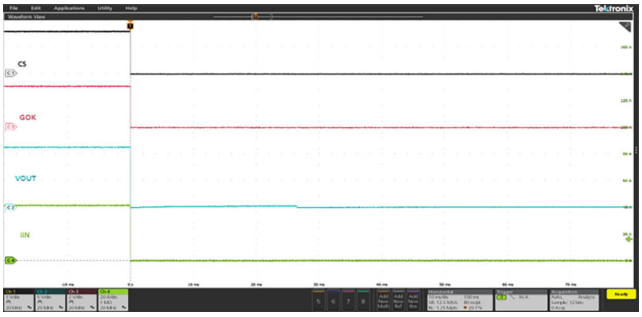


Fig. 16 - Slow OCP During Normal Operation (COUT = 2 x 220 µF), Time: 10 ms/Div.

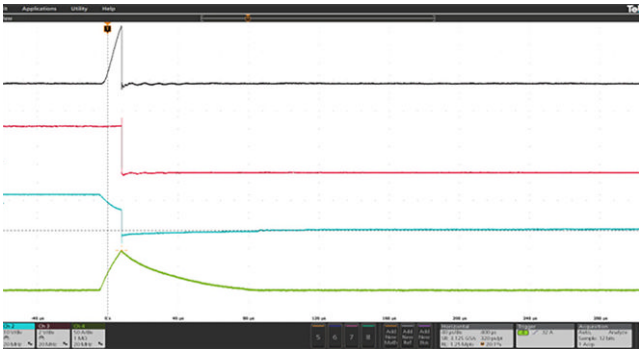


Fig. 17 - Output Short During Normal Operation (COUT = 2 x 220 µF), Time: 40 µs/Div.

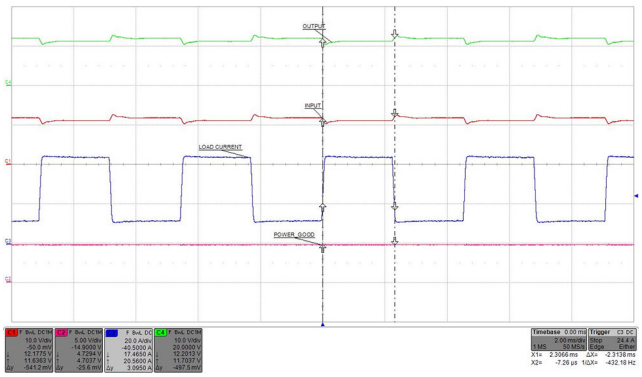


Fig. 18 - 2.3 ms Over Current Blanking During Normal Operation, Time: 2 ms/Div.

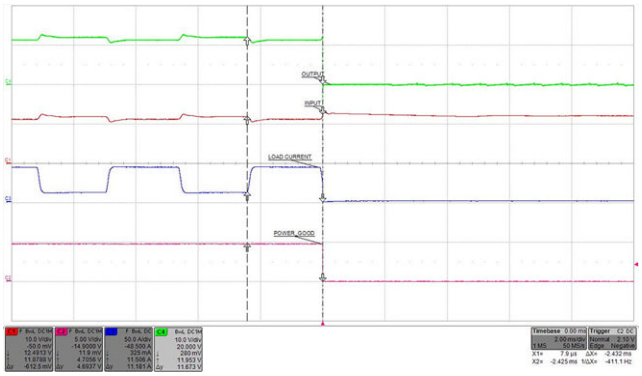


Fig. 19 - Over Current Protection Switch Off after 2.3 ms Blanking During Normal Operation, Time: 2.432 ms

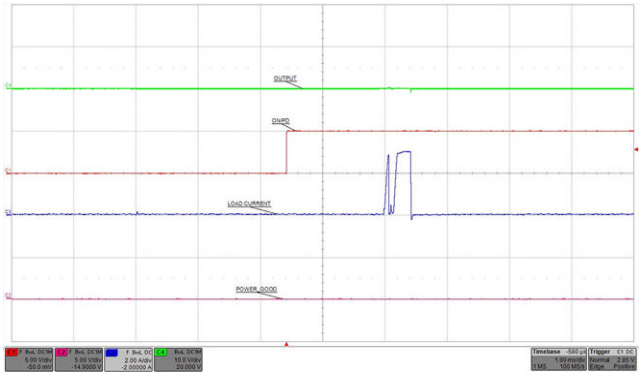


Fig. 20 - Start Up by ON/PD with VOUT Short (IOUT measured before COUT), Time: 1 ms/Div.

DETAILED OPERATIONAL DESCRIPTION

The SiC32305 and SiC32306 integrates a 30 A high-side MOSFET with $R_{DS(on)}$ of 1.2 mΩ, which is suited for hot-swap applications.

The SiC32305 and SiC32306 limits the inrush current to the load when its circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop. It provides an integrated solution for monitoring the output current and the die temperature, eliminating the need for an external current-sensing power resistor, power MOSFET, and thermal sensing device. Also, it provides monitored current and temperature information feedback to the processor or controller. The SiC32305 and SiC32306 limits the internal MOSFET current by controlling the gate voltage through the current limit reference (internal VCLREF) and soft start ramp.

Power-Up Sequence

For hot-swap applications, the input of the SiC32305 and SiC32306 can experience a voltage spike or transient during the hot-plug procedure. This is caused by the parasitic inductance of the input trace and the input capacitor. A fixed 1 ms insertion delay stabilizes the input voltage.

If the SiC32305 and SiC32306 is controlled by a front-end hot- swap controller, there will be a time-on delay before ON / PD can turn on the power FET.

As shown in Fig. 25, the input voltage rises immediately. The power FET GATE voltage should always be pulled low during the V_{IN} plug-in with high dV/dt. The internal LDO output V_{DD} ramps up along with the input voltage. If the SiC32305 and SiC32306 co-operates with the hot-swap controller, the V_{DD} output can be used to power up the hot-swap controller.

The power FET remains off until the ON / PD signal is pulled high. When the ON / PD signal becomes high and the 1 ms insertion delay time ends, the power FET is charged up by the internal 12 µA charge pump under the supervision of the soft-start control loop and the CLREF current limiting loop, which itself is a function of the V_{OUT}/V_{IN} voltage ratio, or alternately, the DAC output of a controller.

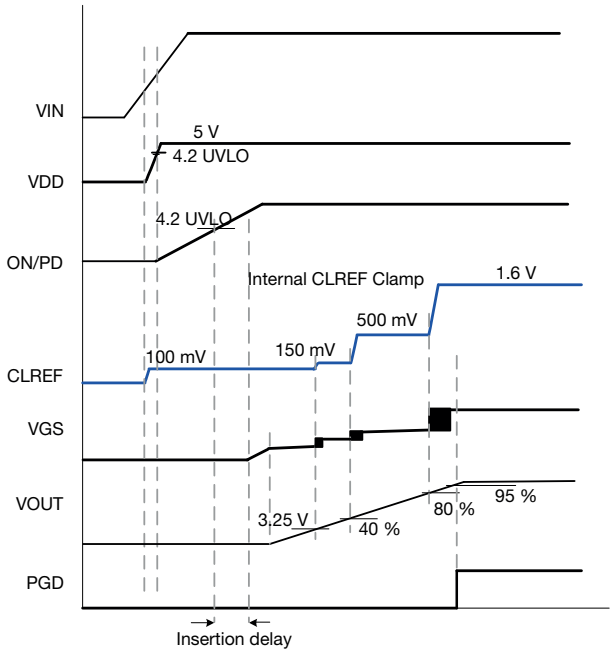


Fig. 21 - Start-Up Sequences Between SiC32305/6 and Front-End Controller

If the SiC32305/6 work as stand-alone devices (see Fig. 26), an external capacitor C_{ON} can be connected from ON / PD to ground for an automatic start-up. The internal 4.2 µA current source charges the capacitor when V_{DD} is higher than UVLO. Also, ON / PD can be pulled up externally to the V_{DD} voltage. An internal current limit reference voltage (VCLREF) determines the current limit level.

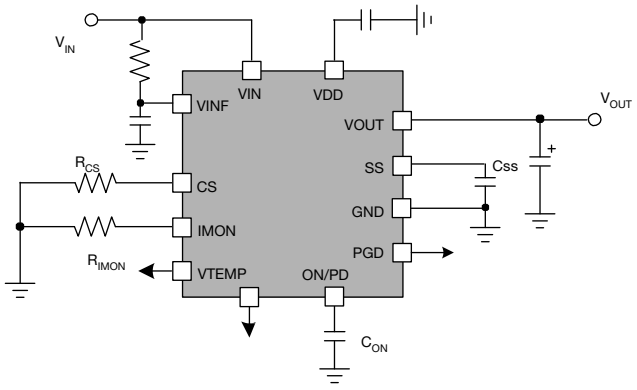


Fig. 22 - Standalone Operating Schematic

Current Limit at Start-Up

The SiC32305 and SiC32306 load current is limited by the VCLREF. The CS voltage is compared with the CLREF voltage through an OTA amplifier to regulate the power FET gate. This prevents the switch current from exceeding the CLREF defined current limit. The CLREF voltage is set per VOUT / VIN ratio during start-up to lower the current clamping level therefore lower power dissipation. Once V_{OUT} is ramped close to V_{IN}, the VCLREF can be raised to the full current limit, the power FET gate is fully enhanced, and the system is ready to draw power from the input.

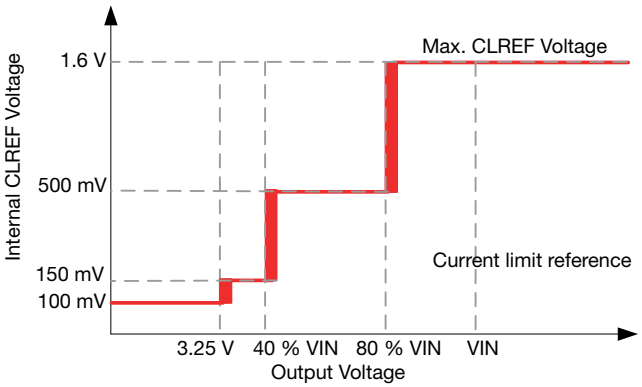


Fig. 23 - Internal Current Limit Reference Voltage (VCLREF) vs. V_{OUT}

As shown in Fig. 27, in order to protect the device from overheating during start-up, a maximum current limit is included during start-up. When V_{OUT} is less 3.25 V, the internal VCLREF is clamped at 100 mV. When V_{OUT} is between 3.25 V and 40 % of V_{IN}, the VCLREF is clamped at 150 mV. When V_{OUT} is between 40 % and 80 % of V_{IN}, CLREF is clamped at 500 mV. When V_{OUT} is > 80 % V_{IN}, CLREF is clamped to 1.6 V.

The desired start-up current limit is a function of the CS resistor RCS. The CLREF voltage is calculated with equation (1):

$$I_{LIMIT\_SS} = \frac{V_{CLREF\_SS}}{CSgain \times R_{CS}} \quad (1)$$

Where V_{CLREF_SS} is the internal reference voltage at start-up. Then the V_{OUT} power-up ramp time can be approximately estimated with equation (2):

$$t_{RAMP} = \frac{V_{IN}}{I_{LOAD}} \times C_{OUT} \quad (2)$$

The V_{OUT} ramp time varies with the load condition and the output capacitor (C_{OUT}) while adopting the VCLREF current limit during start-up. Please refer to design calculator for circuit setting.

A capacitor connected to SS determines the soft-start time. When ON / PD is pulled high, a constant-current source ramps up the voltage on SS. The output voltage rises at aproximately ten times the SS slew rate. The SS capacitor can be set larger to increase the soft-start time.

During start-up, if the CS voltage reaches VCLREF, the power FET gate-to-source voltage is regulated to hold the FET current constant. If the over current clamp condition lasts for 250us, the switch is turned off. If the power FET remains on while the V_{OUT} remains lower than 90 % V_{IN} within the 200 ms maximum soft-start time, the power FET is shut down when the 200 ms time ends (see Fig. 28).

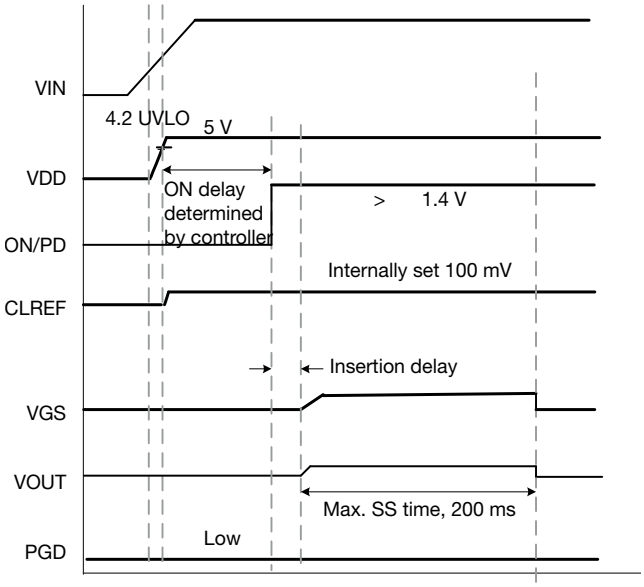


Fig. 24 - Start-Up at Fault

Normal Operation

When the output voltage has ramped up higher than 80 % V_{IN}, the VCLREF voltage will be allowed to operate at full value, 1.6 V.

Once V_{OUT} has completed ramping, the charge pump will drive V_{GS} of the power FET to a fully enhanced phase. Fault supervision circuits will continue to monitor the need for corrective action.

Current Limit at Normal Operation

During normal operation, if the CS voltage exceeds VCLREF voltage for more than 2.3 ms, the switch will be turned off, and the PGD flag will latch. During this 2.3 ms window, the V_{GS} of the power FET remains fully enhanced unless short circuit or over-temperature fault is detected. No current limiting occurs during this 2.3 ms interval. If the PGD pin latches, the power supply or ON / PD of SiC32305 will require cycling to clear the latch.

The desired OCP threshold at normal operation is a function of the CS resistor (R_{CS}). The threshold should be higher than the normal maximum load current, allowing the tolerances in the current sense value. The current limit can be set using equation (5):

$$I_{LIMIT} = \frac{V_{CLREF}}{CSgain \times R_{CS}}$$

Where V_{CLREF} is the voltage of CLREF in normal operation, which is 1.6 V.

CSgain is 20 µA/A. For example, for V_{CLREF} = 1.6 V, R_{CS} = 2.7 kΩ; the desired current limit is 30 A at normal operation.

Short-Circuit Protection

Regardless of the programmed OCP setting level, if a current greater than 100 A is observed, the power FET V_{GS} is forced to turn off rapidly (typically within 200 ns) and the PGD fault will be latched.

SiC32305 will be latched off where as SiC32306 Auto retry 1s after fault is removed.

Auto-Retry Restart (SiC32306):

During short-circuit, overcurrent, or overtemperature faults, the FET turns off and auto-retries to restart after a 1-second delay.

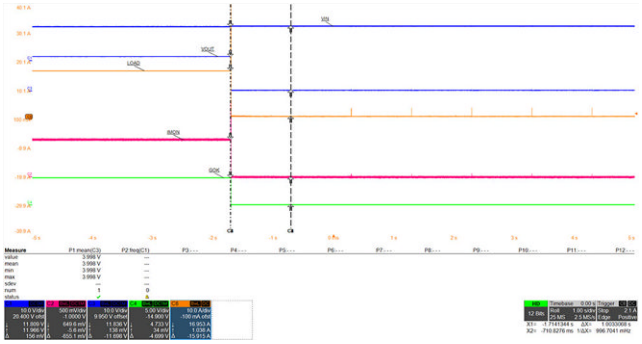


Fig. 25 - SiC32306 Auto Retry after 1 s during short circuit at the outputs

ON / PD Control

ON / PD is used to control both the on/off of the internal power FET and the pull-down mode of the output voltage. When ON / PD is used for power FET on / off control, the FET is turned on if the ON / PD voltage is higher than 1.4 V. If the ON / PD voltage is lower than 1.2 V, the FET is turned off. If ON / PD is used for V_{OUT} pull-down mode, the ON / PD voltage should be driven to aproximately 1.1 V for more than 80 µs. The device recognizes 0.8 V < ON / PD < 1.2 V as a special state that requires pulling down V_{OUT}.

The ON / PD has a fixed 1 ms insertion delay after V_{DD} and V_{IN} have passed the UVLO threshold. All fault functionality is operative during the insertion delay, a fault is detected, PGD will remain low and device won't start up. If a non-latching fault self-clears, then a 1 ms timer will begin once the ON_PD pin is above 1.4 V. When V_{IN} is below the UVLO threshold an internal 1 MΩ pull down resistor will attempt to discharge the ON_PD pin. Once V_{IN} UVLO is cleared, the pull down resistor is disabled and the 4.2 µA charge current is enabled.

Once the ON / PD voltage is pulled higher than 1.4 V, and the 1 ms insertion delay ends, the internal charge pump charges the power FET's GATE. Once the GATE voltage reaches its threshold (V_{GSTH}), the power FET turns on (Fig. 29). The output voltage rises following the soft-start control loop retarding the Gate voltage until V_{OUT} is sufficiently charged. This limits the power FET in-rush current.

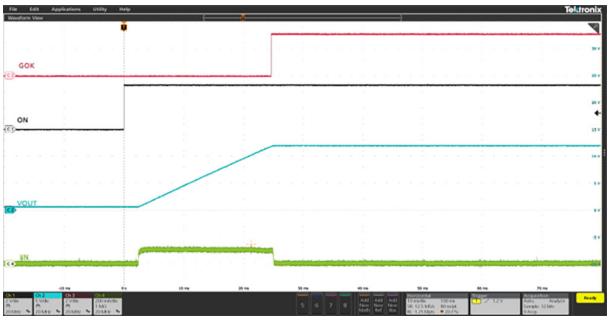


Fig. 26 - Power FET On / Off Control by ON / PD When no Fault Occurs

If the SiC32305 works in stand-alone mode, a capacitor on ON / PD can be used for automatic start-up by the internal 4.2 µA pull-up current source. Once the ON / PD voltage reaches its turn-on threshold, the power FET Gate is charged by the internal charge pump.

When the ON / PD voltage is set to around 1.1 V for more than 80 µs, devices enter in pull-down mode (see Fig. 31). In pull-down mode, an integrated 625 Ω pull-down resistor discharges the output after a fixed delay time (2 ms). If the ON / PD signal is pulled low directly, the pull-down mode is disabled, and the switch output voltage discharges through the external load.

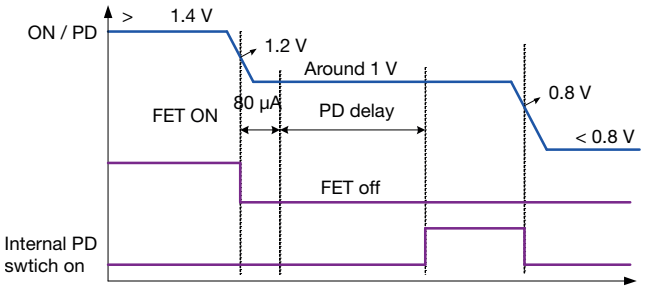


Fig. 27 - PD Mode Control by ON / PD

The connection of ON / PD shown in Fig. 31. controls ON / PD through a resistor divider from the controller. For example, choose R_{ON} =100 kΩ. If ON / PD is only used for the power FET on / off control, the resistor R_{PD} can be set to 0 Ω. Pull-down mode can be set by selecting a 22 kΩ R_{PD} resistor. ON / PD is set to around 1 V by the external resistor divider and the ON / PD internal 4.2 µA current source.

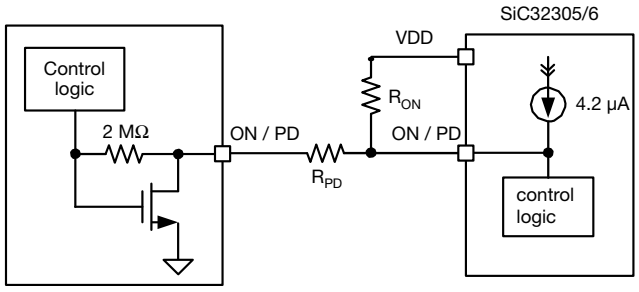


Fig. 28 - ON / PD Connection

PGD Report

PGD is an open-drain, active-low signal which reports the eFuse status. When a fault occurs, or VOUT is below VTH_PGD, PGD is pulled low.

Pull up PGD to the V_{DD} voltage through a 100 kΩ resistor. During the V_{DD} power-up, the PGD output is driven low. Before the power FET is turned on, the PGD fault state is checked during the ON / PD 1 ms insertion delay. All fault functionality is operative during the insertion delay time.

PGD flags the following fault events:

1. Over-current protection: when the CS voltage exceeds the CLREF threshold during normal operation, the PGD is pulled low and latches after a 2.3 ms moderate over-current blanking time
2. Short-circuit protection: when the load current reaches 100 A, short circuit current threshold rapidly, PGD is pulled low immediately and latches
3. The integrated power FET D-S, G-D, and G-S short detection: detailed performance characteristics can be reviewed in the “Damaged Integrated Power FET Detection” section. Although these faults cause PGD either to pull low immediately, or stays low, the PGD pin does not latch unless the 200 ms soft start timer expires.
4. Over-temperature protection at junction temperature TJ > 142 °C: once a fault is detected PGD is pulled low and latches. Over-temperature protection hysteresis is 20 °C.

The release of the fault latch can be accomplished by recycling V_{IN} or by toggling ON / PD.

Fig. 32 shows the FET on / off control with the PGD timing diagram.

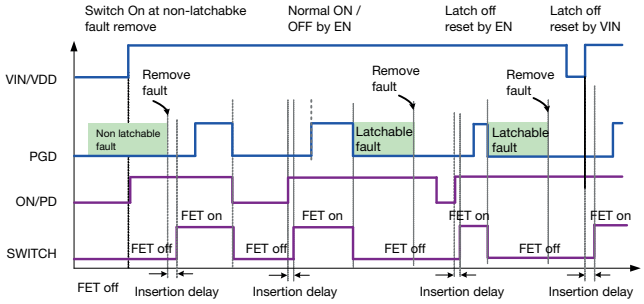


Fig. 29 - FET On / Off Control With PGD Timing Diagram

Damaged Integrated Power FET Detection

Damaged integrated power FET detection includes FET drain-source shorts, gate-drain shorts, and gate-source shorts.

1. D-S short detection during start-up

Once the V_{DD} is higher than the UVLO rising threshold, the controller detects a shorted pass FET during power-up by treating an output voltage that exceeds 70 % x V_{IN} during power up as a short on the MOSFET. Once the short is removed and the controller detects V_{OUT} < 70 % x V_{IN}, and the hot-swap controller prepares for normal start-up.

2. G-D short detection during start-up

The G-D short is detected by monitoring the G-S voltage. During power-up, the controller detects the power FET G-D short by the condition of power FET drain-to-gate voltage (V_{GS} > 2 V). The fault is removed, and the controller detects V_{GS} < 2 V.

3. G-S, G-D short detection during normal operation

When the part operates normally and V_{OUT} remains higher than 90 % of V_{IN}, the controller determines the power FET G-S or G-D short by the V_{CP} - V_{GATE} voltage, where VCP is the internal charge pump voltage. If VCP - VGATE voltage falls belows threshold, the switch is off and PGD pulls low. The fault latch can be cleared by recycling V_{IN} or by toggling ON / PD.

The power FET short faults are listed in Table 1

TABLE 1 - THE POWER FET SHORT FAULTS

FET FAULT		DETECTION CONDITION	PGD FLAG
Start-up FET short	D - S	V_{OUT} > 70 % x V_{IN}	Keep low until V_{OUT} < 70 % x V_{IN}
	G - D	V_{GS} > 2 V	Keep low until V_{GS} < 2 V
Normal operation FET short	G - D / G - S	(V_{CP} - V_{GATE}) > 2 V after 200 ms	Pull low

Input and Output Transient Protection

The hot-swap system experiences positive transients on the input during a hot plug or rapid turn-off with high current due to parasitic inductance in the input circuit.

For input transient protection, a TVS diode (transient voltage suppressor, a type of Zener diode) may be required on the input to limit transient voltages below the absolute maximum ratings.

The output may experience negative transients during rapid turn-off with high current due to inductance in the output circuit. The lowest voltage allowed on the device output is -0.3 V_{DC} and -1 V for 500 µs transient pulse. If a transient makes OUT more negative, the internal ESD Zener diode attached to the pin will become forward biased, and the current will be conducted across the substrate to the ground. The internal ESD diode may not be strong enough to sustain a large current, and the current may disrupt normal operation or, if large enough, damage the part.

An output voltage clamp diode may be required on the output to limit negative transients. Select a Schottky diode with a low forward voltage at the anticipated current during an output short. By doing this, the negative voltage spike at the output terminal can be clamped at less than -0.7 V, thus the IC is protected during a short output.

Current Sense (CS Output)

CS provides a current proportional to the output current (the current through the power device). The gain of the current sense is 20 µA/A.

There is a resistor (R_{CS}) connected from CS to form an external voltage. Use equation (6) and equation (7) to determine a proper reference voltage:

$I_{CS} = I_{OUT}$ x 20 µA/A (6)

$V_{CS} = I_{CS}$ x R_{CS} (7)

Current Monitor (I_{MON} Output)

The gain of the current monitor is 20 µA/A. There is a resistor (R_{IMON}), connected from I_{MON} to ground. The I_{MON} voltage range of 0 V to 1.6 V is required to keep I_{MON}'s output current linearly proportional to the output current use equation (8) and equation (9) to determine a proper reference voltage:

$I_{MON} = I_{OUT}$ x 20 µA/A (8)

$V_{IMON} = I_{MON}$ x R_{IMON} (9)

The current monitor output can be used by the controller to accurately monitor the output current. Place a 100 nF capacitor from I_{MON} to GND to smooth the indicator voltage.

Generally, connect a 2 kΩ resistor (R_{IMON}) to ground to set the gain of the output, which is about 20 mV per ampere. For best accuracy, use resistors within 1 percent.

Temperature Sense Output, V_{TEMP}

V_{TEMP} reports the junction temperature. It is a voltage output proportional to the junction temperature. The V_{TEMP} output voltage is 10 mV/°C with a 200 mV offset. See equation (10):

$V_{TEMP} = T_{JUNCTION}$ x 10 mV/°C + 200 mV (10)

For example, if the junction temperature is 100 °C, the V_{TEMP} voltage is 1.2 V. If V_{TEMP} = 0 V, the junction temperature is about -20 °C. The total temperature sense range is -20 °C to +140 °C. When the junction temperature is below -20 °C, V_{TEMP} remains at 0 V.

Thermal Protection

The device temperature is sensed by monitoring the junction temperature of the IC. The temperature information can be read from V_{TEMP}.

The device itself has thermal protection. When the junction temperature exceeds the threshold (142 °C), the power FET is turned off, and PGD is pulled low.

UVLO Protection

The device has a under-voltage lockout protection feature on V_{DD} exceeds the UVLO threshold. The devices can start up only when V_{DD} exceeds the UVLO threshold. The UVLO protection is non-latching fault.

APPLICATION SCHEMATICS

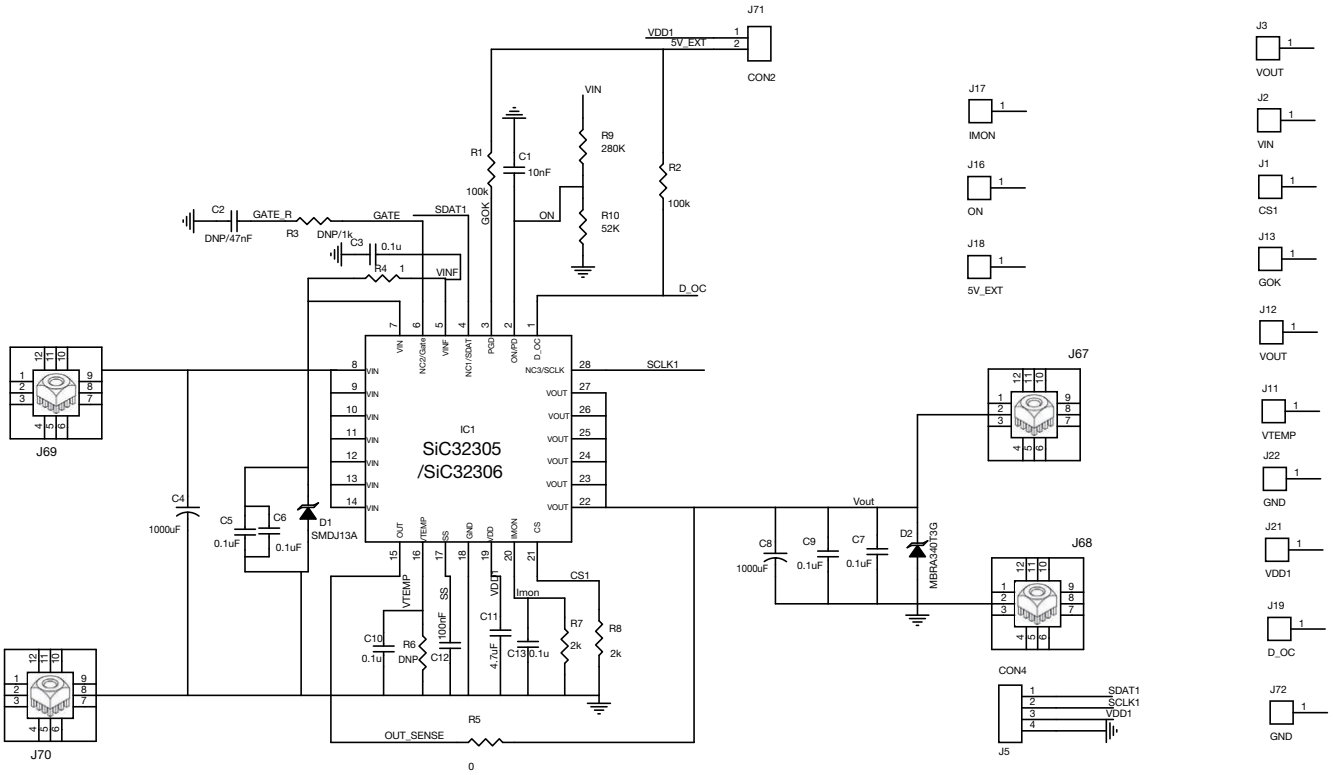


Fig. 30 - SiC32305, SiC3206 Proposed Circuit

The ON pin can interface with micro-processor for on / off and discharge control. Toggling the ON pin will reset the fuse latch. The ON / PD can also be connected to a voltage divider from V_{IN} to set circuit UVLO level.

PRODUCT SUMMARY		
Part number	SiC32305	SiC32306
Description	1.2 mΩ, hot-swap eFuse, I_{MON}, PGD report latch on fault	1.2 mΩ, hot-swap eFuse, I_{MON}, PGD report auto-retry, 1 s after fault is removed
Configuration	Stand alone	Stand alone
Slew rate time (µs)	Adjustable	Adjustable
On delay time (µs)	1000	1000
Input voltage min. (V)	4.5	4.5
Input voltage max. (V)	25	25
On-resistance at input voltage min. (mΩ)	1.2	1.2
On-resistance at input voltage max. (mΩ)	1.2	1.2
Quiescent current at input voltage min. (µA)	2100	2100
Quiescent current at input voltage max. (µA)	2800	2800
Output discharge (yes / no)	Yes	Yes
Reverse blocking (yes / no)	No	No
Continuous current (A)	30	30
Package type	PowerPAK MLP28S-44	PowerPAK MLP28S-44
Package size (W, L, H) (mm)	4 x 4 x 1	4 x 4 x 1
Status code	-	-
Product type	Hot swap, eFuse, slew rate, current report	Hot swap, eFuse, slew rate, current report
Applications	Computers, telecom, industrial	Computers, telecom, industrial

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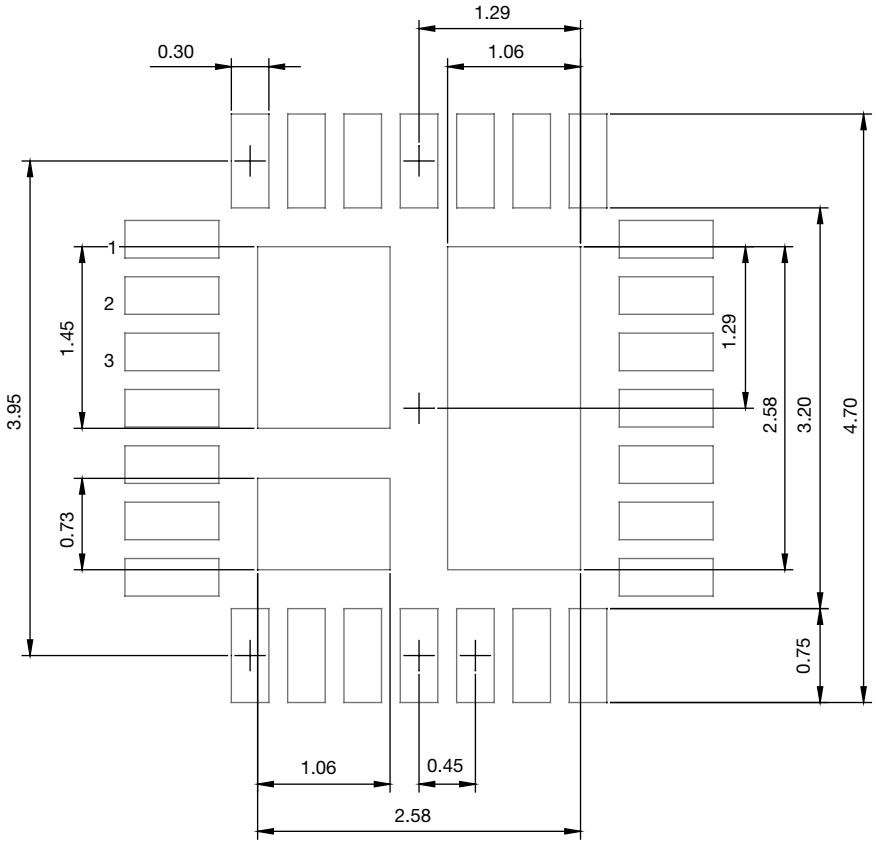
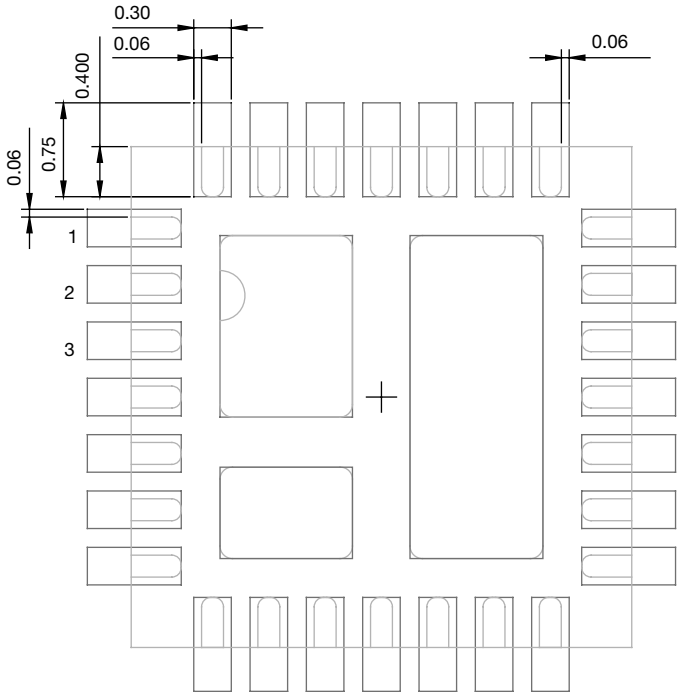
PowerPAK® MLP44-28L Land Pattern

Recommended Land Pattern



Recommended Land Pattern vs. Case Outline



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