

## 60 A VRPower® Integrated Power Stage

### DESCRIPTION

The SiC679 is a high frequency integrated power stage optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance with very low shutdown current. Packaged in Vishay's 5 mm x 5 mm MLP package, SiC679 enables voltage regulator designs to deliver up to 60 A continuous current per phase.

The internal power MOSFETs utilize Vishay's latest TrenchFET® technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

SiC679 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap switch, and user selectable zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V and 3.3 V PWM logic.

The device also supports PS4 mode to reduce power consumption when the system is in standby state.

SiC679 offers operating temperature monitoring, protection features, and warning flags, that improve system monitoring and reliability.

### APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel core processor power delivery
- $V_{CORE}$ ,  $V_{GRAPHICS}$ ,  $V_{SYSTEM\ AGENT}$
- $V_{CCGI}$
- Up to 16 V rail input DC/DC VR modules

### FEATURES

- Highly efficient
  - Thermally enhanced PowerPAK® MLP55-31L package
  - Vishay's latest TrenchFET technology and low side MOSFET with integrated Schottky diode
  - Integrated, low impedance, bootstrap switch
  - Power MOSFETs optimized for 12 V input stage
  - Supports PS4 mode light load requirement with low shutdown supply current
  - Zero current detection for improved light load efficiency
- Highly versatile
  - 5 V and 3.3 V PWM logic with tri-state and hold-off timer
  - 5 V DSBL#, ZCD\_EN# logic with PS4 state support
  - High frequency operation up to 2 MHz
- Robust and reliable
  - Delivers in excess of 60 A continuous current, 70 A, peak (10 ms) and 100 A, peak (10  $\mu$ s)
  - Over current protection
  - Over temperature flag
  - Over temperature protection
  - Undervoltage lockout protection
  - High side MOSFET short detection
- Effective monitoring and reporting
  - Accurate temperature reporting
  - Warnings and faults reporting flag
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### TYPICAL APPLICATION DIAGRAM

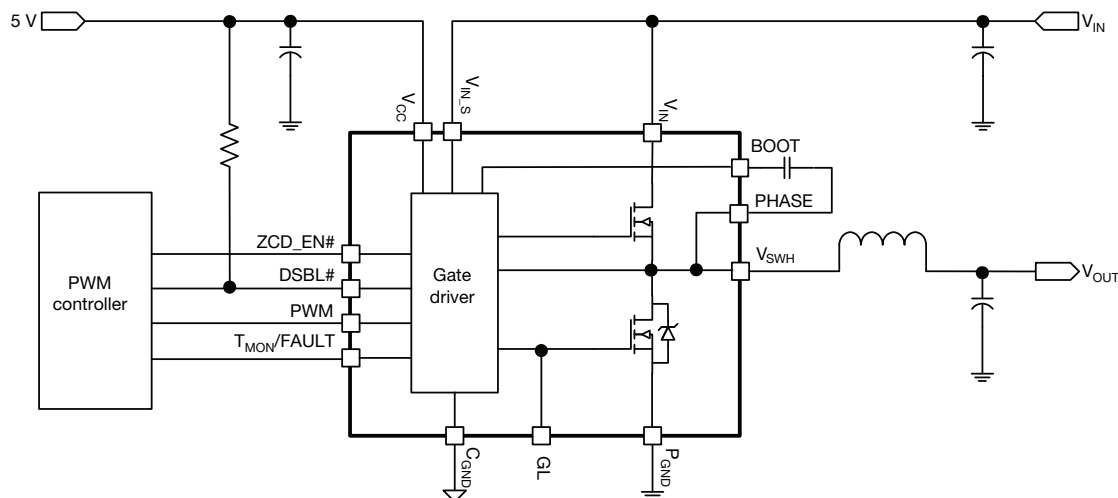
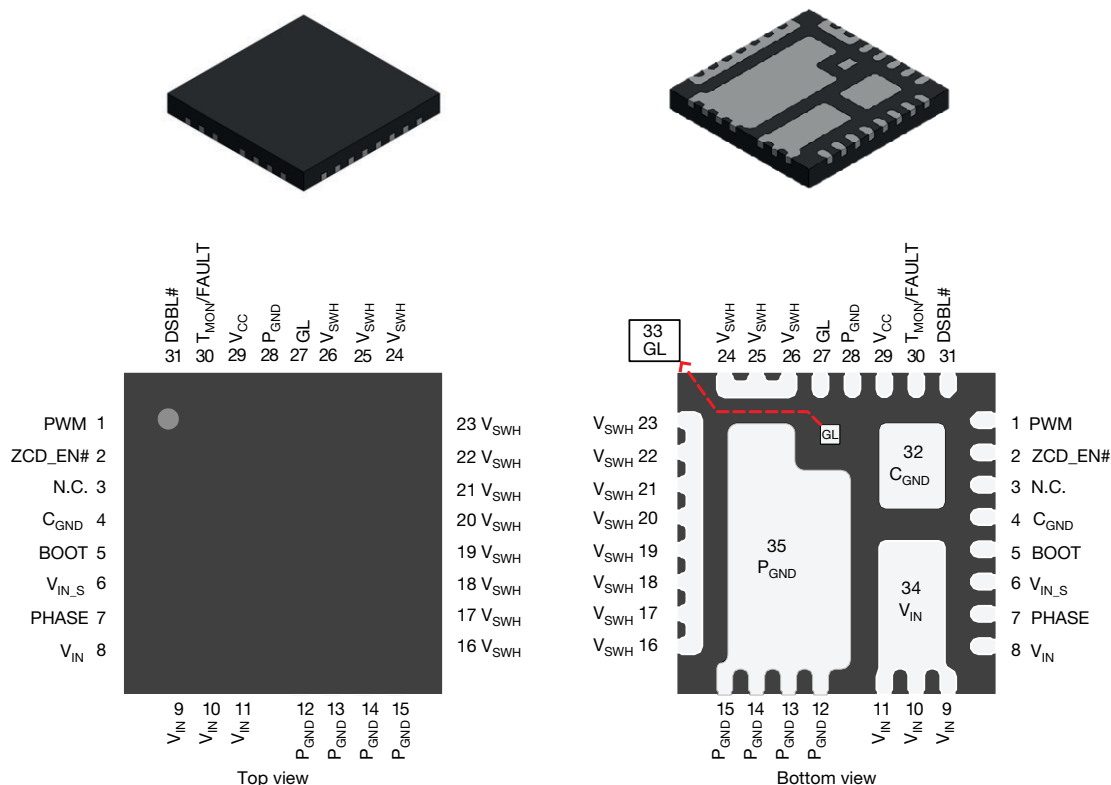
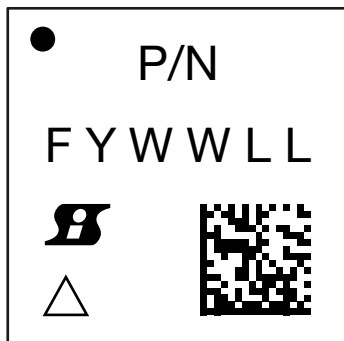


Fig. 1 - Typical Application Diagram

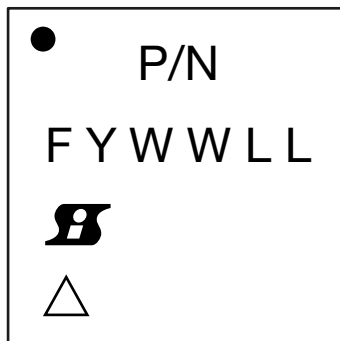
**PINOUT CONFIGURATION**

**Fig. 2 - Pin Configuration**

| PIN CONFIGURATION |                         |                                                                                                                                                                                                                                                                                                                                              |
|-------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIN NUMBER        | NAME                    | FUNCTION                                                                                                                                                                                                                                                                                                                                     |
| 1                 | PWM                     | PWM input                                                                                                                                                                                                                                                                                                                                    |
| 2                 | ZCD_EN#                 | The ZCD_EN# pin enables or disables diode emulation. When ZCD_EN# is LOW, diode emulation is allowed. When ZCD_EN# is HIGH, continuous conduction mode is forced. ZCD_EN# can also be put in a high impedance mode by floating the pin. If ZCD_EN# is floating, the device is placed in a deep sleep state with very low current consumption |
| 3                 | N.C.                    | Not connected                                                                                                                                                                                                                                                                                                                                |
| 5                 | BOOT                    | High side driver bootstrap voltage                                                                                                                                                                                                                                                                                                           |
| 4, 32             | C <sub>GND</sub>        | Analog ground                                                                                                                                                                                                                                                                                                                                |
| 6                 | V <sub>IN,S</sub>       | Over current protection input voltage, connect this pin to power stage input voltage                                                                                                                                                                                                                                                         |
| 7                 | PHASE                   | Return path of high side gate driver                                                                                                                                                                                                                                                                                                         |
| 8 to 11, 34       | V <sub>IN</sub>         | Power stage input voltage. Drain of high side MOSFET                                                                                                                                                                                                                                                                                         |
| 12 to 15, 28, 35  | P <sub>GND</sub>        | Power ground                                                                                                                                                                                                                                                                                                                                 |
| 16 to 26          | V <sub>SWH</sub>        | Phase node of the power stage                                                                                                                                                                                                                                                                                                                |
| 27, 33            | GL                      | Low side MOSFET gate signal                                                                                                                                                                                                                                                                                                                  |
| 29                | V <sub>CC</sub>         | Supply voltage                                                                                                                                                                                                                                                                                                                               |
| 30                | T <sub>MON</sub> /FAULT | Temperature monitor output, FAULT flag output                                                                                                                                                                                                                                                                                                |
| 31                | DSBL#                   | Disable input, active low. If DSBL# is floating, the device is enabled through internal pull-up                                                                                                                                                                                                                                              |

| ORDERING INFORMATION |                    |              |                     |
|----------------------|--------------------|--------------|---------------------|
| PART NUMBER          | PACKAGE            | MARKING CODE | OPTION              |
| SiC679CD-T1-GE3      | PowerPAK MLP55-31L | SiC679       | 5 V PWM optimized   |
| SiC679ACD-T1-GE3     |                    | SiC679A      | 3.3 V PWM optimized |

**PART MARKING INFORMATION**


Marking with 2D code



Marking without 2D code

- = pin 1 indicator
- P/N = part number code
-  = Siliconix logo
- △ = ESD symbol
- F = assembly factory code
- Y = year code
- WW = week code
- LL = lot code
-  = 2D code

**ABSOLUTE MAXIMUM RATINGS**

| ELECTRICAL PARAMETER                      | SYMBOL                            | LIMIT                  | UNIT |
|-------------------------------------------|-----------------------------------|------------------------|------|
| Input voltage                             | $V_{IN}, V_{IN\_S}$               | -0.3 to +24            | V    |
| Control logic supply voltage              | $V_{CC}$                          | -0.3 to +7             |      |
| Switch node (DC voltage)                  | $V_{SWH}$                         | -0.3 to +24            |      |
| Switch node (AC voltage) <sup>(1)</sup>   |                                   | -7 to +35              |      |
| BOOT voltage (DC voltage)                 | $V_{BOOT}$                        | 32                     |      |
| BOOT voltage (AC voltage) <sup>(2)</sup>  |                                   | 40                     |      |
| BOOT to PHASE (DC voltage)                | $V_{BOOT-PHASE}$                  | -0.3 to +7             |      |
| BOOT to PHASE (AC voltage) <sup>(3)</sup> |                                   | -0.3 to +8             |      |
| All logic inputs and outputs              | PWM, ZCD_EN#, DSBL#, T_MON/FAULT  | -0.3 to $V_{CC} + 0.3$ | °C   |
| Max. operating junction temperature       | $T_J$                             | 150                    |      |
| Ambient temperature                       | $T_A$                             | -40 to +125            |      |
| Storage temperature                       | $T_{stg}$                         | -65 to +150            | V    |
| Electrostatic discharge protection        | Human body model, JESD22-A114     | 2000                   |      |
|                                           | Charged device model, JESD22-C101 | 1000                   |      |

**Notes**

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability
- <sup>(1)</sup> The specification values indicated “AC” is  $V_{SWH}$  to  $P_{GND}$  -7 V (< 20 ns, 10  $\mu$ J), min. and 35 V (< 50 ns), max.
- <sup>(2)</sup> The specification value indicates “AC voltage” is  $V_{BOOT}$  to  $P_{GND}$ , 40 V (< 50 ns) max.
- <sup>(3)</sup> The specification value indicates “AC voltage” is  $V_{BOOT}$  to  $V_{PHASE}$ , 8 V (< 50 ns) max.

**RECOMMENDED OPERATING RANGE**

| ELECTRICAL PARAMETER                           | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|------------------------------------------------|---------|---------|---------|------|
| Input voltage ( $V_{IN}$ )                     | 2.5     | -       | 16      | V    |
| Control logic supply voltage ( $V_{CC}$ )      | 4.5     | 5       | 5.5     |      |
| BOOT to PHASE ( $V_{BOOT-PHASE}$ , DC voltage) | 4       | 4.5     | 5.5     |      |
| Thermal resistance from junction to ambient    | -       | 10.6    | -       | °C/W |
| Thermal resistance from junction to case       | -       | 1.6     | -       |      |

**ELECTRICAL SPECIFICATIONS**(ZCD\_EN# = 5 V, V<sub>IN</sub> = 12 V, V<sub>CC</sub> = 5 V, DSBL# = 5 V, T<sub>A</sub> = 25 °C, unless otherwise stated)

| PARAMETER                              | SYMBOL                      | TEST CONDITION                                                                         | LIMITS |      |      | UNIT |
|----------------------------------------|-----------------------------|----------------------------------------------------------------------------------------|--------|------|------|------|
|                                        |                             |                                                                                        | MIN.   | TYP. | MAX. |      |
| POWER SUPPLY                           |                             |                                                                                        |        |      |      |      |
| Control logic supply current           | I <sub>VCC</sub>            | V <sub>PWM</sub> = FLOAT                                                               | -      | 120  | -    | μA   |
|                                        |                             | V <sub>PWM</sub> = FLOAT, V <sub>ZCD_EN#</sub> = 0 V                                   | -      | 170  | -    |      |
| Drive supply current                   |                             | f <sub>S</sub> = 300 kHz, D = 0.1                                                      | -      | 11   | 20   | mA   |
|                                        |                             | f <sub>S</sub> = 1 MHz, D = 0.1                                                        | -      | 36   | -    |      |
| PS4 mode supply current                | I <sub>VCC</sub>            | V <sub>PWM</sub> = V <sub>ZCD_EN#</sub> = FLOAT,<br>T <sub>A</sub> = -10 °C to +100 °C | -      | 4.5  | 9    | μA   |
|                                        |                             | DSBL# = 0 V                                                                            | -      | 8    | 17   |      |
| BOOTSTRAP SUPPLY                       |                             |                                                                                        |        |      |      |      |
| Bootstrap switch R <sub>DS(on)</sub>   | R <sub>BS</sub>             | V <sub>CC</sub> = 5 V                                                                  | -      | 3.3  | -    | Ω    |
| DSBL# CONTROL INPUT                    |                             |                                                                                        |        |      |      |      |
| DSBL# logic input voltage              | V <sub>IH_DSBL#</sub>       | Input logic high                                                                       | 2      | -    | -    | V    |
|                                        | V <sub>IL_DSBL#</sub>       | Input logic low                                                                        | -      | -    | 0.8  |      |
| DSBL# input current                    | I <sub>DSBL#</sub>          | V <sub>DSBL#</sub> = 5 V                                                               | -      | -    | 1    | μA   |
| PWM CONTROL INPUT (SiC679)             |                             |                                                                                        |        |      |      |      |
| Rising threshold                       | V <sub>TH_PWM_R</sub>       | V <sub>PWM</sub> = FLOAT                                                               | 4.2    | -    | -    | V    |
| Falling threshold                      | V <sub>TH_PWM_F</sub>       |                                                                                        | -      | -    | 0.72 |      |
| Tri-state voltage                      | V <sub>TRI</sub>            |                                                                                        | -      | 2.5  | -    |      |
| Tri-state rising threshold             | V <sub>TRI_TH_R</sub>       |                                                                                        | 1.6    | -    | -    |      |
| Tri-state falling threshold            | V <sub>TRI_TH_F</sub>       |                                                                                        | -      | -    | 3.4  |      |
| Tri-state rising threshold hysteresis  | V <sub>HYS_TRI_R</sub>      | -                                                                                      | 450    | -    | mV   |      |
| Tri-state falling threshold hysteresis | V <sub>HYS_TRI_F</sub>      | -                                                                                      | 225    | -    |      |      |
| PWM input current                      | I <sub>PWM</sub>            | V <sub>PWM</sub> = 5 V                                                                 | -      | -    | 350  | μA   |
|                                        |                             | V <sub>PWM</sub> = 0 V                                                                 | -      | -    | -350 |      |
| PWM CONTROL INPUT (SiC679A)            |                             |                                                                                        |        |      |      |      |
| Rising threshold                       | V <sub>TH_PWM_R</sub>       | V <sub>PWM</sub> = FLOAT                                                               | 2.7    | -    | -    | V    |
| Falling threshold                      | V <sub>TH_PWM_F</sub>       |                                                                                        | -      | -    | 0.69 |      |
| Tri-state voltage                      | V <sub>TRI</sub>            |                                                                                        | -      | 1.8  | -    |      |
| Tri-state rising threshold             | V <sub>TRI_TH_R</sub>       |                                                                                        | 1.38   | -    | -    |      |
| Tri-state falling threshold            | V <sub>TRI_TH_F</sub>       |                                                                                        | -      | -    | 1.95 |      |
| Tri-state rising threshold hysteresis  | V <sub>HYS_TRI_R</sub>      |                                                                                        | -      | 500  | -    | mV   |
| Tri-state falling threshold hysteresis | V <sub>HYS_TRI_F</sub>      |                                                                                        | -      | 225  | -    |      |
| PWM input current                      | I <sub>PWM</sub>            | V <sub>PWM</sub> = 3.3 V                                                               | -      | -    | 225  | μA   |
|                                        |                             | V <sub>PWM</sub> = 0 V                                                                 | -      | -    | -225 |      |
| ZCD_EN# CONTROL INPUT (SiC679)         |                             |                                                                                        |        |      |      |      |
| Rising threshold                       | V <sub>TH_ZCD_EN#_R</sub>   | V <sub>ZCD_EN#</sub> = FLOAT                                                           | 4.2    | -    | -    | V    |
| Falling threshold                      | V <sub>TH_ZCD_EN#_F</sub>   |                                                                                        | -      | -    | 1.1  |      |
| Tri-state voltage                      | V <sub>TRI_ZCD_EN#</sub>    |                                                                                        | -      | 2.5  | -    |      |
| Tri-state rising threshold             | V <sub>TRI_ZCD_EN#_R</sub>  |                                                                                        | 2.1    | -    | -    |      |
| Tri-state falling threshold            | V <sub>TRI_ZCD_EN#_F</sub>  |                                                                                        | -      | -    | 2.9  |      |
| Tri-state rising threshold hysteresis  | V <sub>HYS_TRI_ZCD#_R</sub> |                                                                                        | -      | 600  | -    | mV   |
| Tri-state falling threshold hysteresis | V <sub>HYS_TRI_ZCD#_F</sub> |                                                                                        | -      | 450  | -    |      |
| ZCD_EN# input current                  | I <sub>ZCD_EN#</sub>        | V <sub>ZCD_EN#</sub> = 5 V                                                             | -      | -    | 100  | μA   |
|                                        |                             | V <sub>ZCD_EN#</sub> = 0 V                                                             | -      | -    | -100 |      |

**ELECTRICAL SPECIFICATIONS**(ZCD\_EN# = 5 V, V<sub>IN</sub> = 12 V, V<sub>CC</sub> = 5 V, DSBL# = 5 V, T<sub>A</sub> = 25 °C, unless otherwise stated)

| PARAMETER                                          | SYMBOL                      | TEST CONDITION                         | LIMITS |      |      | UNIT  |
|----------------------------------------------------|-----------------------------|----------------------------------------|--------|------|------|-------|
|                                                    |                             |                                        | MIN.   | TYP. | MAX. |       |
| ZCD_EN# CONTROL INPUT (SiC679A)                    |                             |                                        |        |      |      |       |
| Rising threshold                                   | V <sub>TH_ZCD_EN#_R</sub>   |                                        | 2.8    | -    | -    | V     |
| Falling threshold                                  | V <sub>TH_ZCD_EN#_F</sub>   |                                        | -      | -    | 0.7  |       |
| Tri-state voltage                                  | V <sub>TRI_ZCD_EN#</sub>    | V <sub>ZCD_EN#</sub> = FLOAT           | -      | 1.6  | -    |       |
| Tri-state rising threshold                         | V <sub>TRI_ZCD_EN#_R</sub>  |                                        | 1.5    | -    | -    |       |
| Tri-state falling threshold                        | V <sub>TRI_ZCD_EN#_F</sub>  |                                        | -      | -    | 1.9  |       |
| Tri-state rising threshold hysteresis              | V <sub>HYS_TRI_ZCD#_R</sub> |                                        | -      | 325  | -    | mV    |
| Tri-state falling threshold hysteresis             | V <sub>HYS_TRI_ZCD#_F</sub> |                                        | -      | 250  | -    |       |
| ZCD_EN# input current                              | I <sub>ZCD_EN#</sub>        | V <sub>ZCD_EN#</sub> = 3.3 V           | -      | -    | 100  | μA    |
|                                                    |                             | V <sub>ZCD_EN#</sub> = 0 V             | -      | -    | -100 |       |
| TIMING SPECIFICATIONS                              |                             |                                        |        |      |      |       |
| Tri-state to GH/GL rising propagation delay        | t <sub>PD_TRI_R</sub>       | No load, see Fig. 4                    | -      | 50   | -    | ns    |
| Tri-state hold-off time                            | t <sub>TSHO</sub>           |                                        | -      | 47   | -    |       |
| GH - turn off propagation delay                    | t <sub>PD_OFF_GH</sub>      |                                        | -      | 25   | -    |       |
| GH - turn on propagation delay (dead time rising)  | t <sub>PD_ON_GH</sub>       |                                        | -      | 12   | -    |       |
| GL - turn off propagation delay                    | t <sub>PD_OFF_GL</sub>      |                                        | -      | 40   | -    |       |
| GL - turn on propagation delay (dead time falling) | t <sub>PD_ON_GL</sub>       |                                        | -      | 11   | -    |       |
| PWM minimum on-time                                | t <sub>PWM_ON_MIN.</sub>    |                                        | -      | 20   | -    | μs    |
| PS4 exit latency                                   | t <sub>PS4EXIT</sub>        |                                        | -      | -    | 5.5  |       |
| UNDER VOLTAGE LOCKOUT                              |                             |                                        |        |      |      |       |
| V <sub>CC</sub> under voltage lockout              | V <sub>UVLO</sub>           | V <sub>CC</sub> rising, on threshold   | 4      | -    | -    | V     |
|                                                    |                             | V <sub>CC</sub> falling, off threshold | -      | -    | 3.4  |       |
| V <sub>CC</sub> under voltage lockout hysteresis   | V <sub>UVLO_HYST</sub>      |                                        | -      | 250  | -    | mV    |
| THERMAL MONITOR AND FAULT FLAG <sup>(2)</sup>      |                             |                                        |        |      |      |       |
| Gain                                               | T <sub>OUT_GAIN</sub>       |                                        | -      | 8    | -    | mV/°C |
| Offset voltage at 0 °C                             | V <sub>OFF_0C</sub>         |                                        | 0.4    | 0.6  | 0.8  | V     |
| T <sub>OUT</sub> range 125 °C (temp. reporting)    | T <sub>OUT_125C</sub>       |                                        | -      | 1.6  | -    |       |
| FAULT mode                                         | FAULT <sub>HIGH</sub>       |                                        | 2.4    | -    | 3.6  |       |
| FAULT drive current                                | FAULT <sub>DRIVE</sub>      |                                        | -      | 97   | -    | mA    |
| Thermal flag                                       | T <sub>THDN</sub>           |                                        | -      | 140  | -    | °C    |
| Thermal flag hysteresis                            | T <sub>THDN_HYS</sub>       |                                        | -      | 25   | -    |       |
| PROTECTIONS <sup>(2)</sup>                         |                             |                                        |        |      |      |       |
| Over current protection                            | I <sub>OCP</sub>            |                                        | 90     | 110  | -    | A     |
| Over temperature protection                        | T <sub>SHDN</sub>           |                                        | -      | 165  | -    | °C    |

**Notes**

(1) Typical limits are established by characterization and are not production tested

(2) Guaranteed by design



## DETAILED OPERATIONAL DESCRIPTION

### DSBL# Input, Enable Function

The DSBL# pin shuts down the driver and disables both high side and low side MOSFETs. In this state, standby current is minimized. When DSBL# is low, both PWM and ZCD\_EN# internal dividers are disconnected to reduce current consumption. If DSBL# is left unconnected, an internal pull-up resistor will pull the pin to  $V_{CC}$  and enable the SiC679.

### PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above  $V_{PWM\_TH\_R}$  the low side is turned OFF and the high side is turned ON. When PWM input is driven below  $V_{PWM\_TH\_F}$  the high side is turned OFF and the low side is turned ON. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is a third state that is entered as the PWM output of a tri-state compatible controller enters its high impedance state. The high impedance state of the controller's PWM output allows the SiC679 to pull the PWM input into the tri-state region (see definition of PWM logic and tri-state, fig. 4). If the PWM input stays in this region for the tri-state hold-off period,  $t_{TSHO}$ , both high side and low side MOSFETs are turned OFF. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC679 incorporates PWM voltage thresholds that are compatible with 5 V logic.

### Diode Emulation Mode and PS4 Mode (ZCD\_EN#)

The ZCD\_EN# pin enables or disables diode emulation mode. When ZCD\_EN# is driven below  $V_{TH\_ZCD\_EN\#\_F}$ , diode emulation is allowed. When ZCD\_EN# is driven above  $V_{TH\_ZCD\_EN\#\_R}$ , continuous conduction mode is forced. Diode emulation mode allows for higher converter efficiency under light load situations. With diode emulation active, the SiC679 will detect the zero current crossing of the output inductor and turn off the low side MOSFET. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal, therefore, the SiC679 will respond to the ZCD\_EN# input immediately after it changes state.

The ZCD\_EN# pin can be floated resulting in a high impedance state. The SiC679 will pull a floated ZCD\_EN# to the internally set tri-state level. A tri-state ZCD\_EN# combined with a tri-stated PWM output will shut down the SiC679, reducing current consumption to typically 3  $\mu A$ . This is an important feature in achieving the low standby current required in the PS4 state in ultrabooks and notebooks.

### Voltage Input ( $V_{IN}$ )

This is the power input to the drain of the high side power MOSFET. This pin is connected to the high power intermediate BUS rail.

### Switch Node ( $V_{SWH}$ and PHASE)

The switch node,  $V_{SWH}$ , is the power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node  $V_{SWH}$ . This pin is to be used exclusively as the return pin for the BOOT capacitor.

### Ground Connections ( $C_{GND}$ and $P_{GND}$ )

$P_{GND}$  (power ground) should be externally connected to  $C_{GND}$  (control analog ground). The layout of the printed circuit board should be such that the inductance separating  $C_{GND}$  and  $P_{GND}$  is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

### Control and Drive Supply Voltage Input ( $V_{CC}$ )

$V_{CC}$  is the bias supply for the control IC and for the gate drivers.

### Bootstrap Circuit (BOOT)

A bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap switch is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a bootstrap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

### Shoot-Through Protection and Adaptive Dead Time

The SiC679 has an internal adaptive logic to avoid shoot-through and optimize dead time. The shoot-through protection ensures that both high side and low side MOSFETs are not turned on at the same time. The adaptive dead time control operates as follows. The high side and low side gate voltages are monitored to prevent one from turning on until the other gate voltage is sufficiently low ( $< 1$  V). Built-in delays also ensure that one power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

### Under Voltage Lockout (UVLO)

During the start up cycle the UVLO disables the gate drive, holding high side and low side MOSFET gates low until the supply voltage has reached a point at which the logic circuitry can be safely activated. The SiC679 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device.

### T<sub>MON</sub>/FAULT Temperature Monitor and Fault Flag Functions

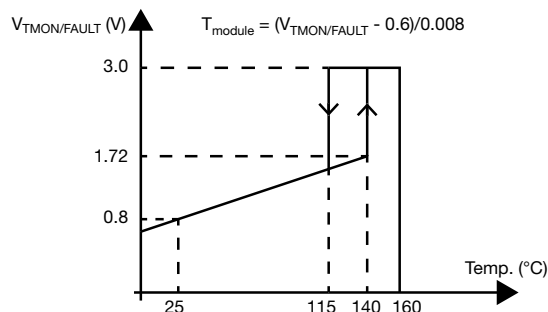
The T<sub>MON</sub>/FAULT output is used to report operating conditions detected by the logic of the driver that require attention.

A fault is reported by the T<sub>MON</sub>/FAULT output going high to 3.3 V.

The reported conditions are high temperature, insufficient bootstrap voltage, persistent over-current, high side MOSFET short.

The T<sub>MON</sub>/FAULT output also reports the operating temperature of the SiC679.

The temperature is converted to a voltage with a conversion gain of 8 mV/°C and a target value of 600 mV at 0 °C.



In a multi-phase topology, all T<sub>MON</sub>/FAULT signals are connected to the PWM controller and will indicate the temp. of the warmest device.

If the operating temperature exceeds 140 °C the T<sub>MON</sub>/FAULT output will signal a fault condition. The fault is reset when the temperature is below the temperature hysteresis threshold.

For proper operation, the T<sub>MON</sub> output must be biased with a resistor to ground. A 1 kΩ resistor is recommended. The SiC679 also has an over temperature shutdown feature that stops operation when the temperature is above 160 °C. The over temperature shutdown fault is reset by DISBL# cycling or power cycling.

### Over Current Protection Function

The SiC679 is equipped with over-current protection. An over-current condition will also be reported through the T<sub>MON</sub>/FAULT flag. The flag is automatically reset after 128 switching cycles that do not trigger the protection. When the output current exceeds safe operating levels the SiC679 will protect the power devices by forcing an early termination of the high side conduction time and eventually folding the operating frequency (skipping PWM cycles) as needed.

### High Side MOSFET Short Detection

A failure of the high side MOSFET may cause significant system damage. For this reason the SiC679 monitors the switching node (PHASE) cycle by cycle in order to promptly detect a short of the high side power device. After four consecutive HS short condition cycles are detected, the SiC679 will report the fault with the T<sub>MON</sub>/FAULT flag, and will ignore the incoming PWM signal. The low side MOSFET is activated to protect the load from high voltage.

The fault flag can only be reset by cycling power to the driver's logic.

### FUNCTIONAL BLOCK DIAGRAM

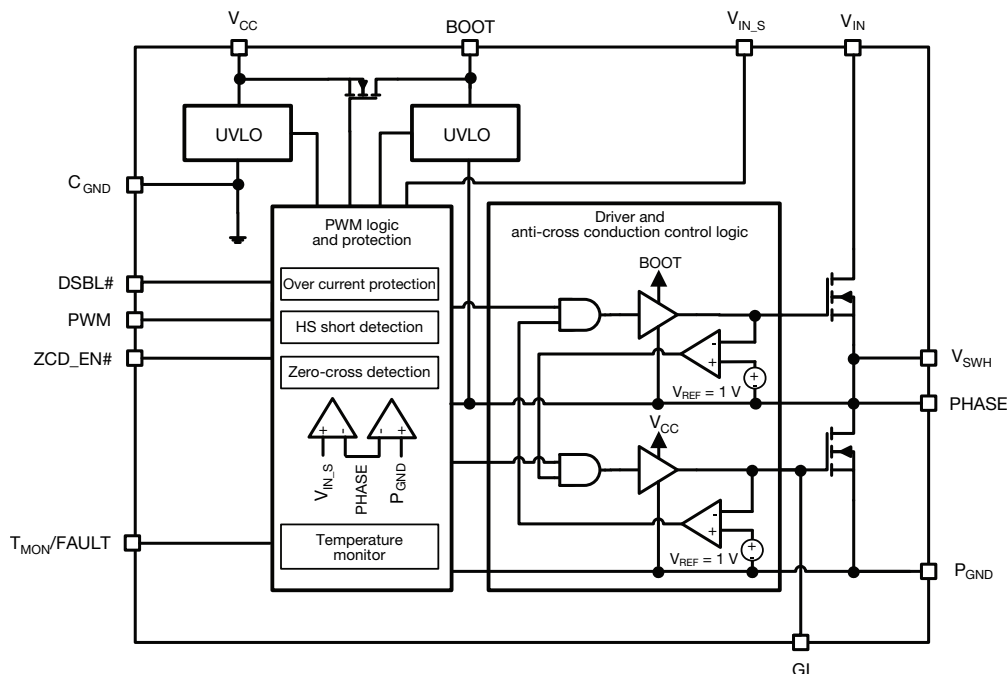


Fig. 3 - Functional Block Diagram



| DEVICE TRUTH TABLE |           |           |    |                                  |
|--------------------|-----------|-----------|----|----------------------------------|
| DSBL#              | ZCD_EN#   | PWM       | GH | GL                               |
| L                  | X         | X         | L  | L                                |
| H                  | Tri-state | X         | L  | L                                |
| H                  | L         | L         | L  | H, $I_L > 0$ A<br>L, $I_L < 0$ A |
| H                  | L         | H         | H  | L                                |
| H                  | L         | Tri-state | L  | L                                |
| H                  | H         | L         | L  | H                                |
| H                  | H         | H         | H  | L                                |
| H                  | H         | Tri-state | L  | L                                |

## PWM TIMING DIAGRAM

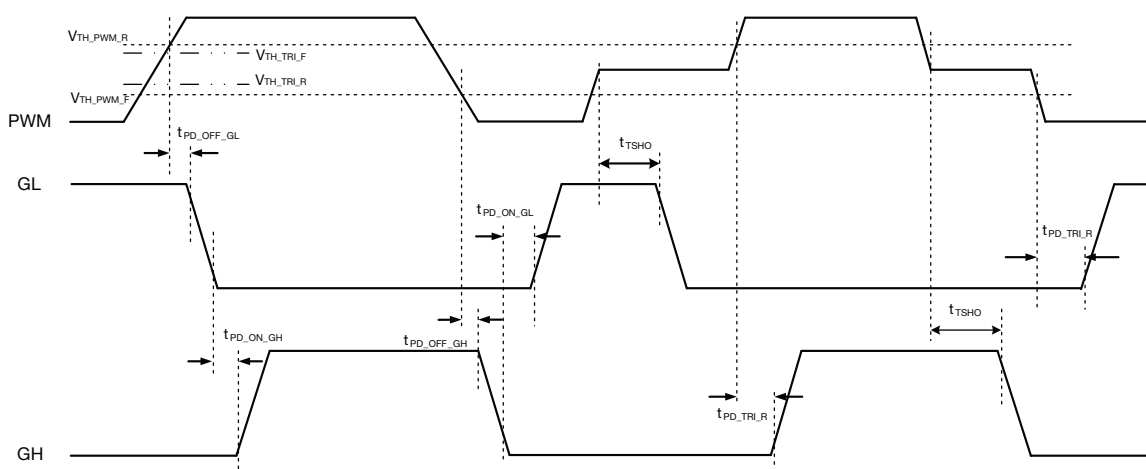


Fig. 4 - Definition of PWM Logic and Tri-state

## ZCD\_EN# - PS4 Exit Timing

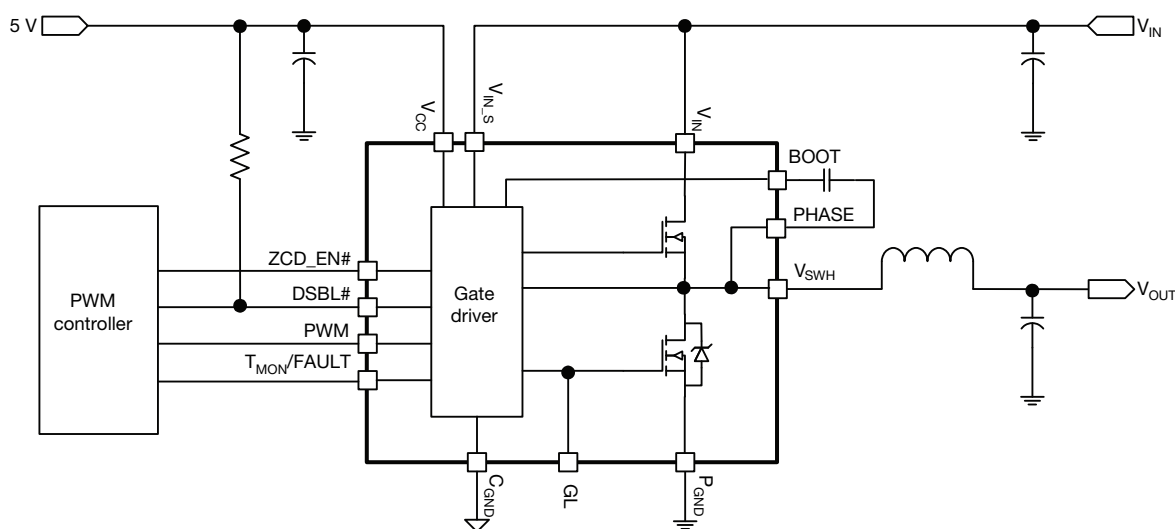


Fig. 5 - ZCD\_EN# - PS4 Exit Timing





## ELECTRICAL CHARACTERISTICS

Test condition:  $V_{IN} = 12\text{ V}$  (unless otherwise stated),  $V_{CC} = 5\text{ V}$ ,  $ZCD\_EN\# = 5\text{ V}$ ,  $DSBL\# = 5\text{ V}$ ,  $V_{OUT} = 1.05\text{ V}$ ,  $L_{OUT} = 220\text{ nH}$  ( $DCR = 0.29\text{ m}\Omega$ ),  $T_A = 25\text{ }^\circ\text{C}$ , natural convection cooling (all power loss and normalized power loss curves show SiC679 losses only unless otherwise stated)

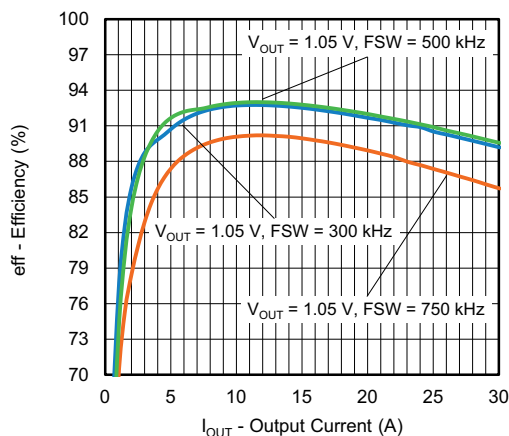


Fig. 6 - Efficiency vs. Output Current ( $V_{IN} = 12\text{ V}$ )

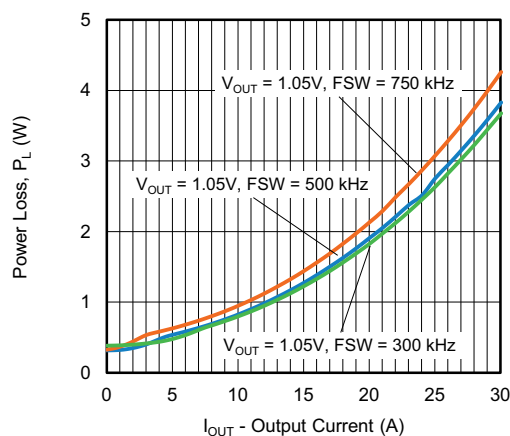


Fig. 8 - Power Loss vs. Output Current ( $V_{IN} = 12\text{ V}$ )

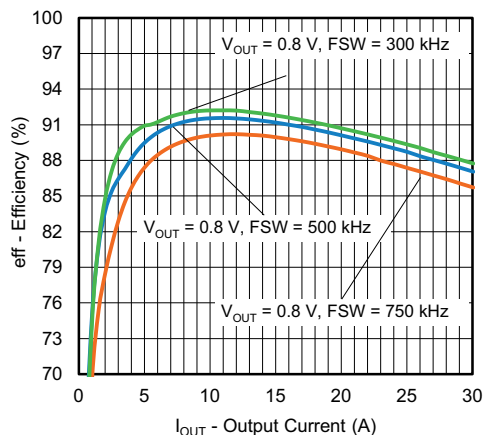


Fig. 7 - Efficiency vs. Output Current ( $V_{IN} = 12\text{ V}$ )

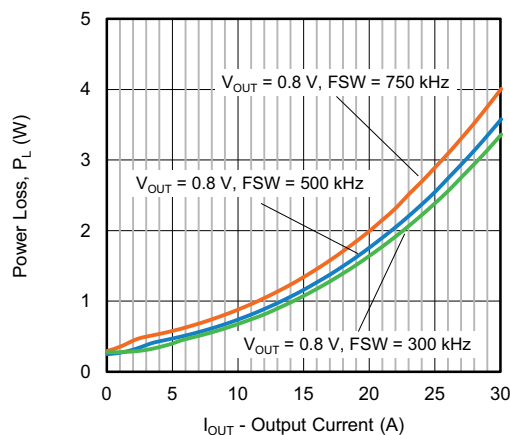


Fig. 9 - Power Loss vs. Output Current ( $V_{IN} = 12\text{ V}$ )



## ELECTRICAL CHARACTERISTICS

Test condition:  $V_{IN} = 13\text{ V}$  (unless otherwise stated),  $V_{CC} = 5\text{ V}$ ,  $ZCD\_EN\# = 5\text{ V}$ ,  $DSBL\# = 5\text{ V}$ ,  $V_{OUT} = 1.05\text{ V}$ ,  $L_{OUT} = 220\text{ nH}$  ( $DCR = 0.29\text{ m}\Omega$ ),  $T_A = 25\text{ }^\circ\text{C}$ , natural convection cooling (all power loss and normalized power loss curves show SiC679 losses only unless otherwise stated)

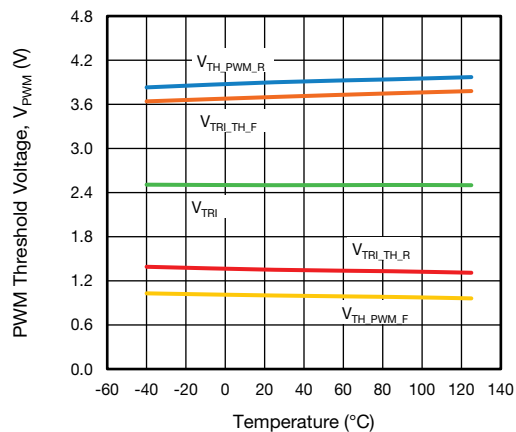


Fig. 10 - PWM Threshold vs. Temperature

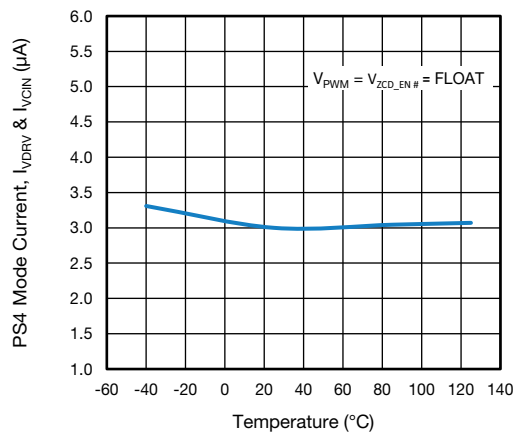


Fig. 12 - PS4 Mode Current vs. Temperature

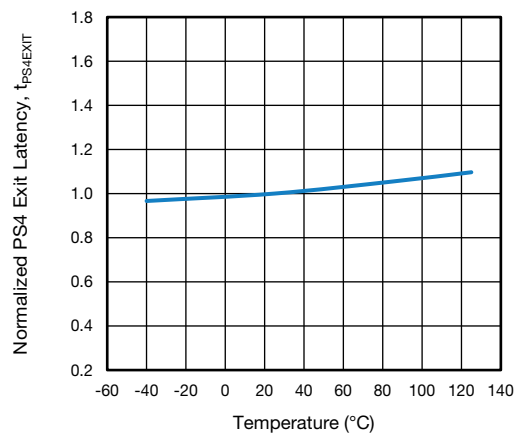
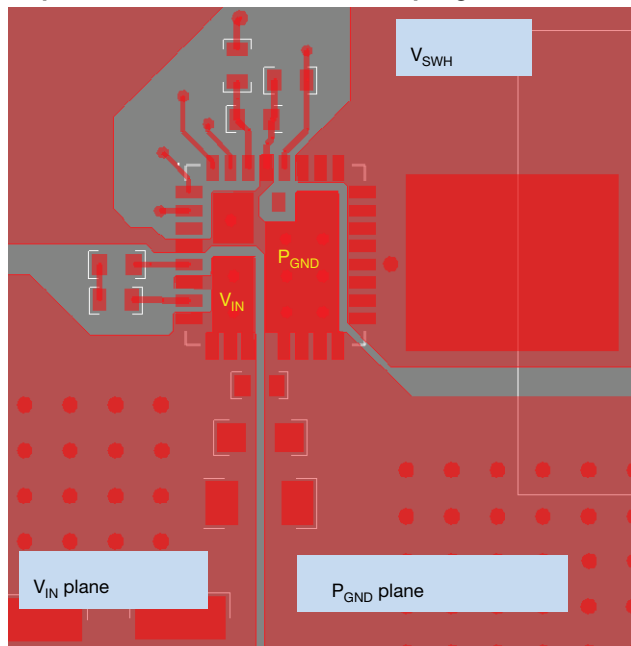


Fig. 11 - PS4 Exit Latency vs. Temperature

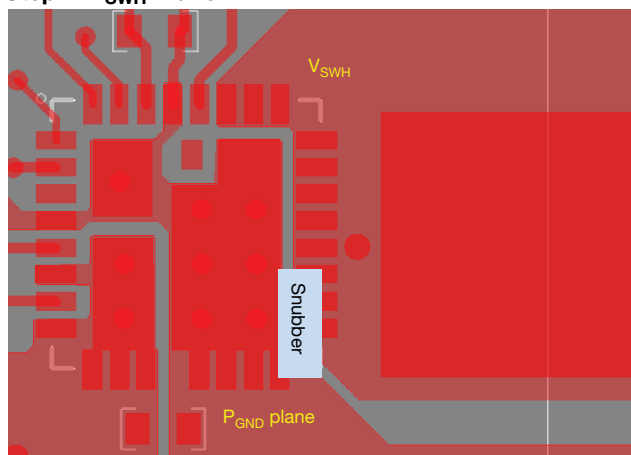
## PCB LAYOUT RECOMMENDATIONS

### Step 1: $V_{IN}$ / GND Planes and Decoupling



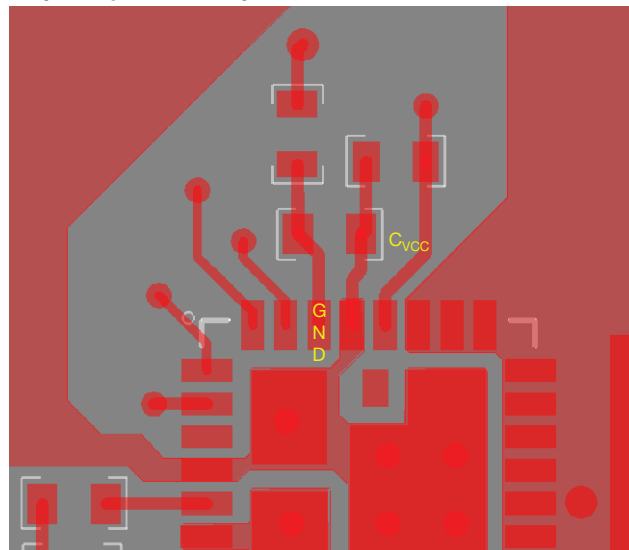
1. Layout  $V_{IN}$  and  $P_{GND}$  planes as shown above
2. Ceramic capacitors should be placed right between  $V_{IN}$  and  $P_{GND}$ , and very close to the device for best decoupling effect
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603, and 0402
4. Smaller capacitance value, closer to device  $V_{IN}$  pin(s) - better high frequency noise absorbing

### Step 2: $V_{SWH}$ Plane



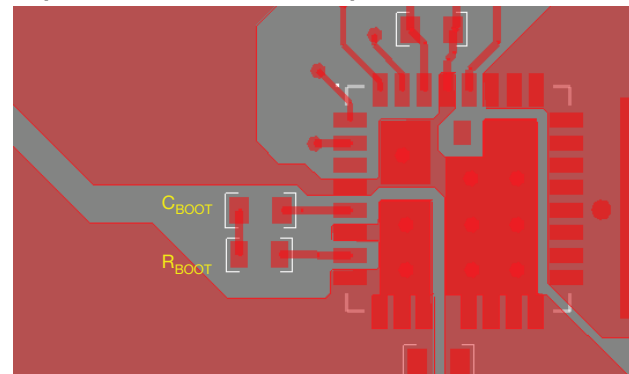
1. Connect output inductor to DrMOS with large plane to lower the resistance
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom

### Step 3: $V_{CIN}$ / $V_{DRV}$ Input Filter

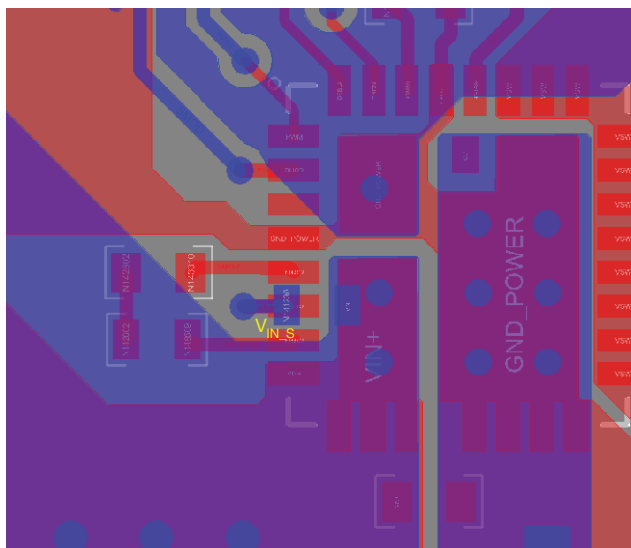
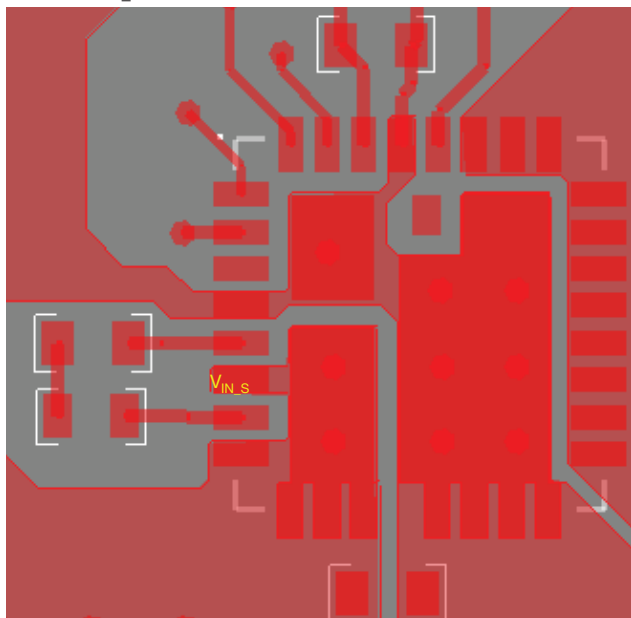


3. The  $V_{CC}$  input filter ceramic cap should be placed very close to DrMOS
4.  $C_{VCC}$  cap should be placed between pin 28 ( $P_{GND}$  of driver IC) and pin 29 to provide maximum instantaneous driver current for low side MOSFET during switching cycle

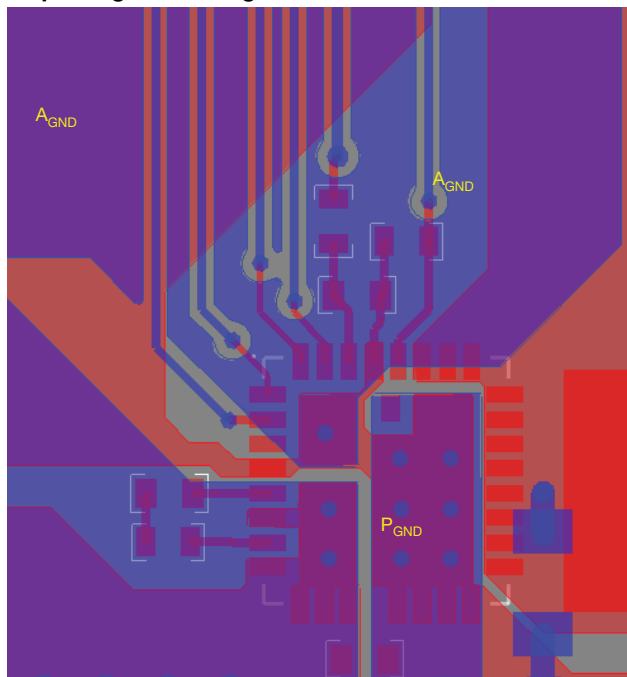
### Step 4: BOOT Resistor and Capacitor Placement



1. These components need to be placed very close to DrMOS, right between PHASE (pin 7) and BOOT (pin 5)
2. To reduce parasitic inductance, chip size 0402 can be used

**Step 5:  $V_{IN\_S}$  Connection**


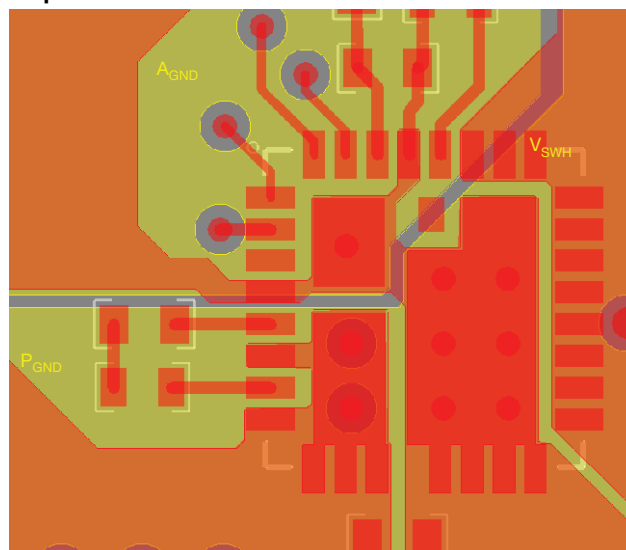
1.  $V_{IN\_S}$  (pin 6) is used to detect HS MOSFET over current. Connect this pin to the  $V_{IN}$  pad
2. To keep the connection flexibility,  $V_{IN\_S}$  (pin 6) can be connected with  $V_{IN}$  through a Via and resistor like the right side. Floating the  $V_{IN\_S}$  pin by unpopulating the resistor will NOT affect normal operation, but this will make the device lose HS OCP function

**Step 6: Signal Routing**


1. Route the PWM / SMOD / DSBL / THDN signal traces out of the top left corner next DrMOS pin1
2. PWM signal is very important signal, both signal and return traces need to pay special attention of not letting this trace cross any power nodes on any layer
3. It is best to “shield” them with GND island form power switching nodes, e.g.  $V_{SWH}$ , to improve signal integrity
4. GL (pin27) has been connected with GL pad internally and does not to connect externally

**Step 7: Adding Thermal Relief Vias**

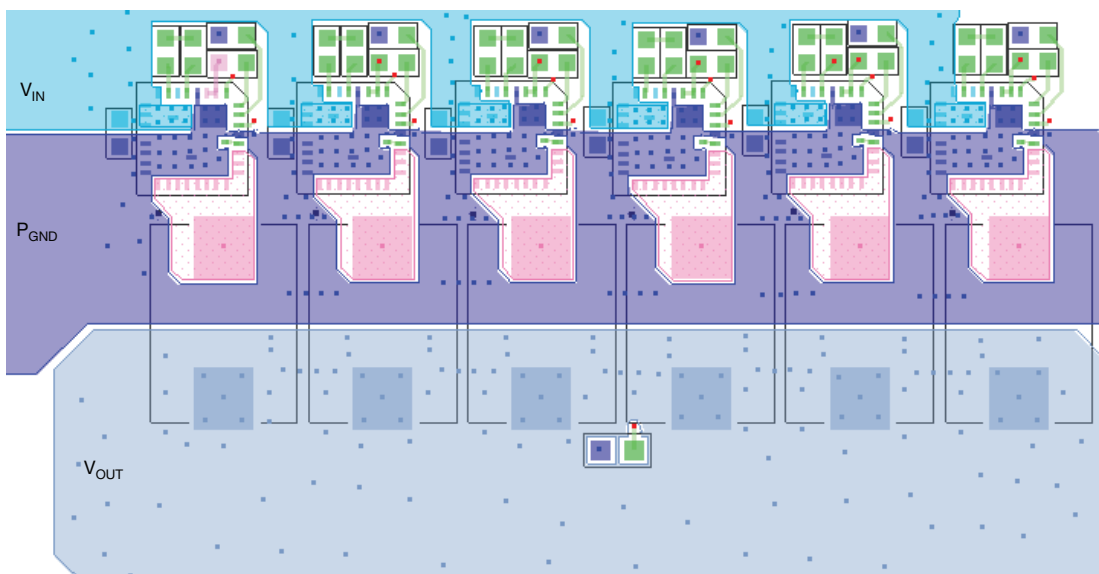

1. Thermal relief Vias can be added on the  $V_{IN}$  and GND pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional Vias can be put on  $V_{IN}$  plane and  $P_{GND}$  plane
3.  $V_{SWH}$  pad is a noise source and not recommended to put Vias on this plane
4. 8 mil drill for pads and 10 mils drill for plane can be the optional Via size with 40 mils pitch. The Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

**Step 8: Ground Connection**


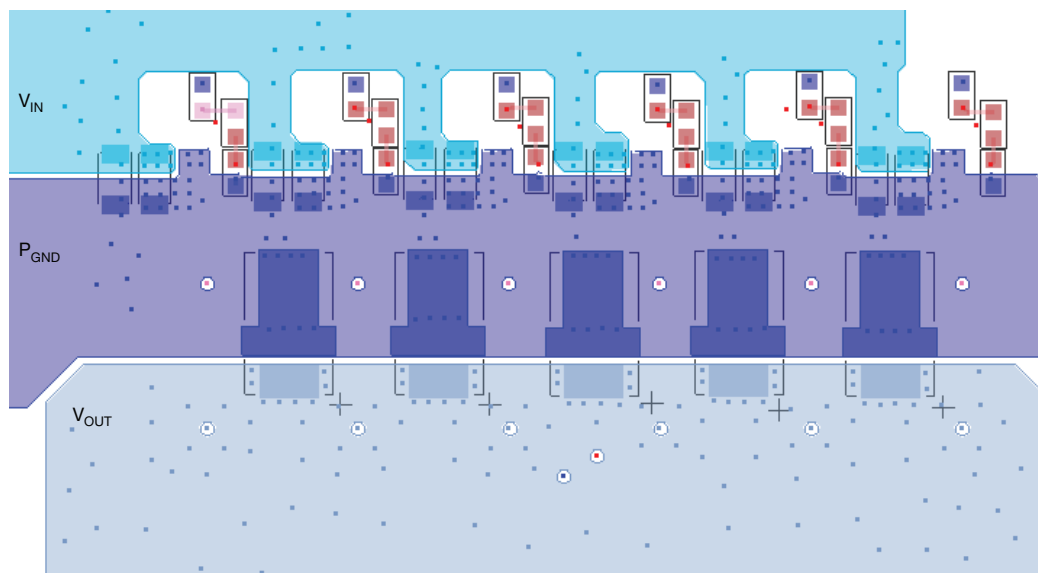
1. It is recommended to make single connection between  $A_{GND}$  and  $P_{GND}$  and this connection can be done on top layer
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into  $A_{GND}$  and  $P_{GND}$  plane
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer

### Multi-Phases VRPower PCB Layout

The following is an example of 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling capacitors next to them. The inductors are placed as close as possible to the SiC679 to minimize the PCB copper loss. Vias are applied on all PADs ( $V_{IN}$ ,  $P_{GND}$ ,  $C_{GND}$ ) of the SiC679 to ensure that both electrical and thermal performance are optimized. Large copper planes are used for all high current loops, such as  $V_{IN}$ ,  $V_{SWH}$ ,  $V_{OUT}$  and  $P_{GND}$ . These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC679 to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.



**Fig. 13 - Multi-Phase VRPower Layout Top View**



**Fig. 14 - Multi-Phase VRPower Layout Bottom View**

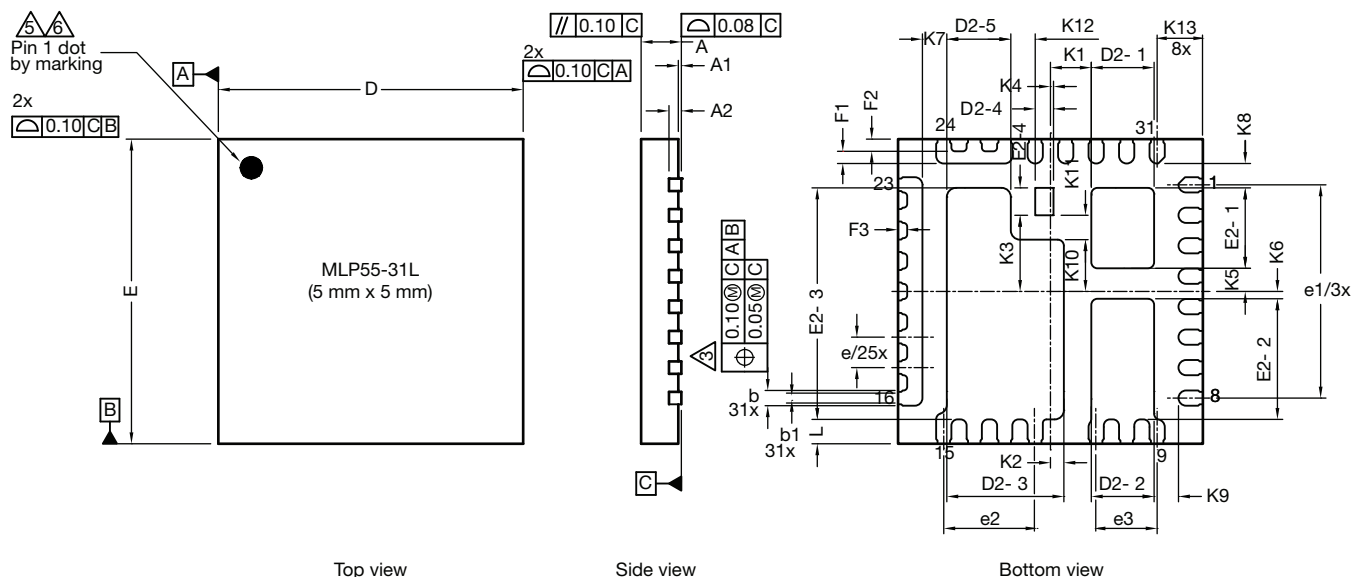


| PRODUCT SUMMARY             |                                                                             |                                                                               |
|-----------------------------|-----------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| Part number                 | SiC679                                                                      | SiC679A                                                                       |
| Description                 | 60 A Power stage plus, 2.5 V to 16 V, 5 V <sub>PWM</sub> with ZCD, PS4 mode | 60 A Power stage plus, 2.5 V to 16 V, 3.3 V <sub>PWM</sub> with ZCD, PS4 mode |
| Input voltage min. (V)      | 2.5                                                                         | 2.5                                                                           |
| Input voltage max. (V)      | 16                                                                          | 16                                                                            |
| Current rating (A)          | 60                                                                          | 60                                                                            |
| Switch frequency max. (kHz) | 2000                                                                        | 2000                                                                          |
| Enable (yes / no)           | Yes                                                                         | Yes                                                                           |
| Monitoring features         | T <sub>MON</sub> /FAULT Monitor                                             | T <sub>MON</sub> /FAULT Monitor                                               |
| Protection                  | OCP, OTP, UVLO                                                              | OCP, OTP, UVLO                                                                |
| Light load mode             | ZCD                                                                         | ZCD                                                                           |
| Pulse-width modulation (V)  | 5                                                                           | 3.3                                                                           |
| Package type                | PowerPAK® MLP55-31L                                                         | PowerPAK® MLP55-31L                                                           |
| Package size (W, L, H) (mm) | 5 x 5 x 0.75                                                                | 5 x 5 x 0.75                                                                  |
| Status code                 | 1                                                                           | 1                                                                             |
| Product type                | VRPower (DrMOS)                                                             | VRPower (DrMOS)                                                               |
| Applications                | Computers, networking                                                       | Computers, networking                                                         |

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## PowerPAK<sup>®</sup> MLP55-31L Case Outline



| DIM. | MILLIMETERS |      |      | INCHES     |       |       |
|------|-------------|------|------|------------|-------|-------|
|      | MIN.        | NOM. | MAX. | MIN.       | NOM.  | MAX.  |
| A    | 0.70        | 0.75 | 0.80 | 0.027      | 0.029 | 0.031 |
| A1   | 0.00        | -    | 0.05 | 0.000      | -     | 0.002 |
| A2   | 0.20 ref.   |      |      | 0.008 ref. |       |       |
| b    | 0.20        | 0.25 | 0.30 | 0.078      | 0.098 | 0.011 |
| b1   | 0.15        | 0.20 | 0.25 | 0.006      | 0.008 | 0.010 |
| D    | 4.90        | 5.00 | 5.10 | 0.193      | 0.196 | 0.200 |
| e    | 0.50 BSC    |      |      | 0.019 BSC  |       |       |
| e1   | 3.50 BSC    |      |      | 0.138 BSC  |       |       |
| e2   | 1.50 BSC    |      |      | 0.060 BSC  |       |       |
| e3   | 1.00 BSC    |      |      | 0.040 BSC  |       |       |
| E    | 4.90        | 5.00 | 5.10 | 0.193      | 0.196 | 0.200 |
| L    | 0.35        | 0.40 | 0.45 | 0.013      | 0.015 | 0.017 |
| D2-1 | 0.98        | 1.03 | 1.08 | 0.039      | 0.041 | 0.043 |
| D2-2 | 0.98        | 1.03 | 1.08 | 0.039      | 0.041 | 0.043 |
| D2-3 | 1.87        | 1.92 | 1.97 | 0.074      | 0.076 | 0.078 |
| D2-4 | 0.30 BSC    |      |      | 0.012 BSC  |       |       |
| D2-5 | 1.05        | 1.10 | 1.15 | 0.041      | 0.043 | 0.045 |
| E2-1 | 1.27        | 1.32 | 1.37 | 0.050      | 0.052 | 0.054 |
| E2-2 | 1.93        | 1.98 | 2.03 | 0.076      | 0.078 | 0.080 |
| E2-3 | 3.75        | 3.80 | 3.85 | 0.148      | 0.150 | 0.152 |
| E2-4 | 0.45 BSC    |      |      | 0.018 BSC  |       |       |
| F1   | 0.15        | 0.20 | 0.25 | 0.006      | 0.008 | 0.010 |
| F2   | 0.20 ref.   |      |      | 0.008 ref. |       |       |
| F3   | 0.15 ref.   |      |      | 0.006 ref. |       |       |

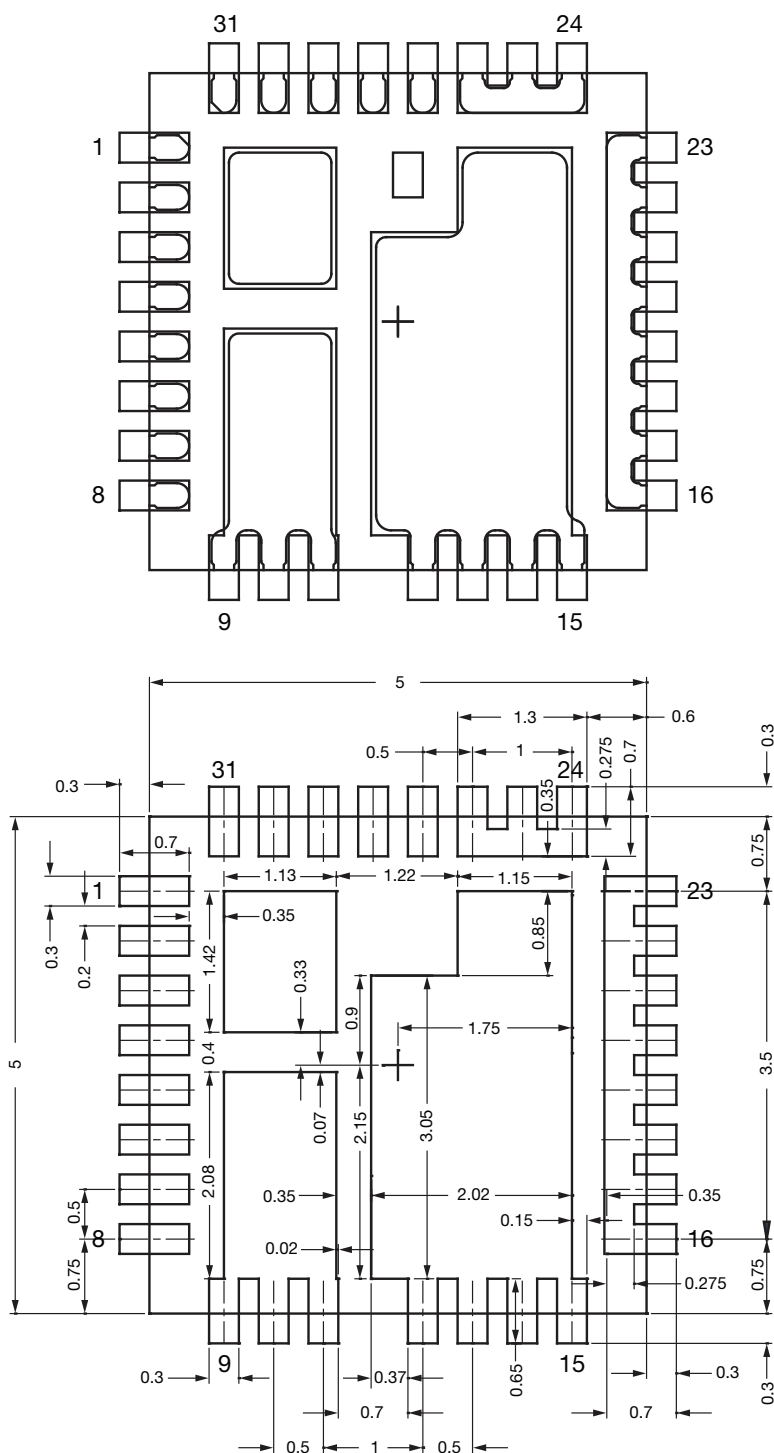


| DIM.                                         | MILLIMETERS |          |      | INCHES |           |      |
|----------------------------------------------|-------------|----------|------|--------|-----------|------|
|                                              | MIN.        | NOM.     | MAX. | MIN.   | NOM.      | MAX. |
| K1                                           |             | 0.67 BSC |      |        | 0.026 BSC |      |
| K2                                           |             | 0.22 BSC |      |        | 0.008 BSC |      |
| K3                                           |             | 1.25 BSC |      |        | 0.049 BSC |      |
| K4                                           |             | 0.10 BSC |      |        | 0.004 BSC |      |
| K5                                           |             | 0.38 BSC |      |        | 0.015 BSC |      |
| K6                                           |             | 0.12 BSC |      |        | 0.005 BSC |      |
| K7                                           |             | 0.40 BSC |      |        | 0.016 BSC |      |
| K8                                           |             | 0.40 BSC |      |        | 0.016 BSC |      |
| K9                                           |             | 0.40 BSC |      |        | 0.016 BSC |      |
| K10                                          |             | 0.85 BSC |      |        | 0.033 BSC |      |
| K11                                          |             | 0.40 BSC |      |        | 0.016 BSC |      |
| K12                                          |             | 0.40 BSC |      |        | 0.016 BSC |      |
| K13                                          |             | 0.75 BSC |      |        | 0.030 BSC |      |
| ECN: T17-0423-Rev. F, 21-Aug-17<br>DWG: 6025 |             |          |      |        |           |      |

**Notes**

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
4. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
5. Exact shape and size of this feature is optional
6. Package warpage max. 0.08 mm
7. Applied only for terminals

# Recommended Land Pattern PowerPAK® MLP31-55



E25-0221-Rev. A, 21-Apr-2025  
DWG: 3034



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