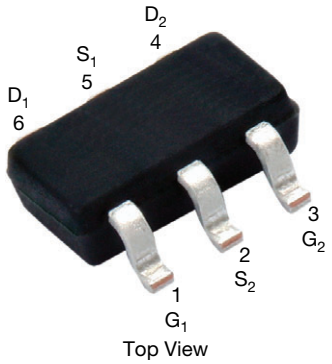
Automotive N- and P-Channel 20 V (D-S) MOSFET

TSOP-6 Dual



Top View

Marking Code: 9U

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

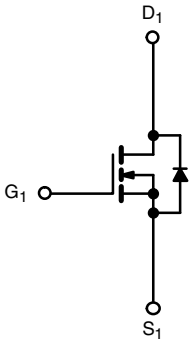
AUTOMOTIVE GRADE

Pb-free

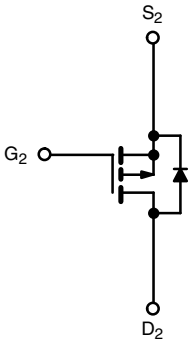
RoHS COMPLIANT

HALOGEN FREE

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	20	-20
$R_{DS(on)}$ (Ω) at V_{GS} = ± 4.5 V	0.077	0.166
$R_{DS(on)}$ (Ω) at V_{GS} = ± 2.5 V	0.120	0.318
I_D (A)	3.57	-2.5
Configuration	N- and p-pair	



N-Channel MOSFET



P-Channel MOSFET

ORDERING INFORMATION	
Package	TSOP-6 Dual
Lead (Pb)-free and halogen-free	SQ3585CEV (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V_{DS}	20	-20	V
Gate-source voltage		V_{GS}	± 12	± 12	
Continuous drain current	T_C = 25 °C	I_D	3.57	-2.5	A
	T_C = 125 °C		2	-1.45	
Pulsed drain current		I_{DM}	12	-10	
Continuous source current (diode conduction)		I_S	2.1	-2.1	
Maximum power dissipation	T_C = 25 °C	P_D	1.67	1.67	W
	T_C = 125 °C		0.56	0.56	
Unclamped inductive surge UIS		I_{AV}	3.3	3	A
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175		°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	N-CHANNEL MAX.	P-CHANNEL MAX.	UNIT
Maximum junction-to-ambient [a]	Steady state	R_{thJA}	150	150	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	90	90	

Note

a. Surface mounted on 1" x 1" FR4 board

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SPECIFICATIONS (T_J = 25°C, unless otherwise noted)								
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static								
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		N-Ch	0.6	-	1.5	V
		V_{DS} = V_{GS}, I_D = -250 µA		P-Ch	-0.6	-	-1.5	
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 20 V	N-Ch	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = -20 V	P-Ch	-	-	-1	
		V_{GS} = 0 V	V_{DS} = 20 V, T_J = 55 °C	N-Ch	-	-	5	
		V_{GS} = 0 V	V_{DS} = -20 V, T_J = 55 °C	P-Ch	-	-	-5	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 4.5 V	V_{DS} ≥ 5 V	N-Ch	5	-	-	A
		V_{GS} = -4.5 V	V_{DS} ≤ -5 V	P-Ch	-5	-	-	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V	I_D = 1 A	N-Ch	-	0.049	0.077	Ω
		V_{GS} = -4.5 V	I_D = -1 A	P-Ch	-	0.140	0.166	
		V_{GS} = 2.5 V	I_D = 1 A	N-Ch	-	0.066	0.120	
		V_{GS} = -2.5 V	I_D = -1 A	P-Ch	-	0.265	0.318	
Forward transconductance [a]	g_{fs}	V_{DS} = 5 V, I_D = 1 A		N-Ch	-	7	-	S
		V_{DS} = -5 V, I_D = -1 A		P-Ch	-	3	-	
Diode forward voltage [a]	V_{SD}	I_S = 1.05 A, V_{GS} = 0 V		N-Ch	-	0.80	1.10	V
		I_S = -1.05 A, V_{GS} = 0 V		P-Ch	-	-0.83	-1.10	
Dynamic [b]								
Total gate charge	Q_g	V_{GS} = 4.5 V	V_{DS} = 10 V, I_D = 1 A	N-Ch	-	2.0	3.0	nC
		V_{GS} = -4.5 V	V_{DS} = -10 V, I_D = -1 A	P-Ch	-	3.0	5.0	
Gate-source charge	Q_{gs}	V_{GS} = 4.5 V	V_{DS} = 10 V, I_D = 1 A	N-Ch	-	1.0	-	
		V_{GS} = -4.5 V	V_{DS} = -10 V, I_D = -1 A	P-Ch	-	1.0	-	
Gate-drain charge	Q_{gd}	V_{GS} = 4.5 V	V_{DS} = 10 V, I_D = 1 A	N-Ch	-	1.0	-	
		V_{GS} = -4.5 V	V_{DS} = -10 V, I_D = -1 A	P-Ch	-	1.0	-	
Gate resistance	R_g	f = 1 MHz		N-Ch	3.4	-	9.1	Ω
				P-Ch	3.4	-	9.1	
Turn-on delay time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 1 Ω P-Channel V_{DD} = -10 V, R_L = 10 Ω I_D ≅ -1 A, V_{GEN} = -10 V, R_g = 1 Ω		N-Ch	-	11	17	ns
				P-Ch	-	9	14	
Rise time	t_r			N-Ch	-	15	23	
				P-Ch	-	18	27	
Turn-off delay time	$t_{d(off)}$			N-Ch	-	19	29	
				P-Ch	-	14	21	
Fall time	t_f			N-Ch	-	8	12	
				P-Ch	-	5	9	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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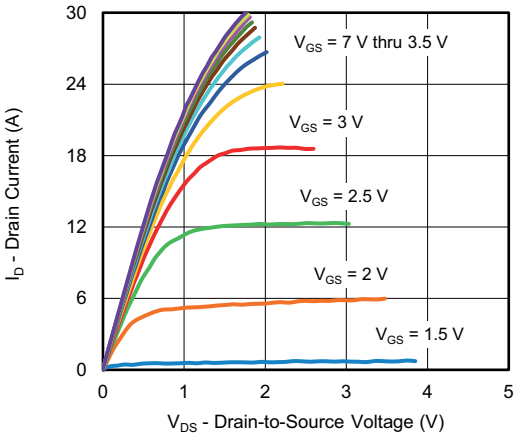
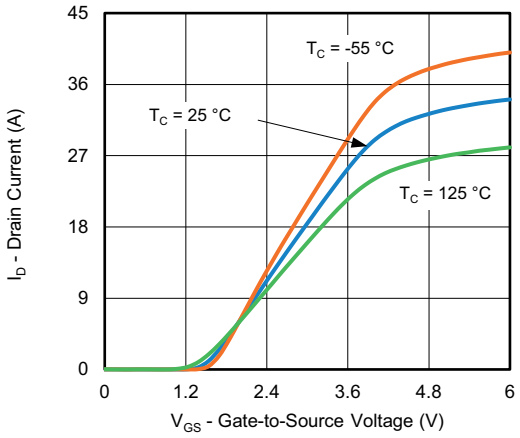
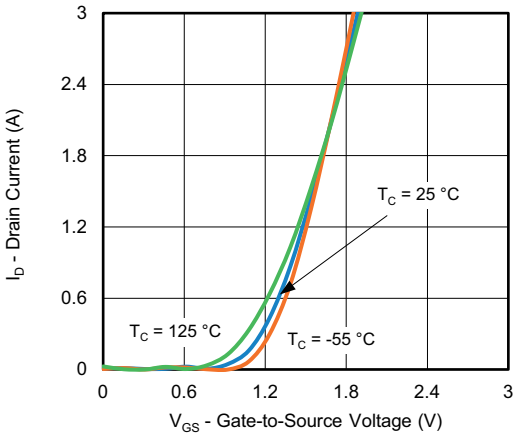
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



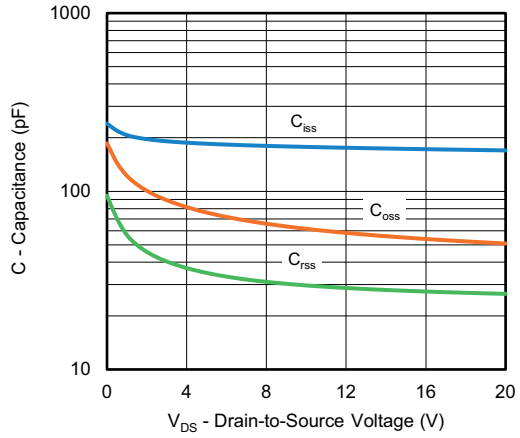
Output Characteristics



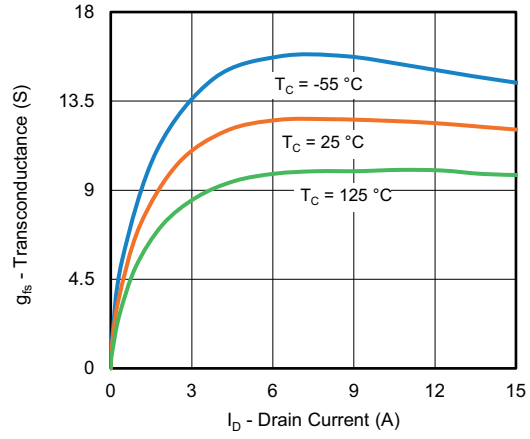
Transfer Characteristics



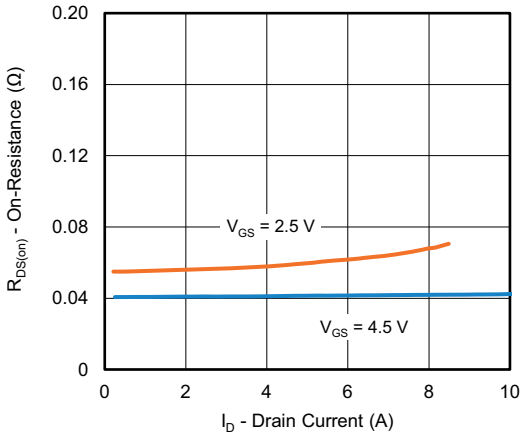
Transfer Characteristics



Capacitance



Transconductance



On-Resistance vs. Drain Current

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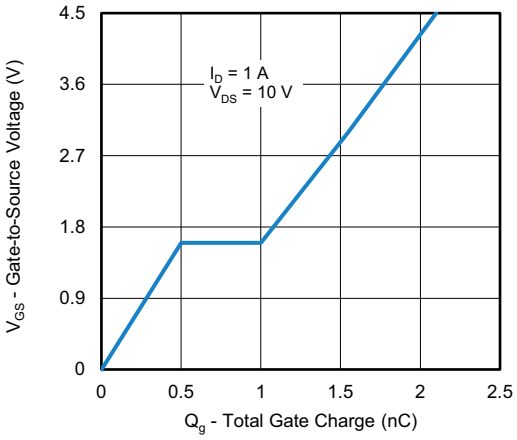
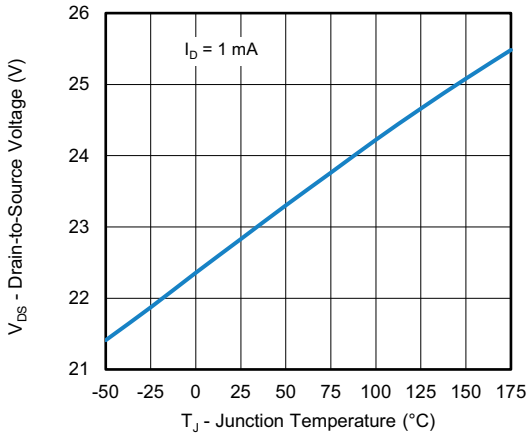
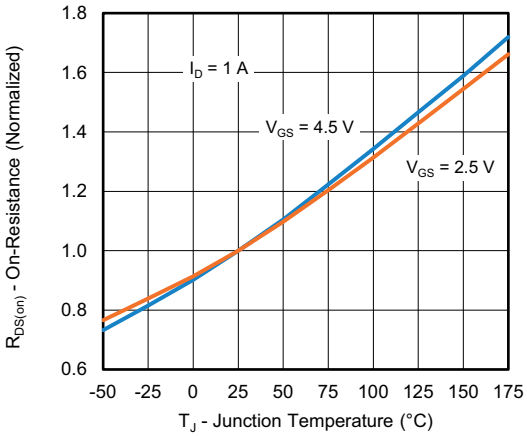


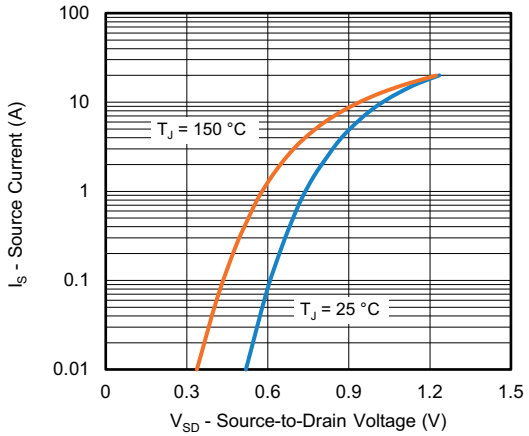
Gate Charge



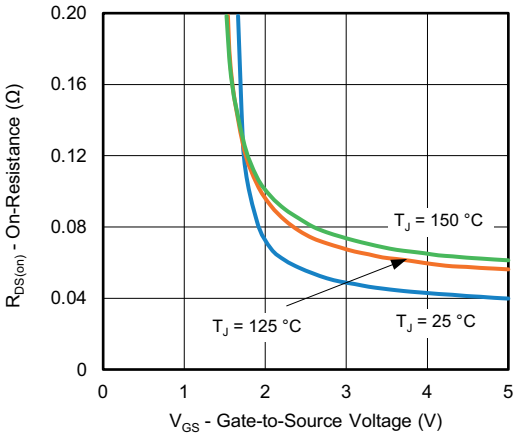
Drain Source Breakdown vs. Junction Temperature



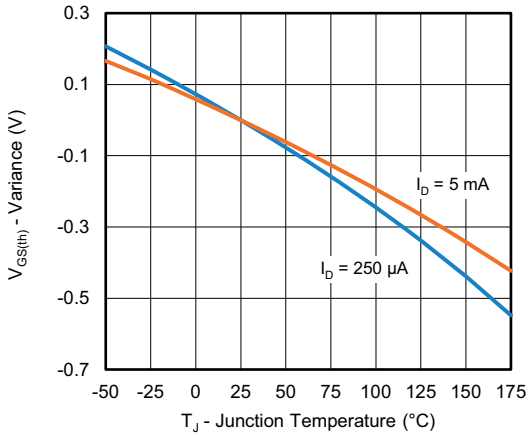
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

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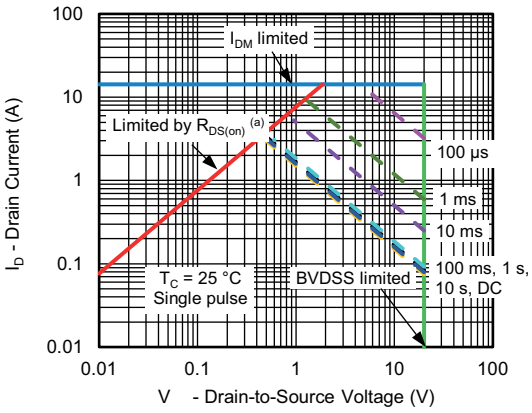

Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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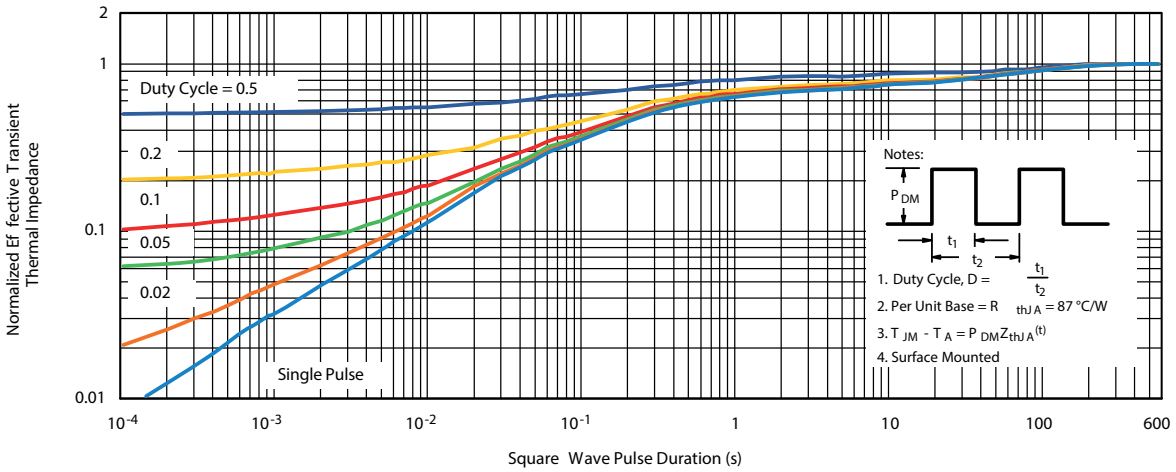
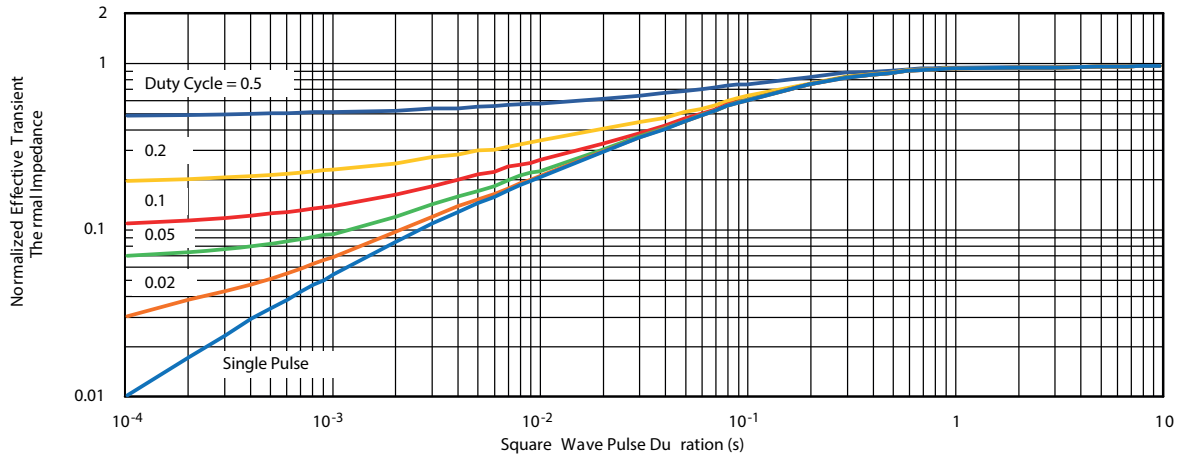


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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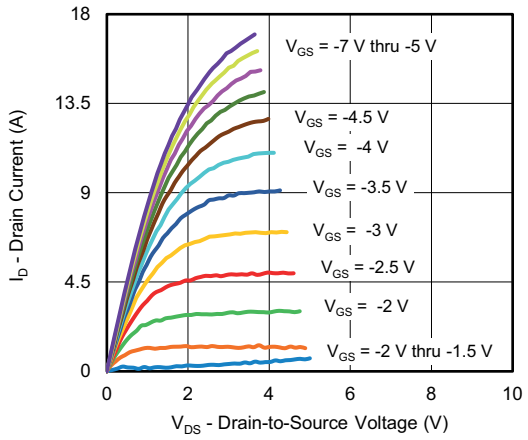
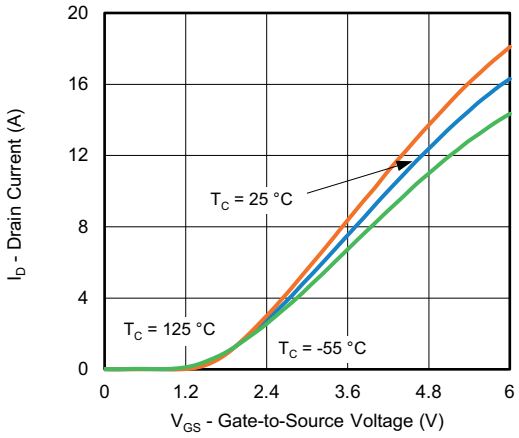
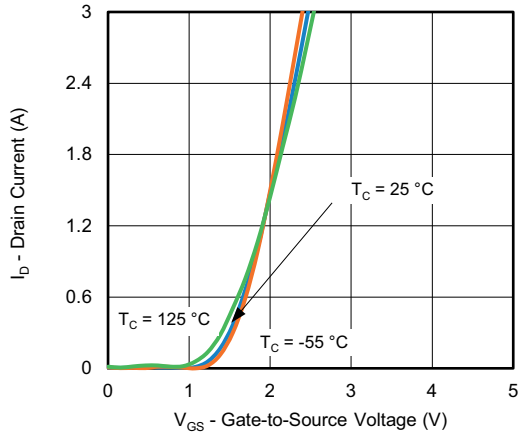
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



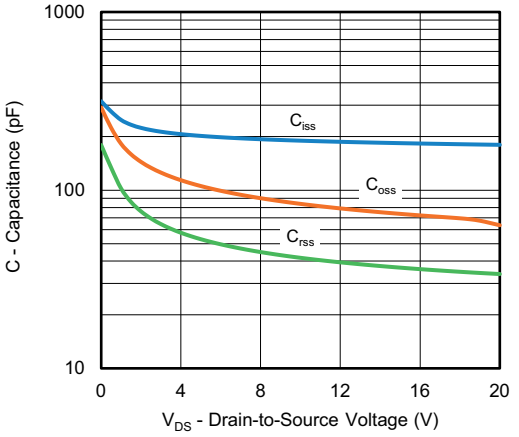
Output Characteristics



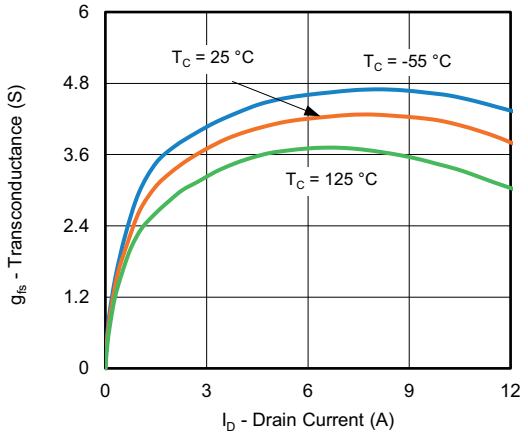
Transfer Characteristics



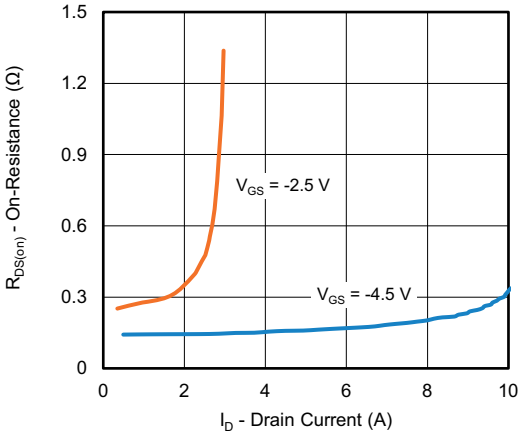
Transfer Characteristics



Capacitance



Transconductance



On-Resistance vs. Drain Current

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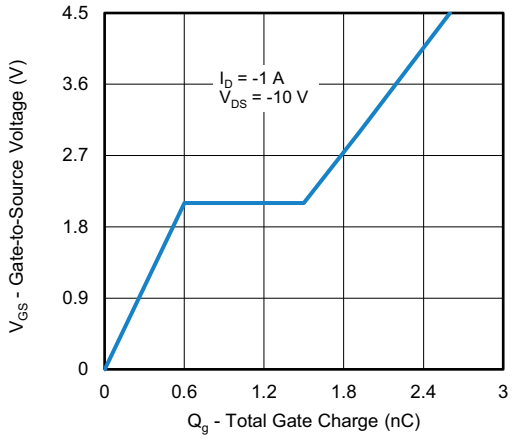
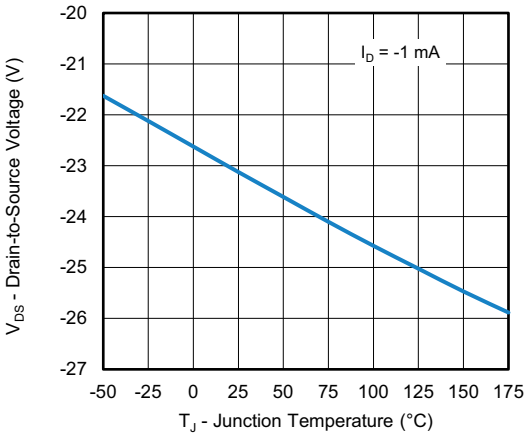
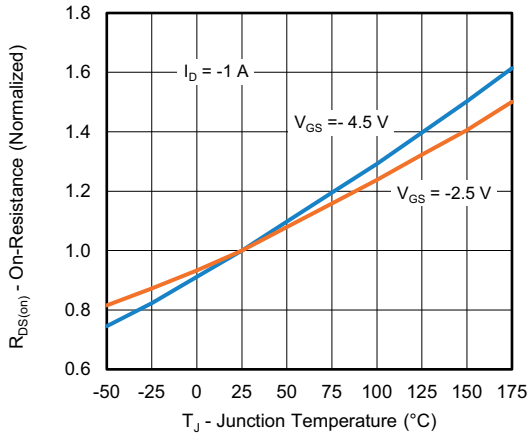


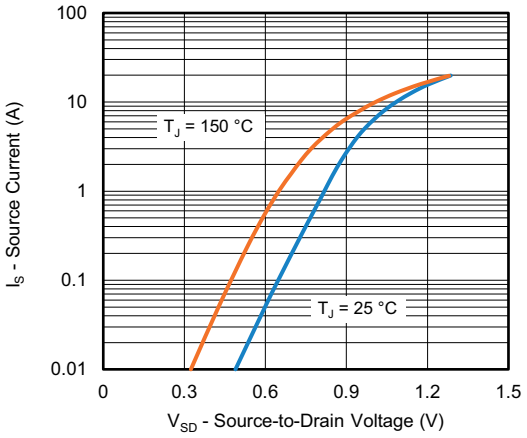
Gate Charge



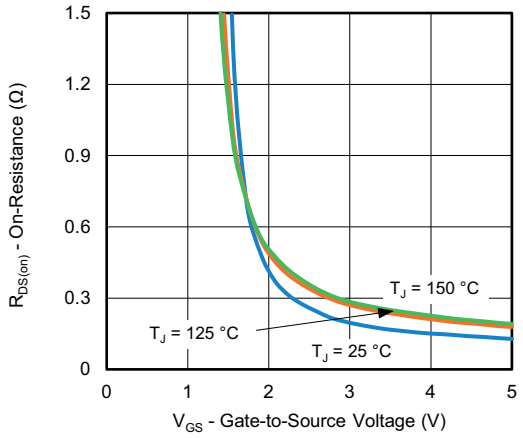
Drain Source Breakdown vs. Junction Temperature



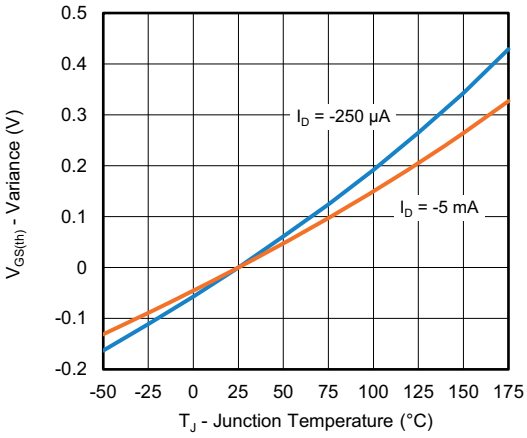
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

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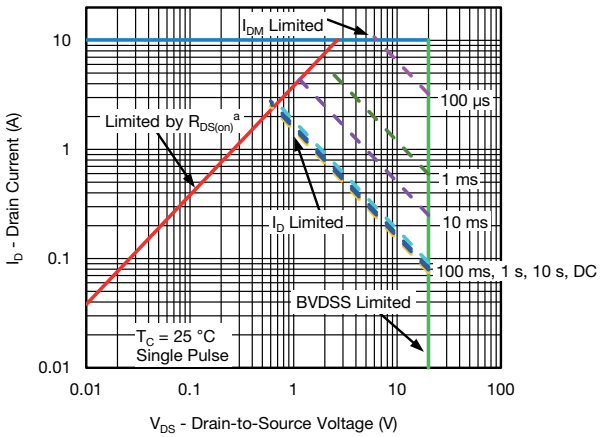

Safe Operating Area

Note

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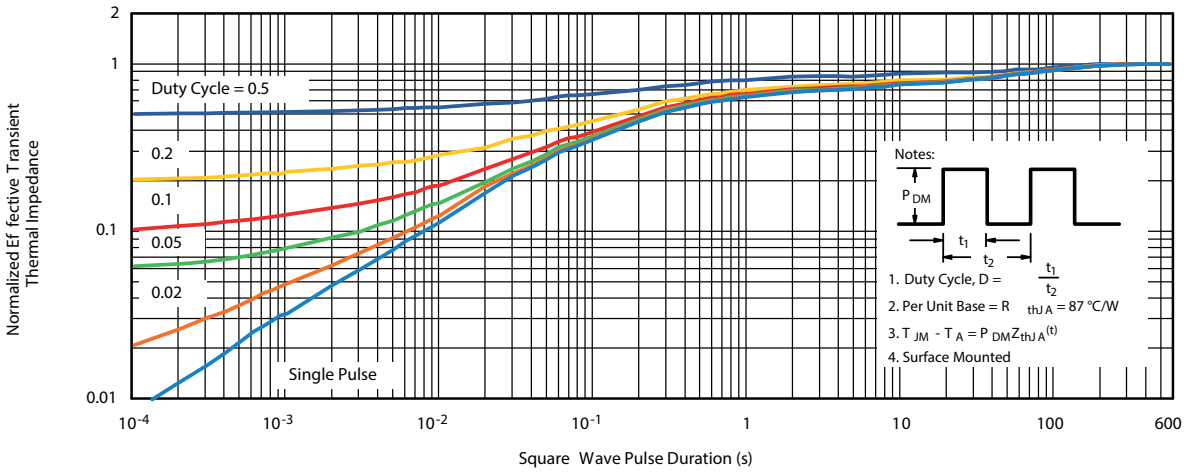
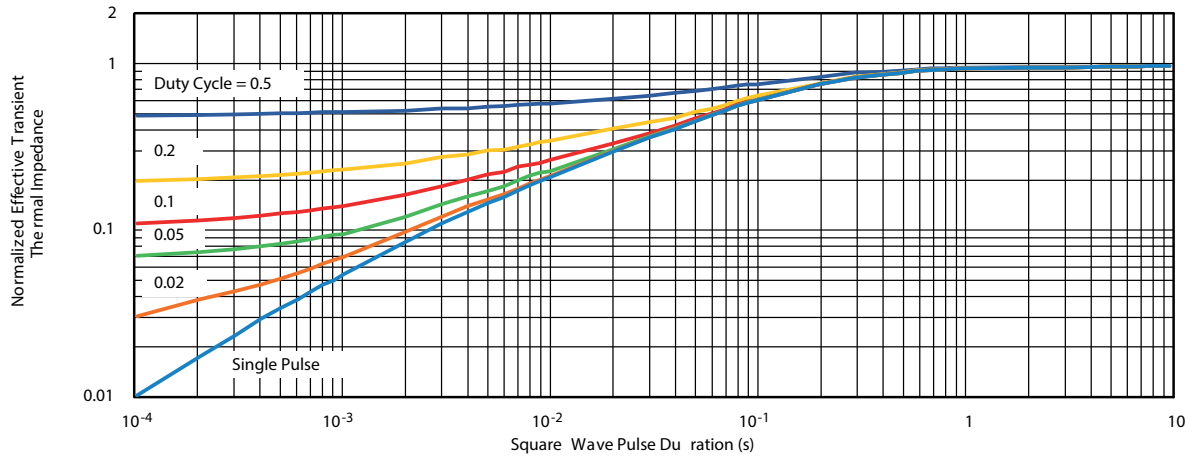
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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