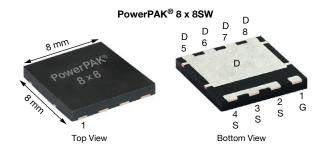
Vishay Siliconix

RoHS

COMPLIANT

HALOGEN FREE

# N-Channel 80 V (D-S) 175 °C MOSFET



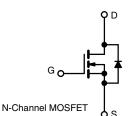
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	80				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.00175				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.00250				
Q <sub>g</sub> typ. (nC)	154				
I <sub>D</sub> (A) <sup>a</sup>	322				
Configuration	Single				

#### **FEATURES**

- TrenchFET® Gen III power MOSFET
- · Wettable flanks enhances solderability
- Fully lead (Pb)-free device
- Very low R<sub>DS(on)</sub>
- Very low R<sub>thJC</sub>
- PowerPAK® 8 x 8 with fuse lead to increase current density
- 100 % R<sub>q</sub> and UIS tested
- Up to 322 A maximum continuous drain current
- Optimized safe operating area / SOA
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

#### **APPLICATIONS**

- Hot swap
- · Load switch
- Oring
- Motor drive
- · Battery management



ORDERING INFORMATION	
Package	PowerPAK® 8 x 8SW
Lead (Pb)-free and halogen-free	SiEH3812EW-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage Gate-source voltage		$V_{DS}$	80	V	
		$V_{GS}$	± 20	v	
Continuous drain current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 25 °C		322		
	T <sub>C</sub> = 70 °C	1 .	269		
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	29 b		
	T <sub>A</sub> = 70 °C	†	24 <sup>b</sup>	^	
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	800	Α Α	
Continuous source-drain diode current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	379		
	T <sub>A</sub> = 25 °C		3.1 b		
Single pulse avalanche current	l 0.1 mall	I <sub>AS</sub>	92		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	430	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		417		
	T <sub>C</sub> = 70 °C	P <sub>D</sub>	292	- w	
	T <sub>A</sub> = 25 °C		3.4 b	VV	
	T <sub>A</sub> =70 °C		2.4 <sup>b</sup>		
Operating junction and storage temperature range Soldering recommendations (peak temperature) °		T <sub>J</sub> , T <sub>stq</sub>	-55 to +175	°C	
			260		

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient <sup>b</sup>	Steady state	$R_{thJA}$	33	44	°C/W	
Maximum junction-to-case (drain)	Steady state	Rthuc	0.27	0.36		

#### **Notes**

a.  $T_C = 25 \,^{\circ}C$ 

Surface mounted on 1" x 1" FR4 board

b. Surface mounted on 1 x 1 FR4 board
 c. See solder profile (<a href="https://www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
 d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



# Vishay Siliconix

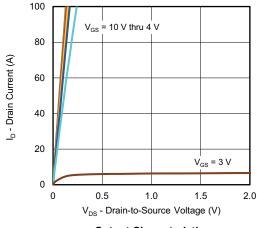
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					•		
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 10 mA	-	50	-		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-7	-	mV/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	-	3	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20$	-	-	± 100	nA	
Zana mata walka sa alusin awana t	,	V <sub>DS</sub> = 80 V, V <sub>GS</sub> =0 V	-	-	1	μA	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15		
Darie de la contra del contra de la contra del la contra de la contra de la contra del la contra del la contra de la contra de la contra del la contra del la contra de la contra de la contra del	5	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	0.00140	0.00175		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	0.00195	0.00250	Ω	
Forward transconductance a	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_D = 40 \text{ A}$	-	130	-	S	
Dynamic <sup>b</sup>					•		
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	7780	-	pF	
Output capacitance	C <sub>oss</sub>		-	3145	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	150	-		
Total colorado o co	0	$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	154	231		
Total gate charge	$Q_g$	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> =20 A	-	74	111	nC	
Gate-source charge	Q <sub>gs</sub>		-	30	-		
Gate-drain charge	Q <sub>gd</sub>		-	31	-		
Gate resistance	$R_{g}$	f = 1 MHz	0.8	4	8	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	16	32		
Rise time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_L = 4 \Omega, I_D \cong 10 \text{ A},$	-	22	45		
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	137	275		
Fall time	t <sub>f</sub>		-	49	100		
Turn-on delay time	t <sub>d(on)</sub>		-	96	195	- ns -	
Rise time	t <sub>r</sub>	$\begin{split} V_{DD} = 40 \text{ V}, \text{ R}_L = 4  \Omega, \text{ I}_D &\cong 10 \text{ A}, \\ V_{GEN} = 4.5 \text{ V}, \text{ R}_g = 1  \Omega \end{split}$	-	166	330		
Turn-off delay time	t <sub>d(off)</sub>		-	96	195		
Fall time	t <sub>f</sub>		- 52		105	1	
<b>Drain-Source Body Diode Characteristi</b>	cs						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	379		
Pulse diode forward current	I <sub>SM</sub>		-	-	800	Α	
Body diode voltage	$V_{SD}$	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.72	1.1	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	98	200	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	1 10 A 11/14 100 A/ - T 05 00	-	285	570	nC	
Reverse recovery fall time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	60	-		
Reverse recovery rise time	t <sub>b</sub>		-	38	-	ns	

#### Notes

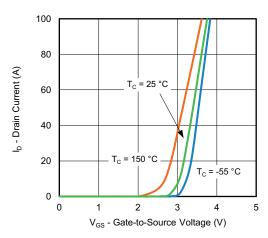
- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

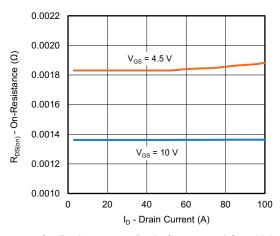




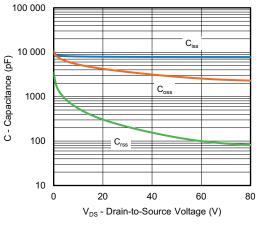
#### **Output Characteristics**



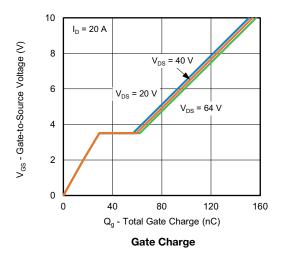
**Transfer Characteristics** 

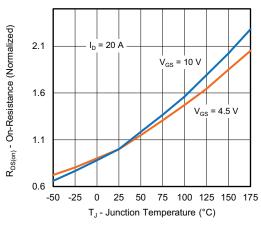


On-Resistance vs. Drain Current and Gate Voltage



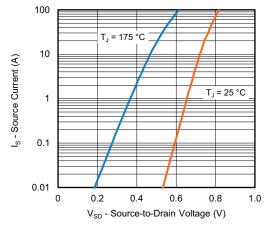
Capacitance



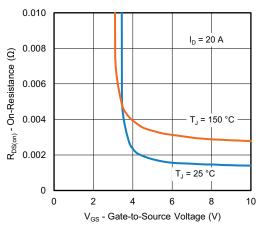


On-Resistance vs. Junction Temperature

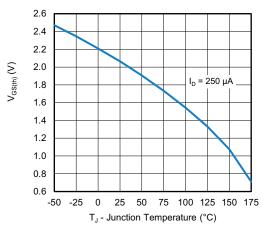




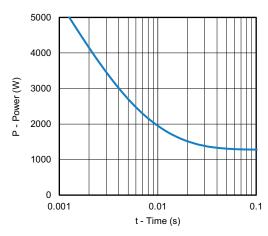
Source-Drain Diode Forward Voltage



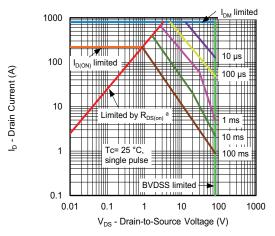
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



Single Pulse Power, Junction-to-Case

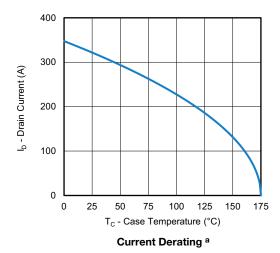


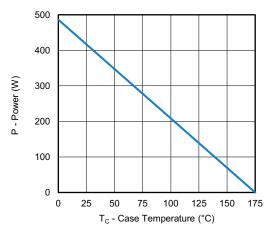
Safe Operating Area, Junction-to-Case

# Note

a.  $V_{GS} > minimum V_{GS}$  at which  $R_{DS(on)}$  is specified





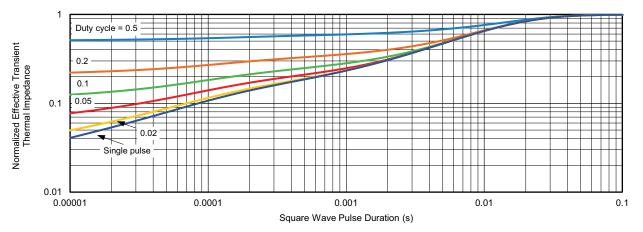


#### Power, Junction-to-Case

#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Case

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