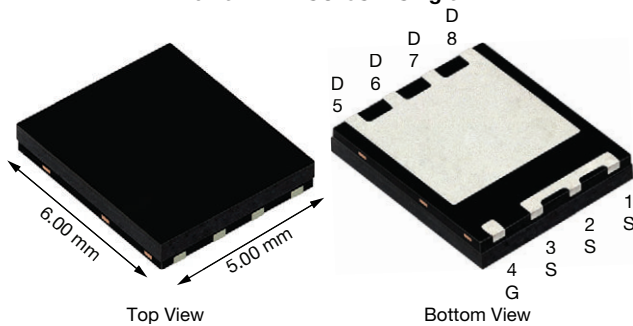


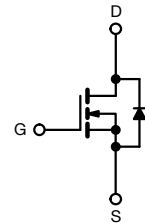
## N-Channel 100 V (D-S) MOSFET

**PowerPAK® SO-8SW Single**

**FEATURES**

- TrenchFET® Gen V power MOSFET
- Very low  $R_{DS(on)}$   $\times$   $Q_g$  figure-of-merit (FOM)
- Leadership  $R_{DS(on)}$  minimizes power loss from conduction
- 100 %  $R_g$  and UIS tested
- Enhance power dissipation and lower  $R_{thJC}$
- Wettable flank to improved solderability
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**
**APPLICATIONS**

- Synchronous rectification
- DC/DC converters
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0039
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0047
$Q_g$ typ. (nC)	34
$I_D$ (A) <sup>a</sup>	155
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8SW
Lead (Pb)-free and halogen-free	SiRS510EPW-T1-RE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	100	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	155	A
		$T_C = 70$ °C	130	
		$T_A = 25$ °C	31 <sup>b, c</sup>	
		$T_A = 70$ °C	26 <sup>b, c</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	200	A	
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C		
		$T_A = 25$ °C	7.6 <sup>b, c</sup>	
Single pulse avalanche current	$I_{AS}$	47	mJ	
Single pulse avalanche energy	$E_{AS}$	109		
Maximum power dissipation	$P_D$	$T_C = 25$ °C	205	W
		$T_C = 70$ °C	144	
		$T_A = 25$ °C	8.3 <sup>b, c</sup>	
		$T_A = 70$ °C	5.8 <sup>b, c</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	14	18	°C/W	
Maximum junction-to-case (drain)	$R_{thJC}$	0.53	0.73		

**Notes**

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 50 °C/W



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	66	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-7.6	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	10	
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	-	0.0032	0.0039	$\Omega$
		$V_{GS} = 7.5\text{ V}, I_D = 15\text{ A}$	-	0.0037	0.0047	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}$	-	72	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	3745	-	pF
Output capacitance	$C_{oss}$		-	900	-	
Reverse transfer capacitance	$C_{rss}$		-	8.5	-	
Total gate charge	$Q_g$	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	-	45.3	68	nC
		$V_{DS} = 50\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 15\text{ A}$	-	34	51	
Gate-source charge	$Q_{gs}$	$V_{DS} = 50\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 15\text{ A}$	-	18.1	-	
Gate-drain charge	$Q_{gd}$		-	2.8	-	
Output charge	$Q_{oss}$		$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	-	100	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.46	2.3	4.6	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	16	30	ns
Rise time	$t_r$		-	7	15	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	$t_f$		-	10	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 7.5\text{ V}, R_g = 1\text{ }\Omega$	-	20	40	
Rise time	$t_r$		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	28	60	
Fall time	$t_f$		-	11	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	187	A
Pulse diode forward current	$I_{SM}$		-	-	200	
Body diode voltage	$V_{SD}$	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$	-	0.74	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	70	140	ns
Body diode reverse recovery charge	$Q_{rr}$		-	130	260	nC
Reverse recovery fall time	$t_a$		-	43	-	ns
Reverse recovery rise time	$t_b$		-	27	-	

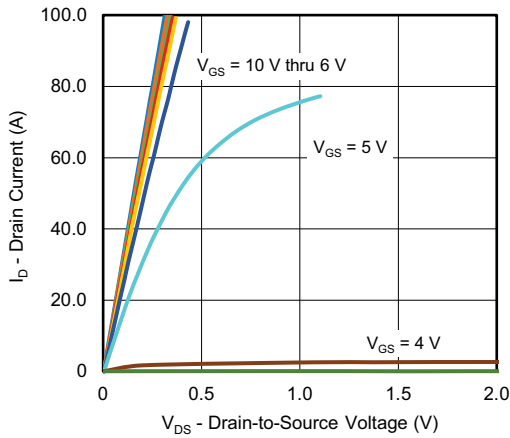
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

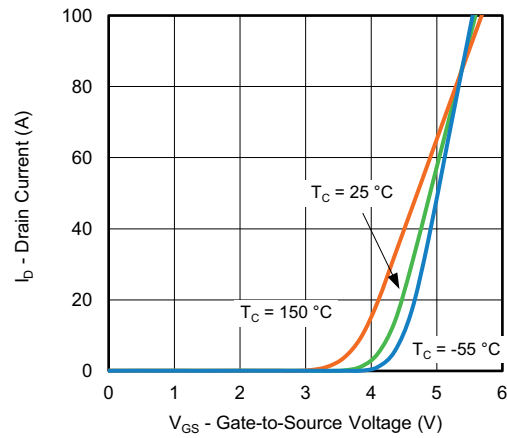
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



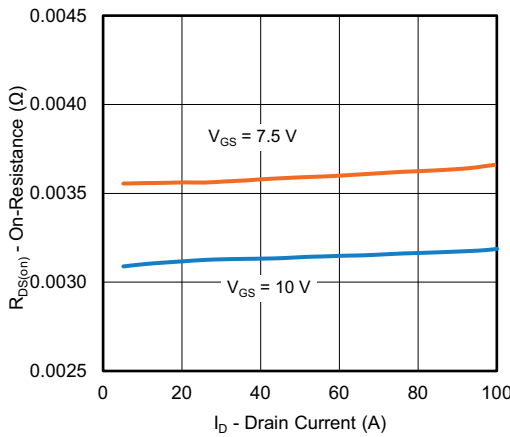
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



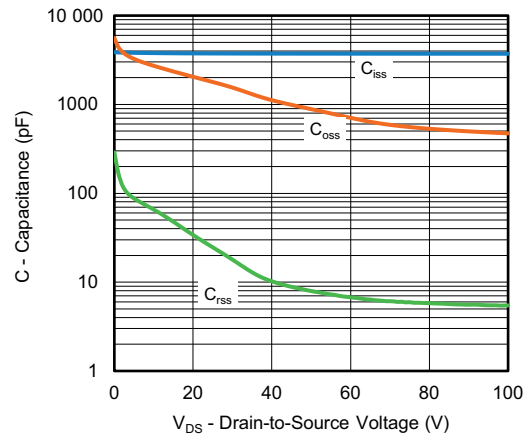
Output Characteristics



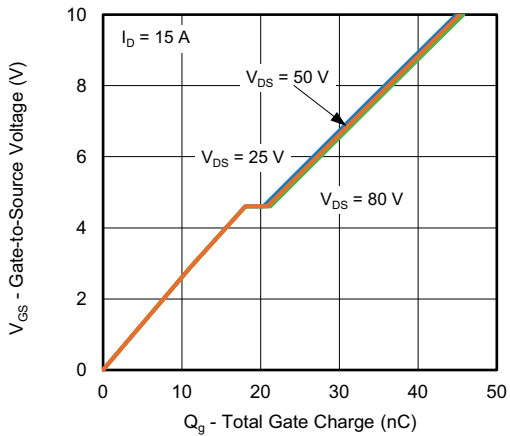
Transfer Characteristics



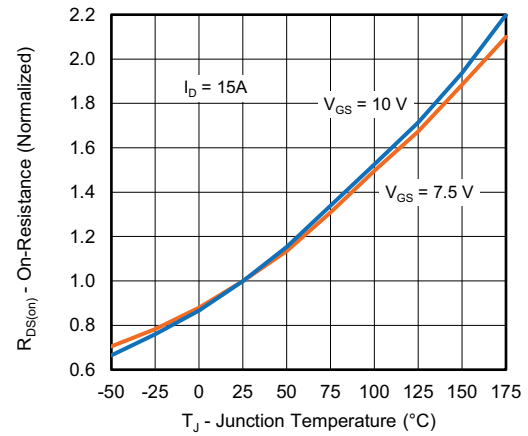
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



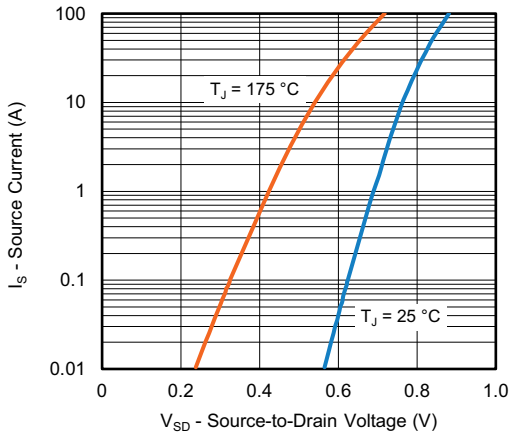
Gate Charge



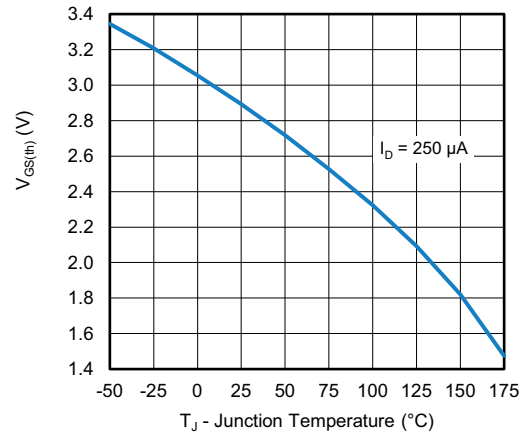
On-Resistance vs. Junction Temperature



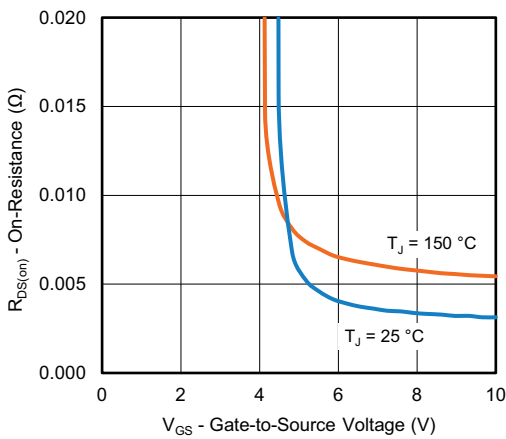
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



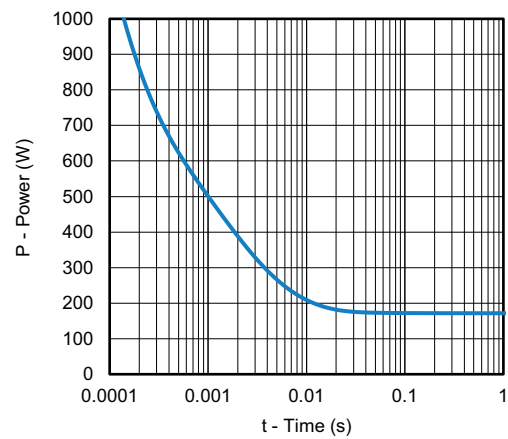
Source-Drain Diode Forward Voltage



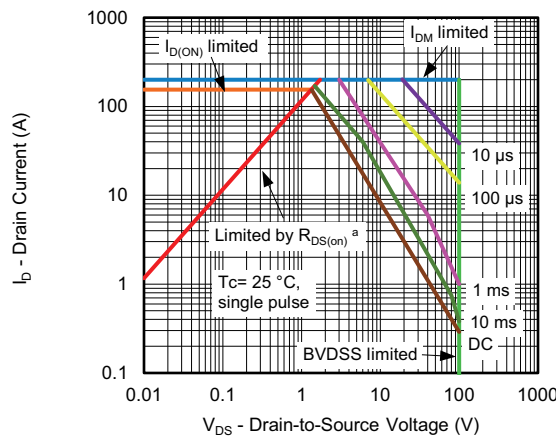
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



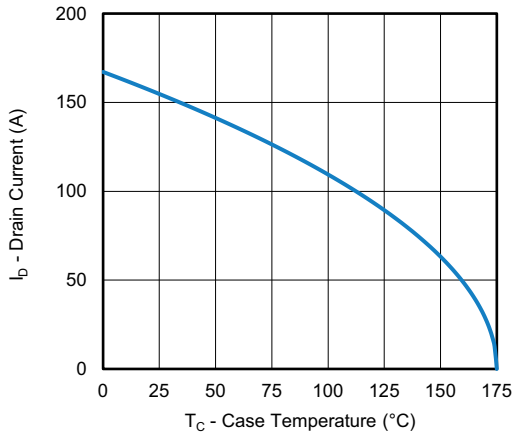
Safe Operating Area, Junction-to-Case

Note

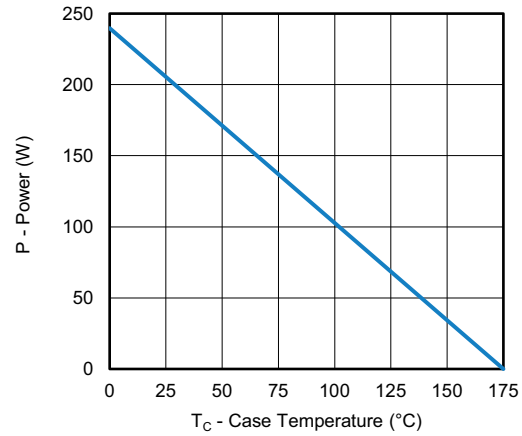
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



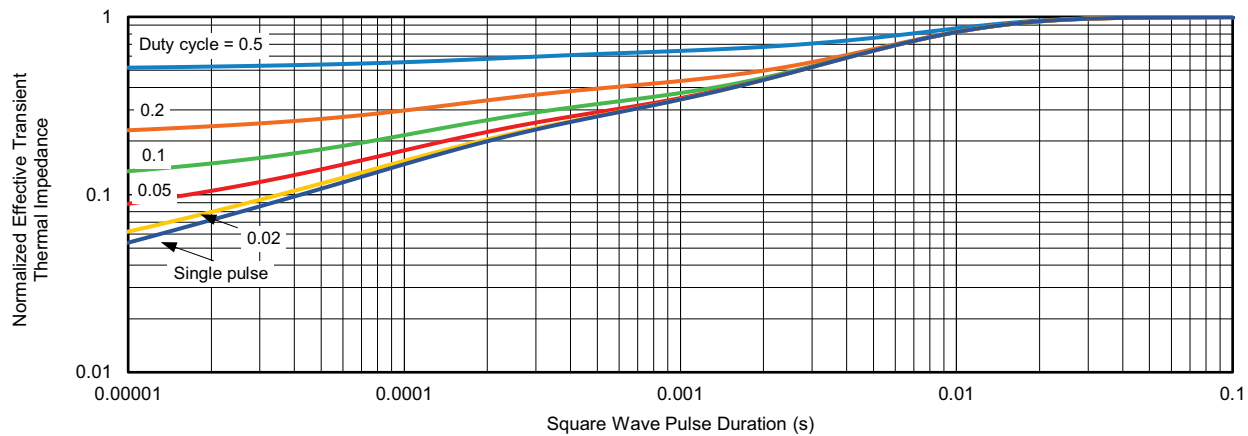
Current Derating <sup>a</sup>



Power, Junction-to-Case

Note

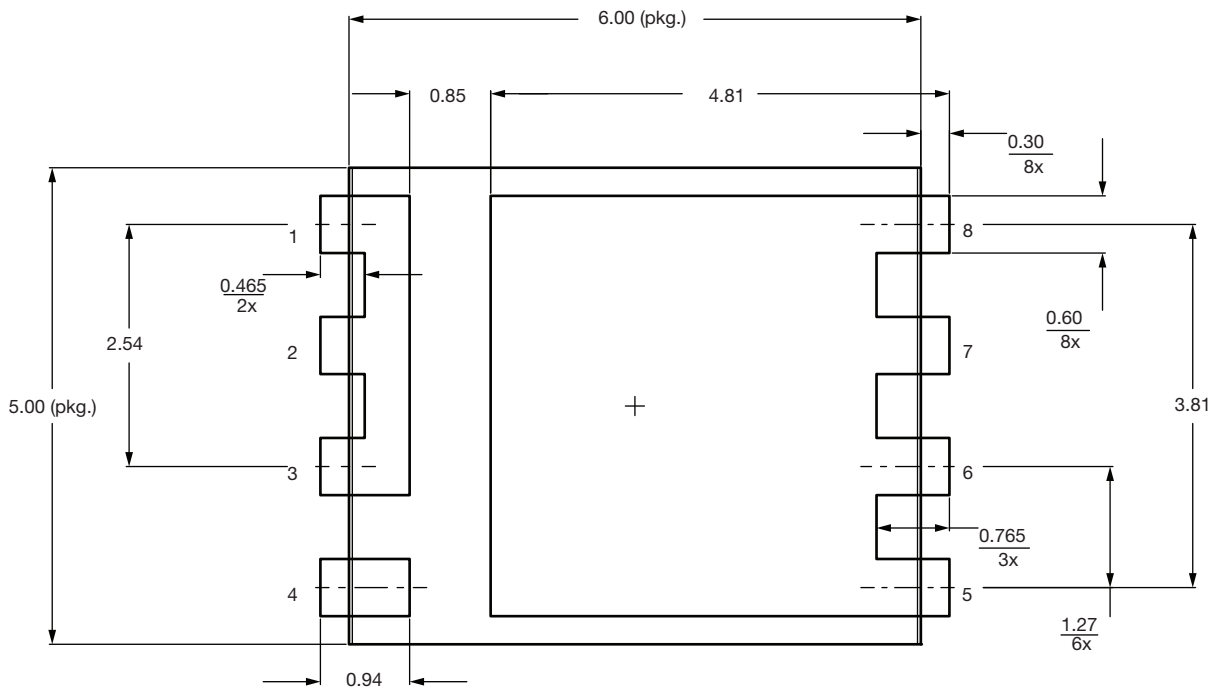
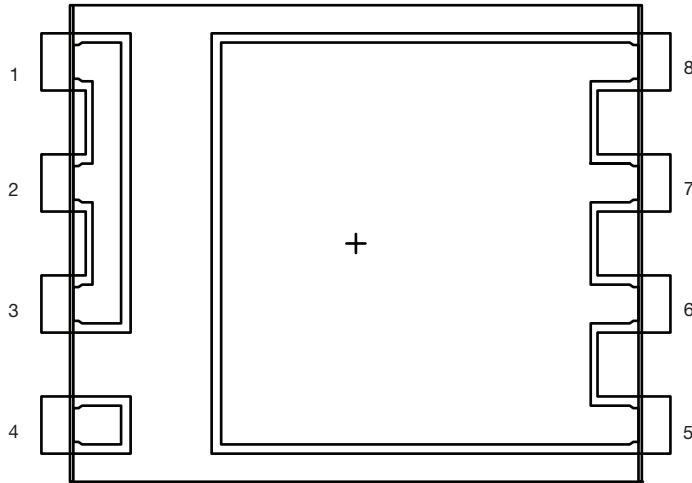
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



Normalized Thermal Transient Impedance, Junction-to-Case

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## Recommended Land Pattern PowerPAK® SO-8SW (PKSO8SWSCCL)



**Note**

- Dimensions in mm

ECN: C24-0483-Rev. A, 20-May-2024  
 DWG: 3027



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