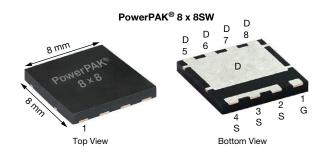
Vishay Siliconix

RoHS

COMPLIANT

HALOGEN FREE

N-Channel 100 V (D-S) 175 °C MOSFET



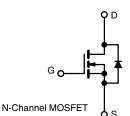
PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.00225			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5 \text{ V}$	0.0029			
Q _g typ. (nC)	95			
I _D (A) ^a	267			
Configuration	Single			

FEATURES

- TrenchFET® Gen III power MOSFET
- · Wettable flanks enhances solderability
- Fully lead (Pb)-free device
- Very low R_{DS(on)}
- Very low R_{thJC}
- PowerPAK® 8 x 8 with fuse lead to increase current density
- 100 % R_q and UIS tested
- Up to 322 A maximum continuous drain current
- Optimized safe operating area / SOA
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Hot swap
- · Load switch
- Oring
- Motor drive
- · Battery management



ORDERING INFORMATION	
Package	PowerPAK® 8 x 8SW
Lead (Pb)-free and halogen-free	SiEH3114EW-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, ur PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100	_	
Gate-source voltage		V _{GS}	± 20	V	
Continuous drain current (T _J = 175 °C)	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 70 ^{\circ}{\rm C}$		267 223		
	T _A = 25 °C	I _D	24 ^b		
T _A = 70 °C Pulsed drain current (t = 100 μs)		I _{DM}	20 ^b 700	Α	
Continuous source-drain diode current	$T_C = 25 ^{\circ}C$ $T_A = 25 ^{\circ}C$	I _S	379 3.1 ^b		
Single pulse avalanche current		I _{AS}	87		
Single pulse avalanche energy L = 0.1 mH		E _{AS}	380	mJ	
Maximum power dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P _D	417 292 3.4 ^b 2.4 ^b	W	
Operating junction and storage temperature range		T _J , T _{stq}	-55 to +175	°C	
Soldering recommendations (peak temperature) ^c			260		

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient ^b	Steady state	R_{thJA}	33	44	°C/W	
Maximum junction-to-case (drain)	Steady state	Rthuc	0.27	0.36	C/VV	

Notes

a. $T_C = 25 \,^{\circ}C$

Surface mounted on 1" x 1" FR4 board

See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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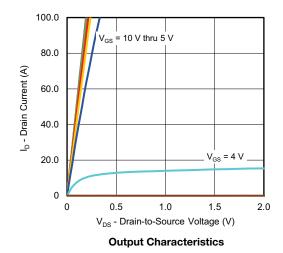
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA	-	64	-	m\//0/	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-8.5	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	-	4	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20$	-	-	± 100	nA	
Zero gate voltage drain current		V _{DS} = 100 V, V _{GS} =0 V	-	-	1	μА	
	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15		
Drain-source on-state resistance ^a	5	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	0.0021	0.00255		
	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, I_D = 20 \text{ A}$	-	0.0023	0.00290	Ω	
Forward transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 40 \text{ A}$	-	115	-	S	
Dynamic ^b			l			L	
Input capacitance	C _{iss}		-	5465	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	2290	-		
Reverse transfer capacitance	C _{rss}			82	-		
Total colored con	0	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	95	142	nC	
Total gate charge	Qg	V _{DS} = 50 V, V _{GS} = 7.5 V, I _D =20 A	-	73	110		
Gate-source charge	Q _{gs}		-	25	-		
Gate-drain charge	Q _{gd}		-	19	-		
Gate resistance	R_{g}	f = 1 MHz	1.1	5.5	11	Ω	
Turn-on delay time	t _{d(on)}		-	16	32		
Rise time	t _r	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega, I_D \cong 10 \text{ A},$	-	25	50		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	88	180		
Fall time	t _f		-	37	80		
Turn-on delay time	t _{d(on)}		-	20	40	ns	
Rise time	t _r	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega, I_D \cong 10 \text{ A},$	-	53	105	= =	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	75	150		
Fall time	t _f		-	37	80		
Drain-Source Body Diode Characteristi	cs						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	379	_	
Pulse diode forward current	I _{SM}		-	-	700	_ A	
Body diode voltage	V_{SD}	$I_S = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.72	1.1	V	
Body diode reverse recovery time	t _{rr}		-	95	190	ns	
Body diode reverse recovery charge	Q _{rr}	1 40 A 41/44 400 A / - T 05 00	-	260	520	nC	
Reverse recovery fall time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	59	-		
Reverse recovery rise time	t _b		-	36	_	ns	

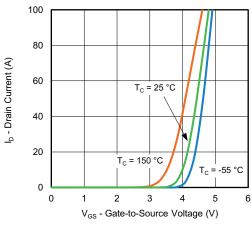
Notes

- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

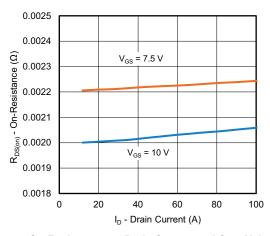


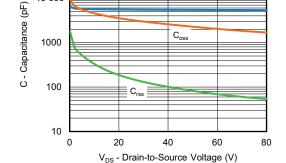






Ciss



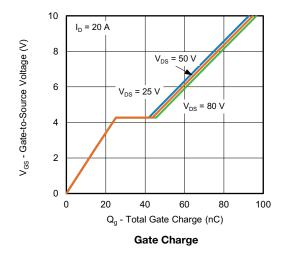


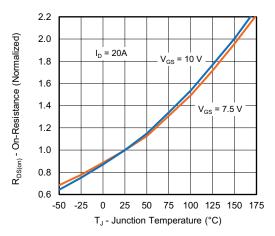
100 000

10 000

On-Resistance vs. Drain Current and Gate Voltage

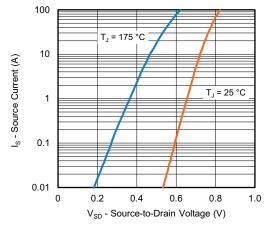




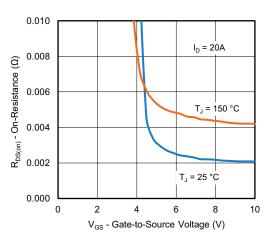


On-Resistance vs. Junction Temperature

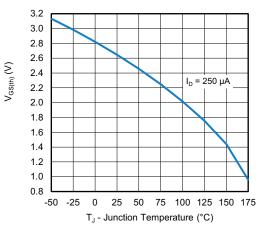




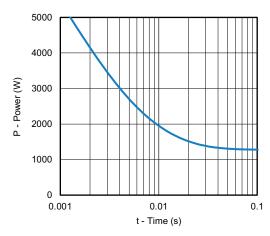
Source-Drain Diode Forward Voltage



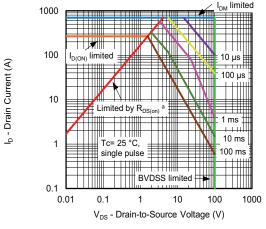
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Case

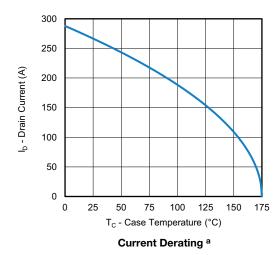


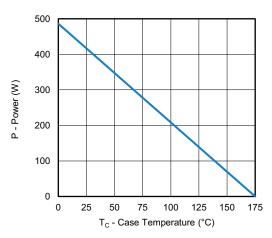
Safe Operating Area, Junction-to-Case

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified





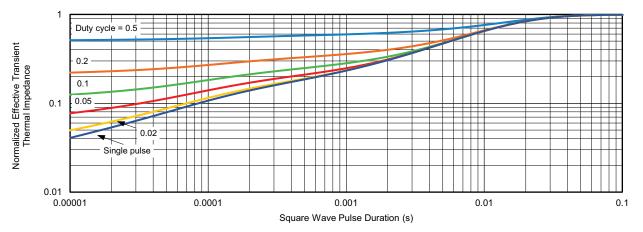


Power, Junction-to-Case

Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?61778.



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