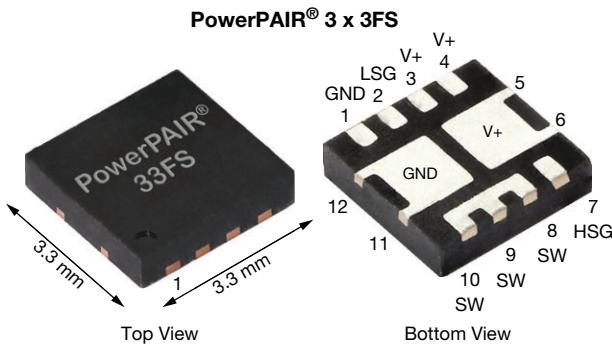


Dual N-Channel 70 V (D-S) MOSFET



FEATURES

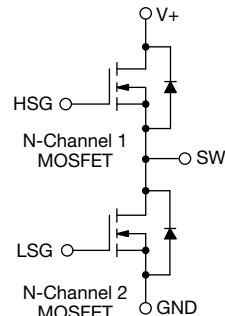
- TrenchFET® Gen IV power MOSFET
- Symmetric dual n-channel
- Flip chip technology optimal thermal design
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized $R_{DS(on)}$ - Q_g and $R_{DS(on)}$ - Q_{gd} FOM elevates efficiency for high frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck
- Computer / server peripherals
- Half bridge
- POL
- Telecom DC/DC



PRODUCT SUMMARY	
V_{DS} (V)	70
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.020
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 3.3$ V	0.024
Q_g typ. (nC) at $V_{GS} = 3.3$ V	5.2
I_D (A)	34.6 ^a
Configuration	Dual

ORDERING INFORMATION

Package	PowerPAIR 3 x 3FS
Lead (Pb)-free, halogen-free, and IOL	SiZF458LDT-T1-UE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	70	
Gate-source voltage	V_{GS}	± 12	V
Continuous drain current ($V_{GS} = 10$ V, $T_J = 150$ °C)	I_D	34.6 27.7 9.7 ^{b, c} 7.7 ^{b, c}	A
Pulsed drain current ($V_{GS} = 5$ V, $t = 100$ μ s)	I_{DM}	50	
Continuous source current (MOSFET diode conduction)	I_S	47.3 3.4 ^{b, c}	
Single pulse avalanche current	I_{AS}	10	
Single pulse avalanche energy	E_{AS}	7.2	mJ
Maximum power dissipation	P_D	48.1 30.8 3.8 ^{b, c} 2.4 ^{b, c}	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)		260	

Notes

- a. $T_C = 25$ °C
- b. Surface mounted on 1" x 1" FR4 board
- c. $t = 10$ s

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient a, b	$t \leq 10 \text{ s}$	R_{thJA}	26	33	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	2	2.6	°C/W

Notes

a. Surface mounted on 1" x 1" FR4 board
b. Maximum under steady state conditions is 67 °C/W

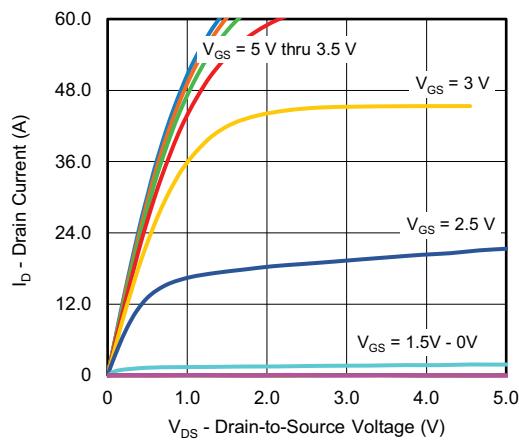
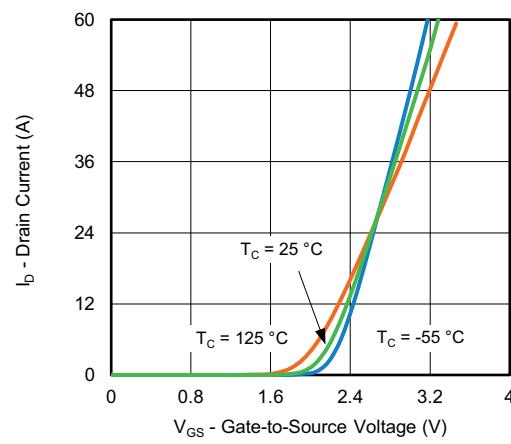
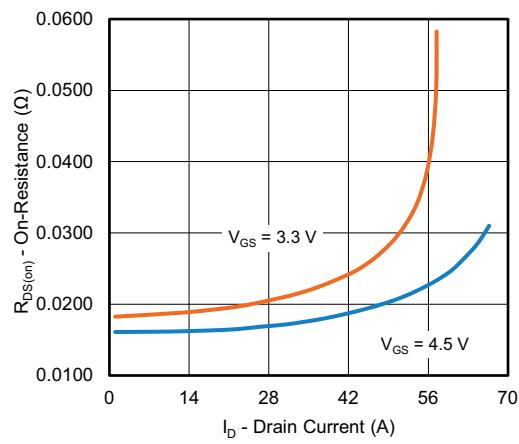
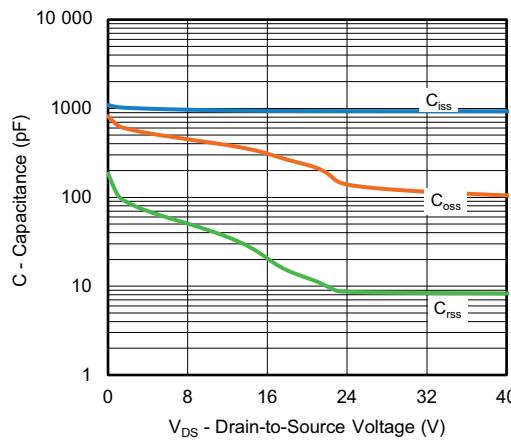
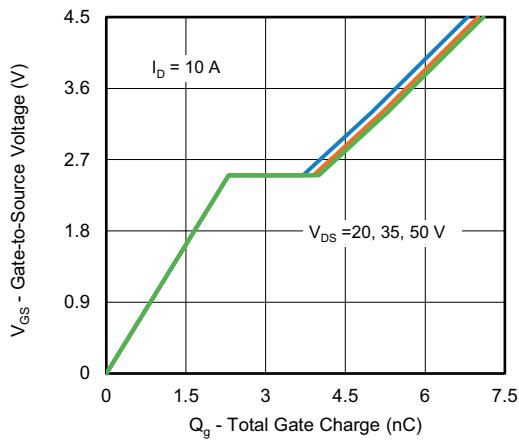
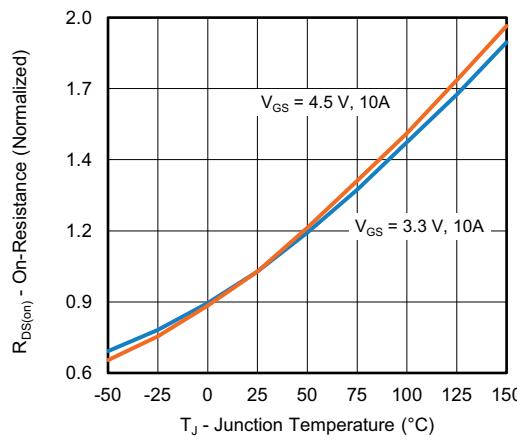
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

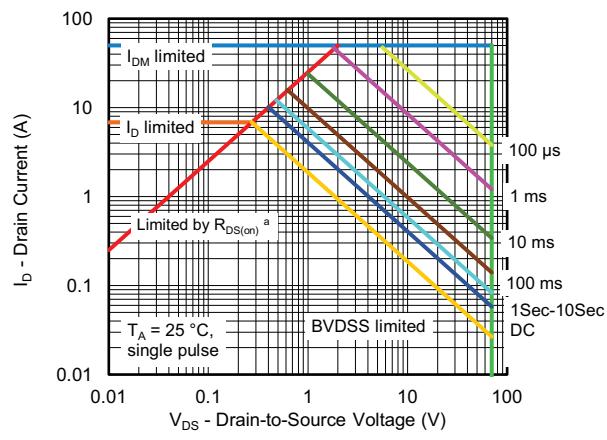
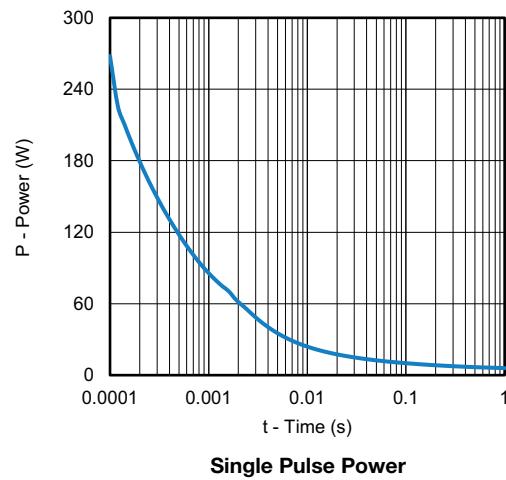
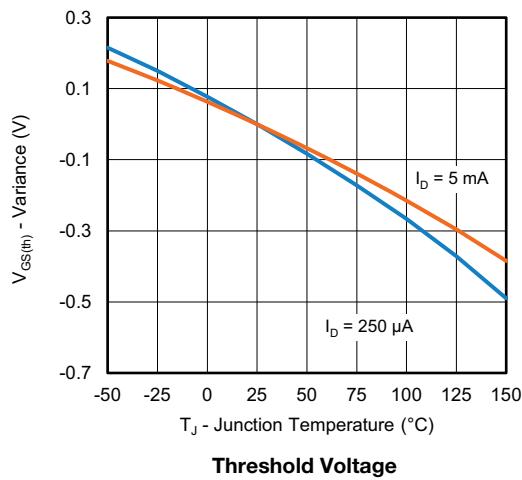
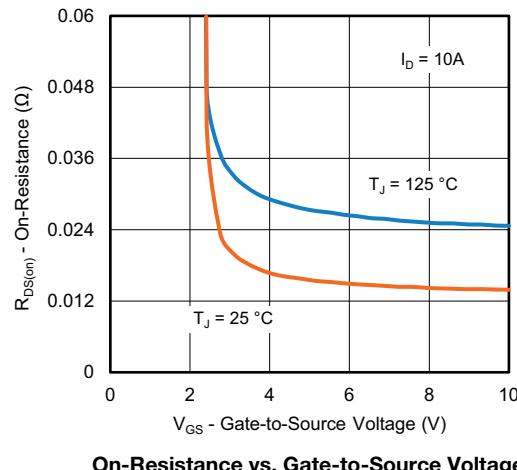
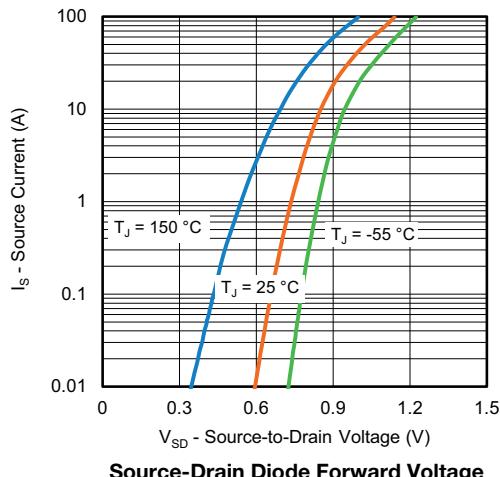
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	70	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10 \text{ mA}$	-	45	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu\text{A}$	-	-3.4	-	mV/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.6	-	1.6	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 70 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	
		$V_{DS} = 70 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 75 \text{ °C}$	-	-	10	μA
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.0163	0.020	
		$V_{GS} = 3.3 \text{ V}, I_D = 10 \text{ A}$	-	0.0189	0.024	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	40	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 35 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	930	-	pF
Output capacitance	C_{oss}		-	111	-	
Reverse transfer capacitance	C_{rss}		-	8.5	-	
Output charge	Q_{oss}	$V_{DS} = 35 \text{ V}, V_{GS} = 0 \text{ V}$	-	10.6	-	nC
Total gate charge	Q_g	$V_{DS} = 35 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	7	11	nC
			-	5.2	8	
Gate-source charge	Q_{gs}	$V_{DS} = 35 \text{ V}, V_{GS} = 3.3 \text{ V}, I_D = 10 \text{ A}$	-	2.3	-	
Gate-drain charge	Q_{gd}		-	1.6	-	
Gate resistance	R_g	$f = 1 \text{ MHz}$	0.4	0.95	1.7	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 35 \text{ V}, R_L = 3.5 \Omega, I_D \geq 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	12	24	ns
Rise time	t_r		-	16	32	
Turn-off delay time	$t_{d(off)}$		-	18	36	
Fall time	t_f		-	5	10	
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-	-	47.3	A
Pulse diode forward current	I_{SM}		-	-	50	
Body diode voltage	V_{SD}	$I_S = 5 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.78	1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = 10 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	-	22	44	ns
Body diode reverse recovery charge	Q_{rr}		-	15	30	nC
Reverse recovery fall time	t_a		-	14	-	ns
Reverse recovery rise time	t_b		-	8	-	

Notes

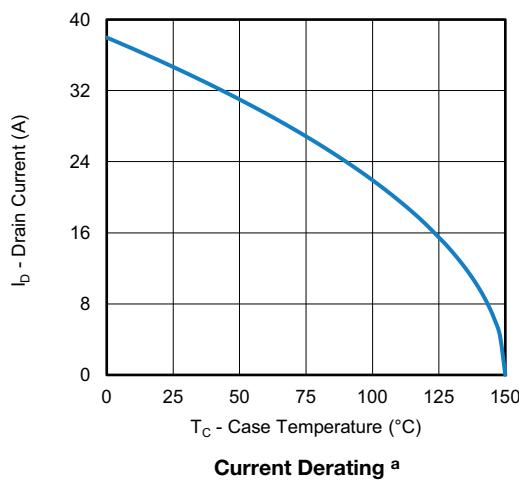
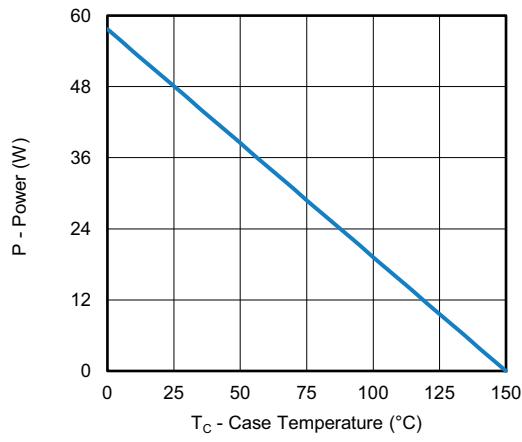
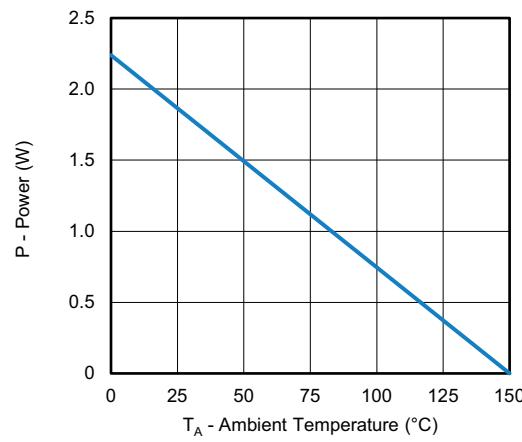
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

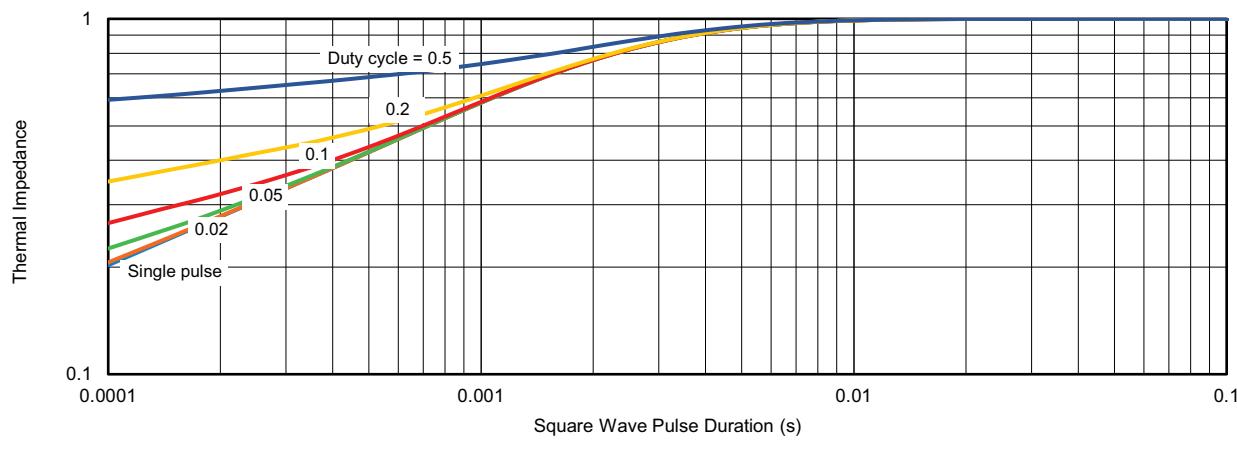
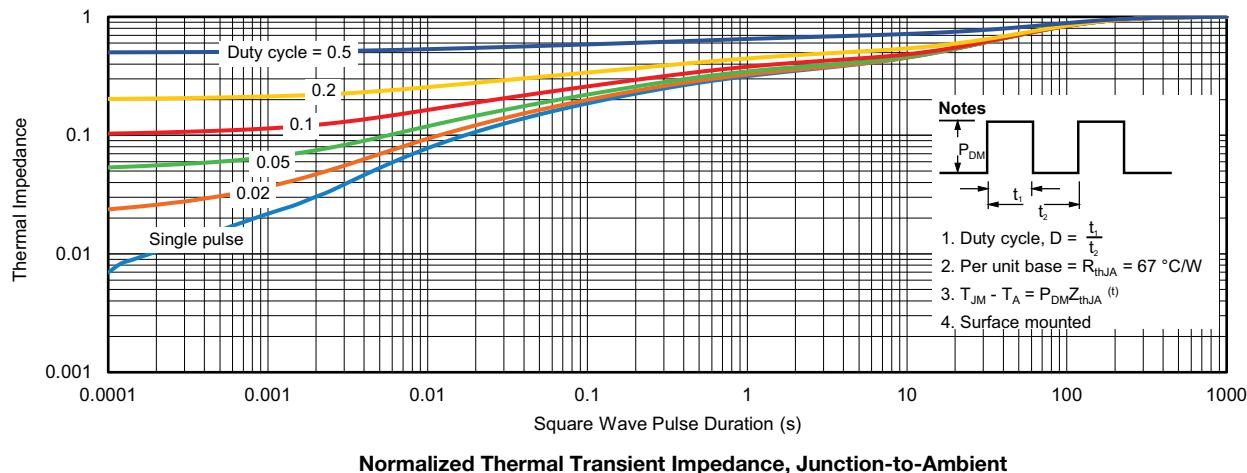
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Notes

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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