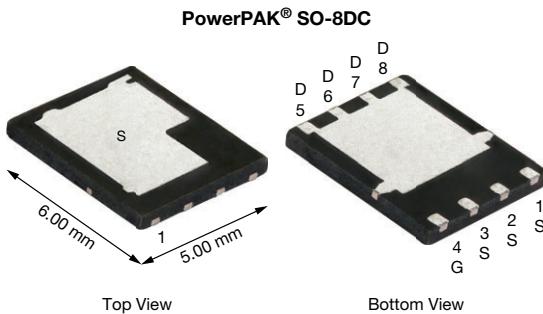


N-Channel 20 V (D-S) MOSFET



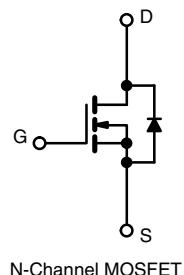
FEATURES

- TrenchFET® power MOSFET
- Top side cooling feature provides additional venue for thermal transfer
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converters
- OR-ing
- Power supplies
- Motor drive control
- Battery and load switch



PRODUCT SUMMARY	
V_{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00041
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0005
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.00120
Q_g typ. (nC)	95
I_D (A)	467 a
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR178DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	-8 / +12	
Continuous drain current ($T_J = 150$ °C)	I_D	467	A
		373	
		104 b, c	
		8.3 b, c	
Pulsed drain current ($V_{GS} = 10$ V, $t = 100$ μ s)	I_{DM}	500	
Continuous source-drain diode current	I_S	113	
		5.6 b, c	
Single pulse avalanche current	I_{AS}	80	mJ
Single pulse avalanche energy	E_{AS}	320	
Maximum power dissipation	P_D	125	W
		80	
		6.25 b, c	
		4 b, c	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) d		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.8	1	
Maximum junction-to-case (source)	R_{thJC}	1.1	1.4	

Notes

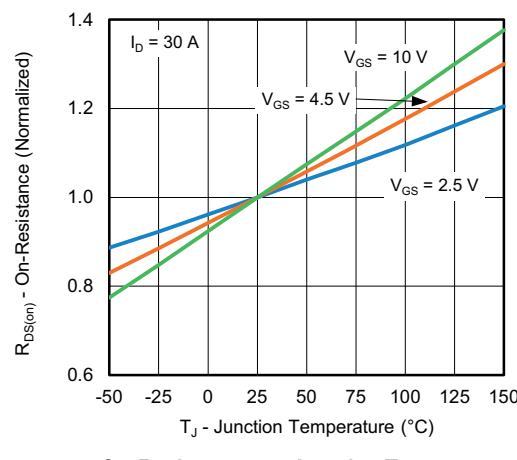
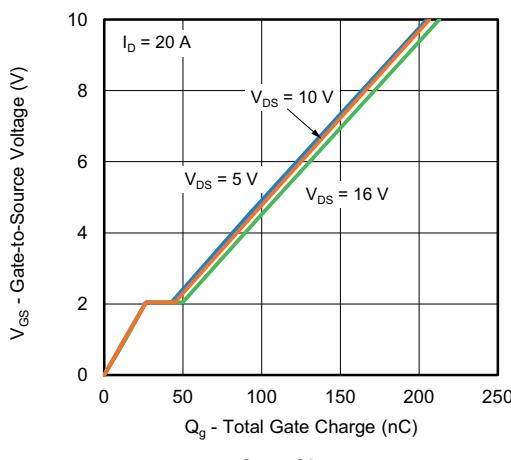
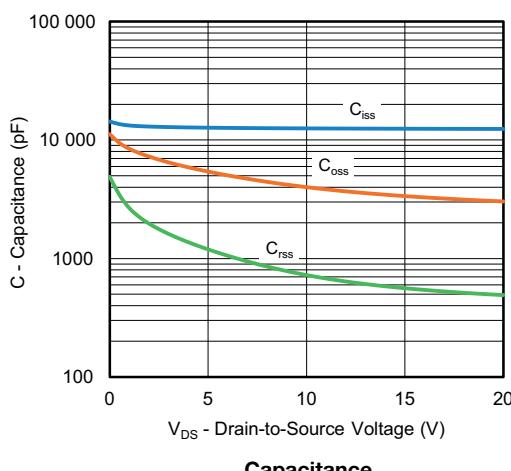
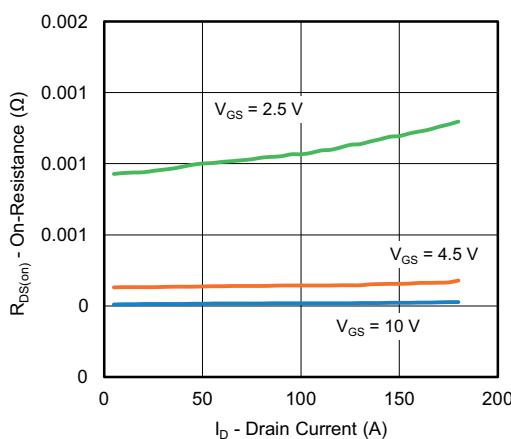
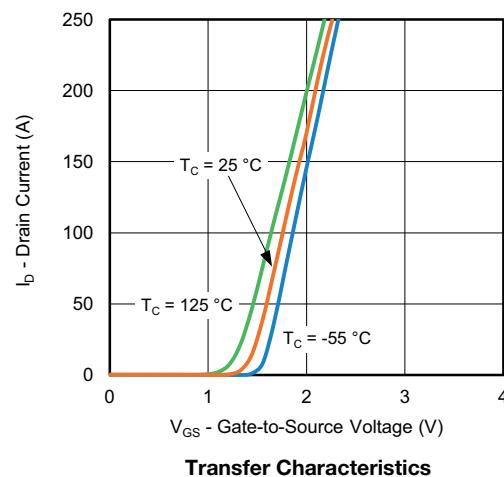
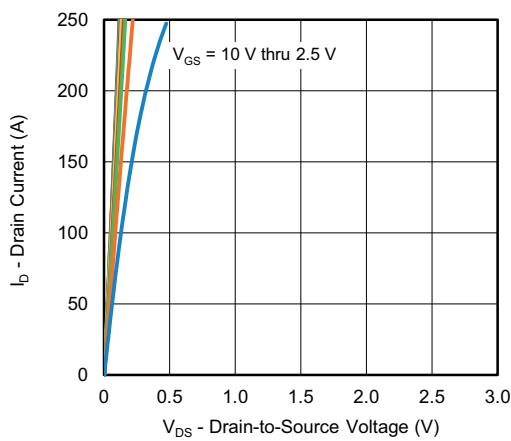
- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?273257). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W

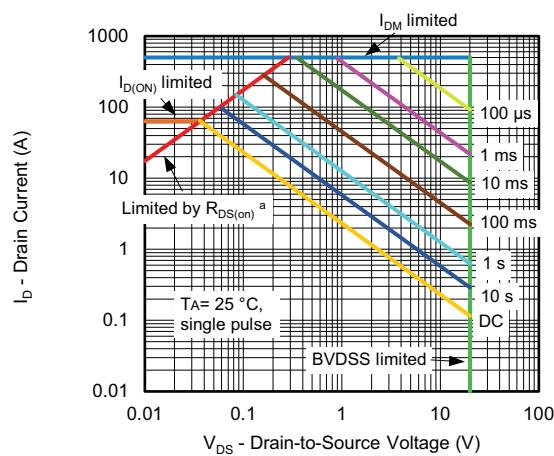
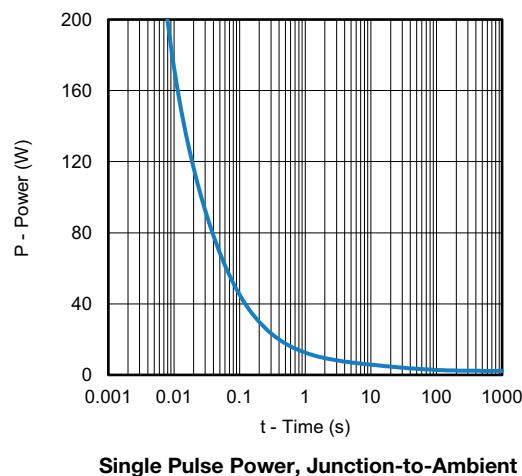
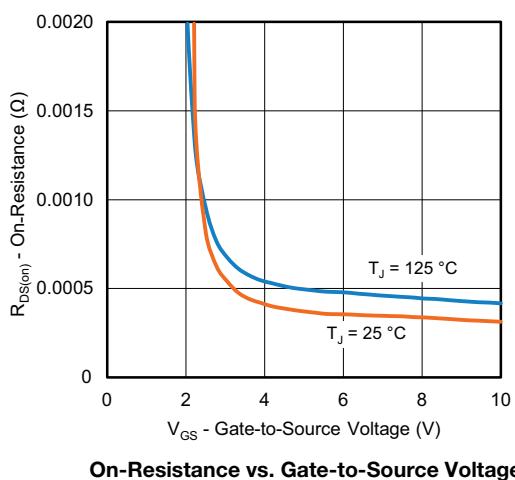
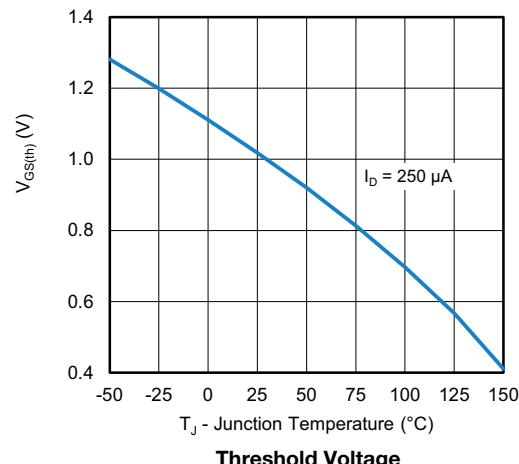
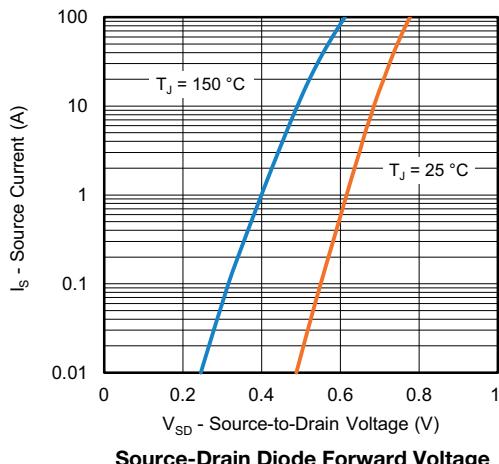
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10 \text{ mA}$	-	14	-	$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$	$I_D = 250 \mu\text{A}$	-	-4.4	-	
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	0.6	-	1.5	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = -8 \text{ V} / +12 \text{ V}$	-	-	± 150	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 70^\circ\text{C}$	-	-	15	
On-state drain current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 10 \text{ V}$, $V_{GS} = 10 \text{ V}$	20	-	-	A
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$	-	0.00033	0.00041	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 30 \text{ A}$	-	0.00041	0.0005	
		$V_{GS} = 2.5 \text{ V}$, $I_D = 30 \text{ A}$	-	0.00090	0.0012	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 50 \text{ A}$	-	295	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	12 430	-	pF
Output capacitance	C_{oss}		-	4070	-	
Reverse transfer capacitance	C_{rss}		-	740	-	
Total gate charge	Q_g	$V_{DS} = 10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$	-	207	310	nC
		$V_{DS} = 10 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 20 \text{ A}$	-	95	143	
Gate-source charge	Q_{gs}		-	26.6	-	
Gate-drain charge	Q_{gd}		-	18.219	-	
Output charge	Q_{oss}	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	62	-	
Gate resistance	R_g	$f = 1 \text{ MHz}$	0.2	0.94	1.9	Ω
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}$, $R_L = 1 \Omega$, $I_D \geq 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$	-	17	40	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(\text{off})}$		-	83	170	
Fall time	t_f		-	14	30	
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}$, $R_L = 1 \Omega$, $I_D \geq 10 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$	-	44	90	
Rise time	t_r		-	100	130	
Turn-off delay time	$t_{d(\text{off})}$		-	128	260	
Fall time	t_f		-	39	80	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-	-	113	A
Pulse diode forward current	I_{SM}		-	-	500	
Body diode voltage	V_{SD}	$I_S = 10 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	0.7	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	-	60	90	ns
Body diode reverse recovery charge	Q_{rr}		-	90	110	
Reverse recovery fall time	t_a		-	27	-	ns
Reverse recovery rise time	t_b		-	19	-	

Notes

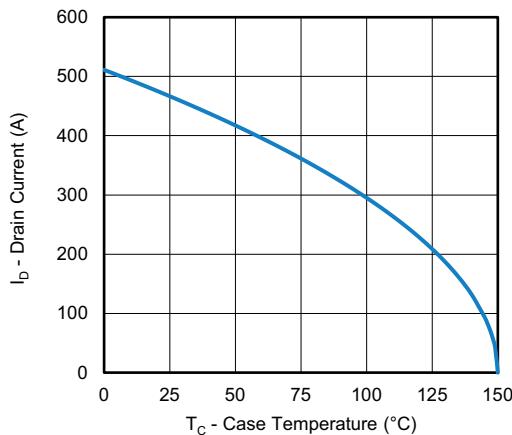
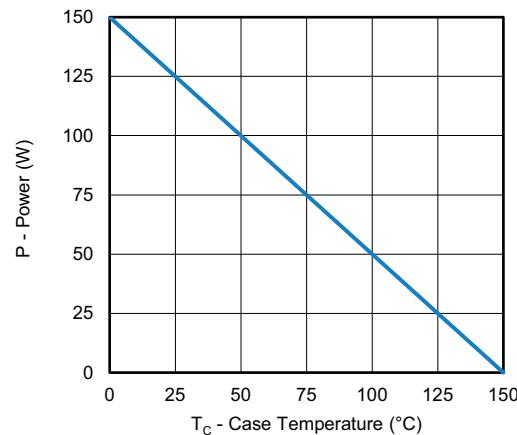
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

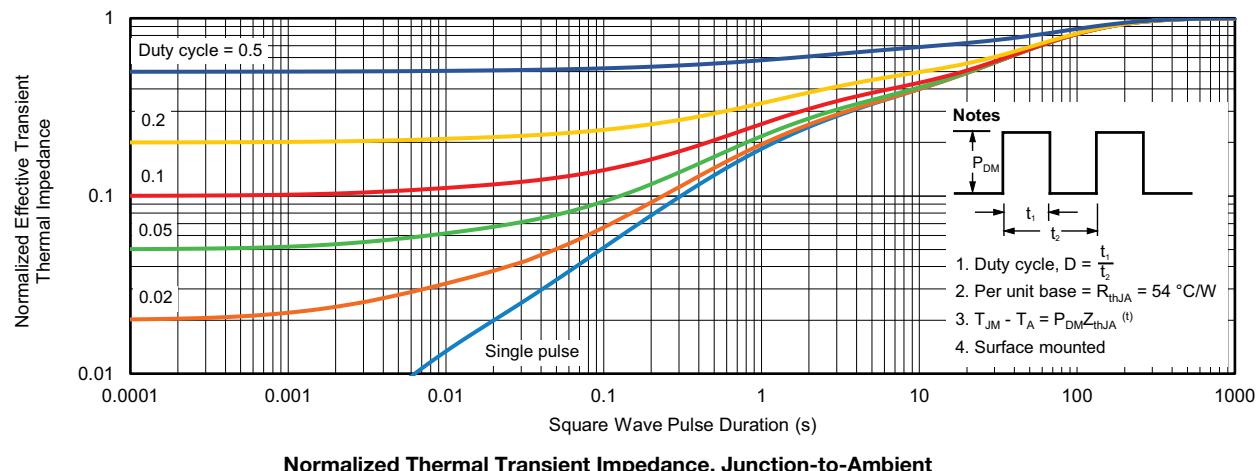
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


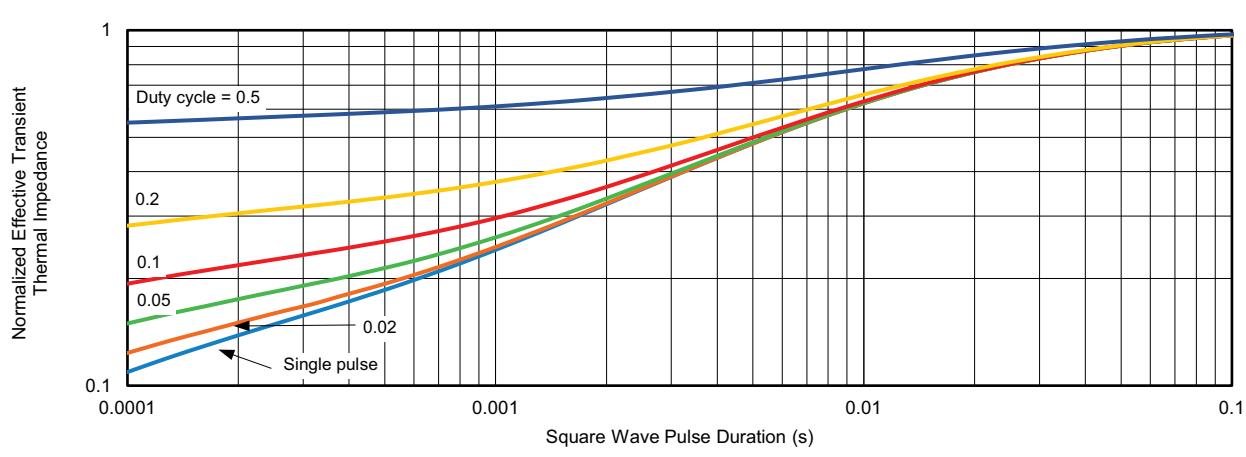
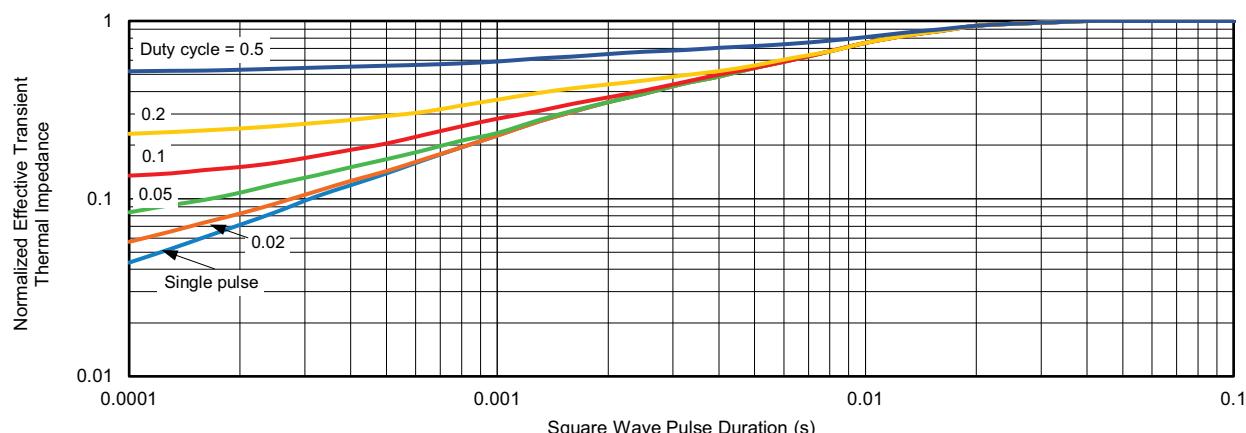
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit


Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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