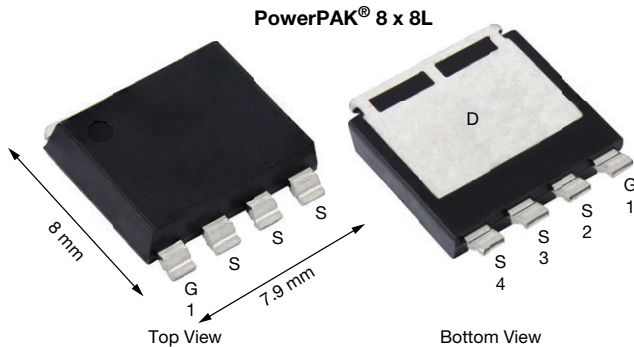


## N-Channel 100 V (D-S) 175 °C MOSFET



### FEATURES

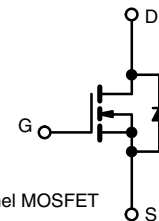
- TrenchFET® Gen V power MOSFET
- Fully lead (Pb)-free device
- Very low  $R_{DS} \times Q_g$  figure of merit (FOM)
- Up to 277 A maximum continuous drain current
- 50 % smaller footprint than D<sup>2</sup>PAK (TO-263)
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- OR-ing
- Motor drive control
- Battery management



N-Channel MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00189
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.00214
$Q_g$ typ. (nC)	85
$I_D$ (A) <sup>a</sup>	277
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SIJH5100E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	100	V	
Gate-source voltage	$V_{GS}$	$\pm 20$	V	
Continuous drain current ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	277	A
		$T_C = 70$ °C	232	
		$T_A = 25$ °C	28 <sup>b</sup>	
		$T_A = 70$ °C	23 <sup>b</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	500	A	
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	303	A
		$T_A = 25$ °C	3 <sup>b</sup>	
Single pulse avalanche current	$I_{AS}$	65	A	
Single pulse avalanche energy	$E_{AS}$	210	mJ	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	333	W
		$T_C = 70$ °C	233	
		$T_A = 25$ °C	3.3 <sup>b</sup>	
		$T_A = 70$ °C	2.3 <sup>b</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	36	45	°C/W
Maximum junction-to-case (drain)				
	$R_{thJC}$	0.36	0.45	

### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	100	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	76	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-9.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20$	-	-	100	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 70\text{ }^\circ\text{C}$	-	-	15	
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$	-	0.0016	0.00189	$\Omega$
		$V_{GS} = 7.5\text{ V}$ , $I_D = 20\text{ A}$	-	0.0018	0.00214	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 75\text{ A}$	-	120	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	-	6900	-	pF
Output capacitance	$C_{oss}$		-	2240	-	
Reverse transfer capacitance	$C_{rss}$		-	23	-	
Total gate charge	$Q_g$	$V_{DS} = 50\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$	-	85	128	nC
		$V_{DS} = 50\text{ V}$ , $V_{GS} = 7.5\text{ V}$ , $I_D = 20\text{ A}$	-	63	95	
Gate-source charge	$Q_{gs}$		-	31	-	
Gate-drain charge	$Q_{gd}$		-	5.3	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.32	1.6	3.2	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$ , $R_L = 5\text{ }\Omega$ , $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	-	20	40	ns
Rise time	$t_r$		-	12	25	
Turn-off delay time	$t_{d(off)}$		-	45	90	
Fall time	$t_f$		-	21	40	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$ , $R_L = 5\text{ }\Omega$ , $I_D \cong 10\text{ A}$ , $V_{GEN} = 7.5\text{ V}$ , $R_g = 1\text{ }\Omega$	-	24	50	
Rise time	$t_r$		-	17	35	
Turn-off delay time	$t_{d(off)}$		-	41	80	
Fall time	$t_f$		-	21	40	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	303	A
Pulse diode forward current	$I_{SM}$		-	-	500	
Body diode voltage	$V_{SD}$	$I_S = 10\text{ A}$ , $V_{GS} = 0\text{ V}$	-	0.75	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	-	135	270	ns
Body diode reverse recovery charge	$Q_{rr}$		-	220	440	nC
Reverse recovery fall time	$t_a$		-	42	-	ns
Reverse recovery rise time	$t_b$		-	93	-	

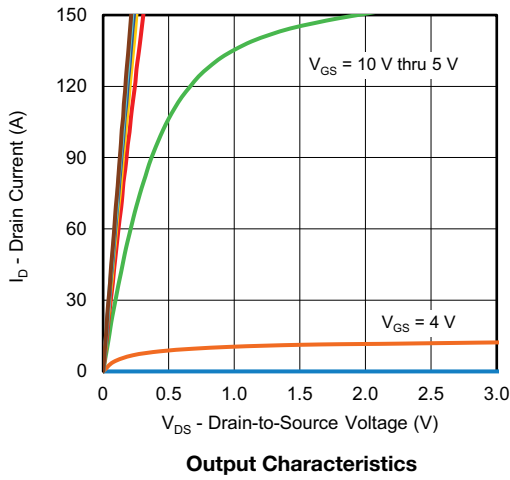
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

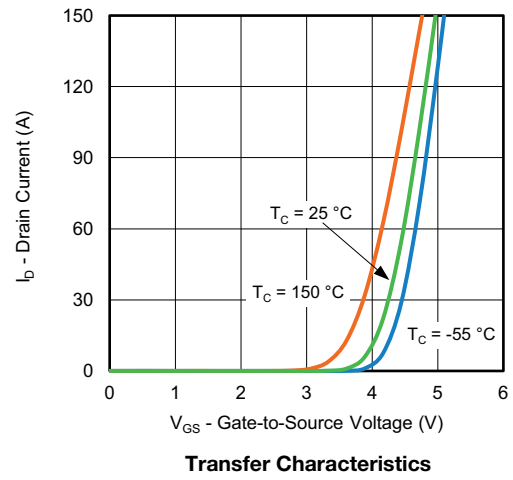
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



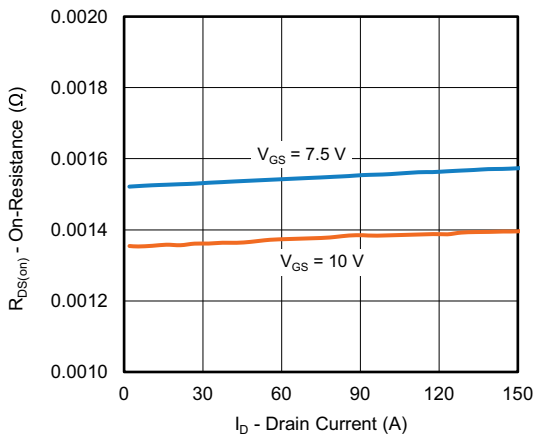
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



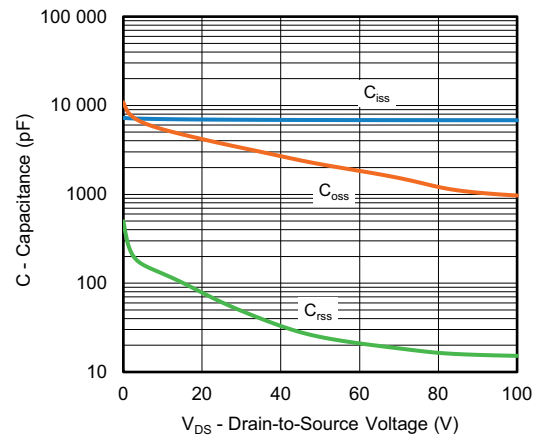
**Output Characteristics**



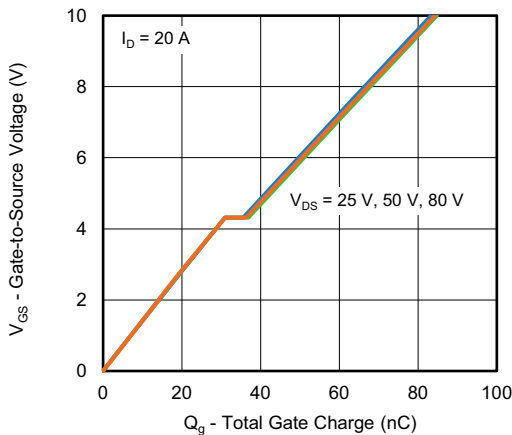
**Transfer Characteristics**



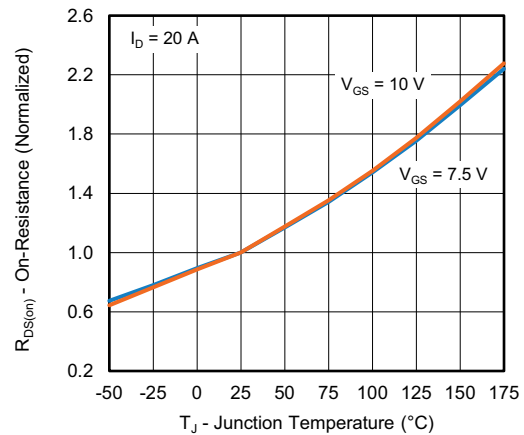
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



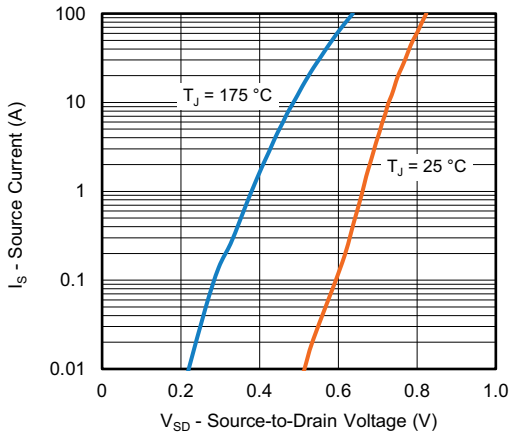
**Gate Charge**



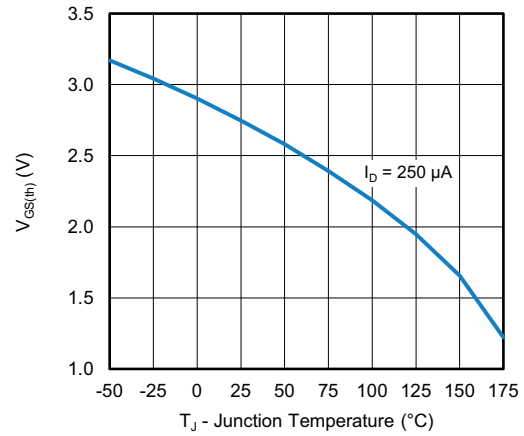
**On-Resistance vs. Junction Temperature**



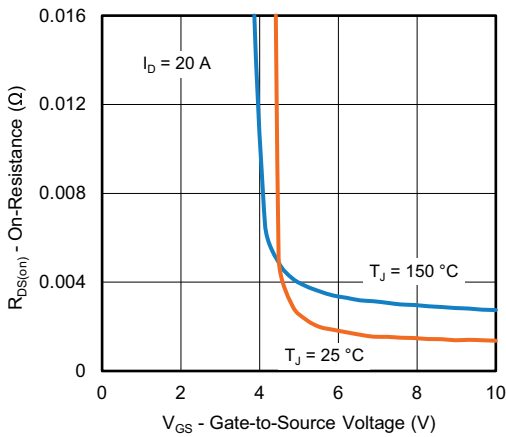
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



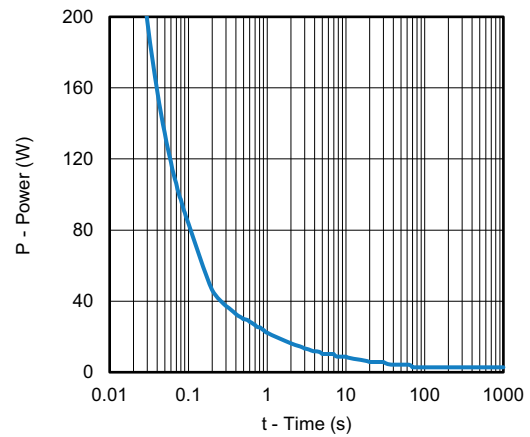
**Source-Drain Diode Forward Voltage**



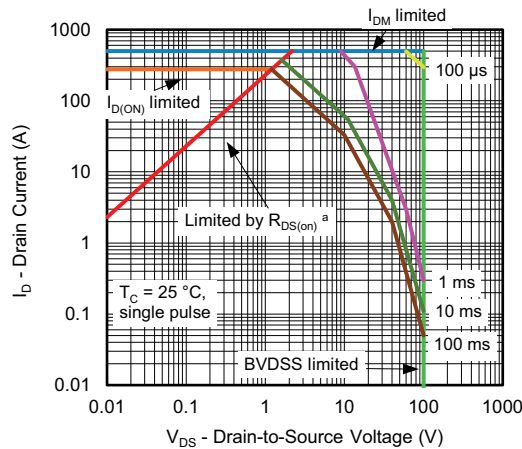
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Ambient**



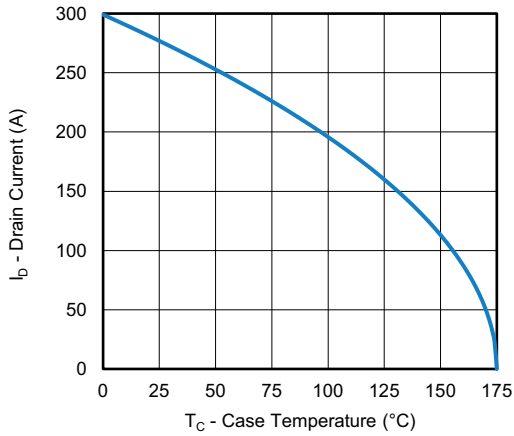
**Safe Operating Area, Junction-to-Ambient**

**Note**

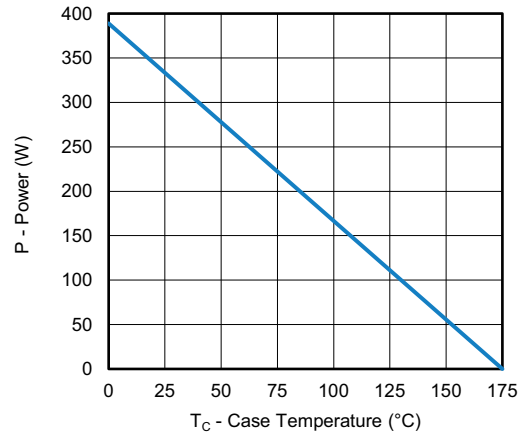
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



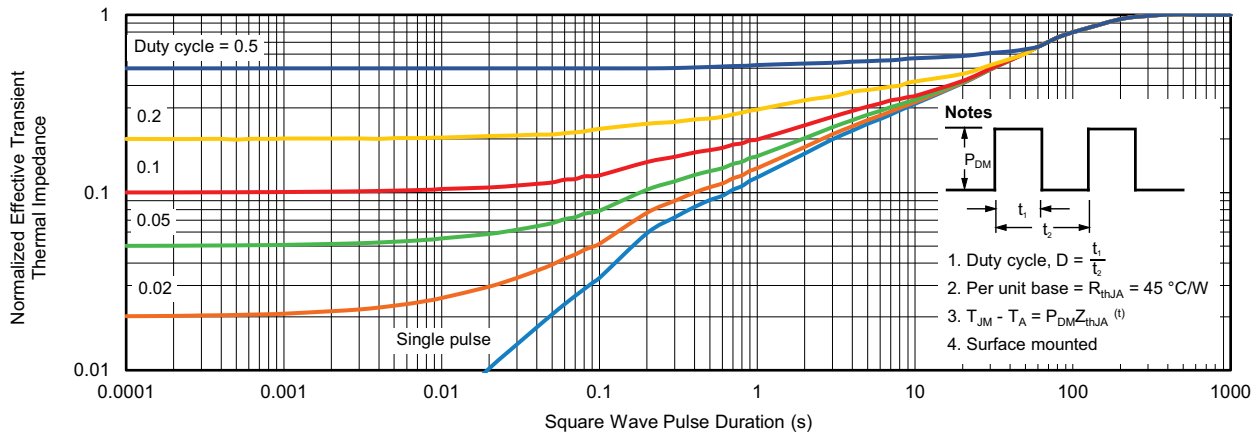
**Power, Junction-to-Case**

**Note**

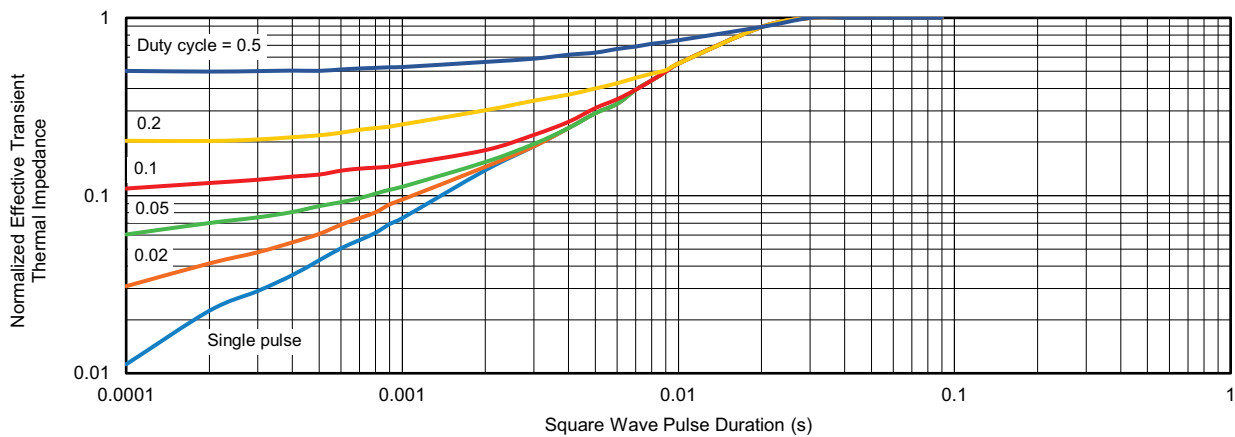
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



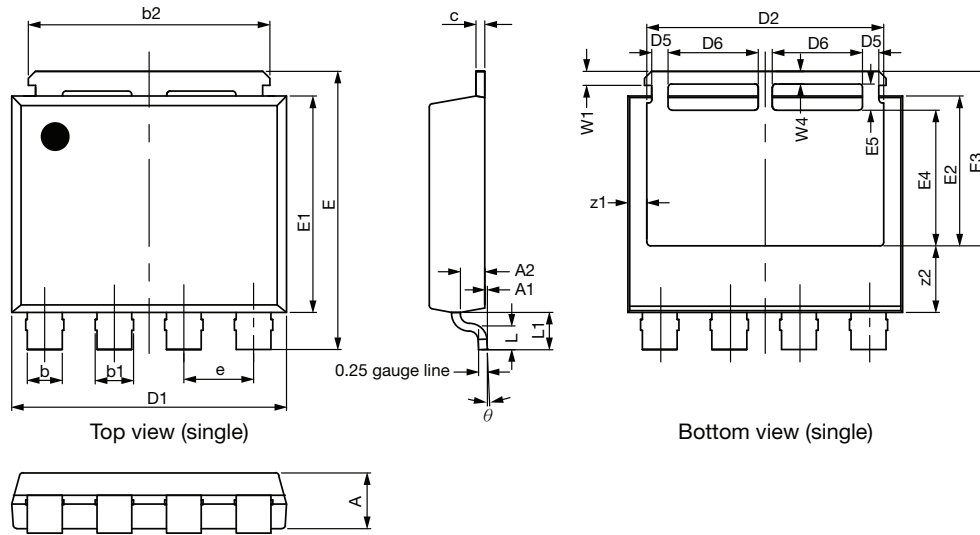
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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### PowerPAK<sup>®</sup> 8 x 8L BWL Case Outline 2



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.50	1.60	1.70	0.059	0.063	0.067
A1	0.00	-	0.127	0.000	-	0.005
A2	0.655	0.705	0.755	0.026	0.028	0.030
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	6.84	6.94	7.04	0.269	0.273	0.277
c	0.20	0.25	0.30	0.008	0.010	0.012
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
e	1.97	2.00	2.03	0.078	0.079	0.080
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	4.21	4.31	4.41	0.166	0.170	0.174
E3	4.92	5.02	5.12	0.194	0.198	0.202
E4	3.80	3.90	4.00	0.150	0.154	0.157
E5	0.65	0.75	0.85	0.026	0.030	0.033
L	0.61	0.68	0.75	0.024	0.027	0.030
L1	1.00	1.07	1.15	0.039	0.042	0.045
W1	0.30	0.40	0.50	0.012	0.016	0.020
W4	0.32	0.37	0.42	0.013	0.015	0.017
z1	0.45	0.55	0.65	0.018	0.022	0.026
z2	1.81	1.91	2.01	0.071	0.075	0.079
θ	0°	-	5°	0°	-	5°

ECN: S19-0643-Rev. B, 05-Aug-2019  
DWG: 6073

**Note**

- Millimeter will govern



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