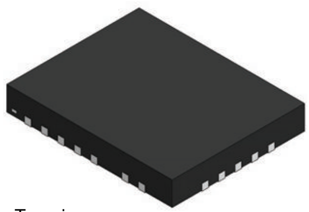
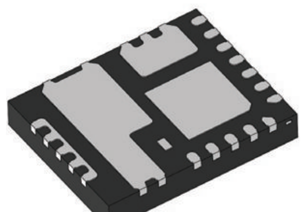
# 40 A VRPower® Smart Power Stage (SPS) Module With Integrated High Accuracy Current and Temperature Monitors


Top view


Bottom view

## DESCRIPTION

The SiC575A is a smart VRPower® device that integrates a high side and low side MOSFET, a high performance driver with integrated bootstrap FET. The SiC575A offers high accuracy current and temperature monitors that can be fed back to the controller and doubler to complete a multiphase DC/DC system. They simplify design and increase performance by eliminating the DCR sensing network and associated thermal compensation. Light-load efficiency is supported via a dedicated left control pin. An industry leading thermally enhanced, 4 mm x 5 mm PowerPAK® MLP package allows minimal overall PCB real estate and low profile construction.

The devices feature a 3.3 V (SiC575A) compatible tri-state PWM input that, working together with multiphase PWM controllers, will provide a robust solution in the event of abnormal operating conditions. The SiC575A also improves system performance and reliability with integrated fault protection of UVLO, over-temperature and over-current. An open-drain fault reporting pin simplifies the handshake between the smart VRPower device and multiphase controllers and can be used to disable the controller during start-up and fault conditions.

## FEATURES

- Highly efficient
- Thermally enhanced PowerPAK® MLP24-45L
  - Vishay latest TrenchFET technology
  - Low side MOSFET with integreated Schottky diode
  - Low impedance bootstrap switch
  - Low shutdown supply current (10 μA)
- Highly versatile
  - Wide input range support: 4.5 V to 21 V
  - Compatible with 3.3 V PWM logic tri-state / middle voltage
  - Up to 2 MHz switching frequency
- Robust and reliable
  - Delivers in excess of 40 A continuous current
  - 50 A (10 ms) and 80 A (10 μs), peak current
  - Down slope current sensing
  - Fault protection
    - Over-temperature protection
    - $V_{CC}$ (3.3 V) / $PV_{CC}$ (5 V) undervoltage lockout (UVLO)
- Effective monitoring / reporting
  - ± 3 % accuracy current monitor ($I_{MON}$)
  - 8 mV/°C temperature monitor with OT flag
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

## APPLICATIONS

- High frequency and high efficiency VRM and VRD
- Core, graphic, and memory regulators for microprocessors
- High density VR for server, networking, and cloud computing
- POL DC/DC converters and video gaming consoles

## TYPICAL APPLICATION DIAGRAM

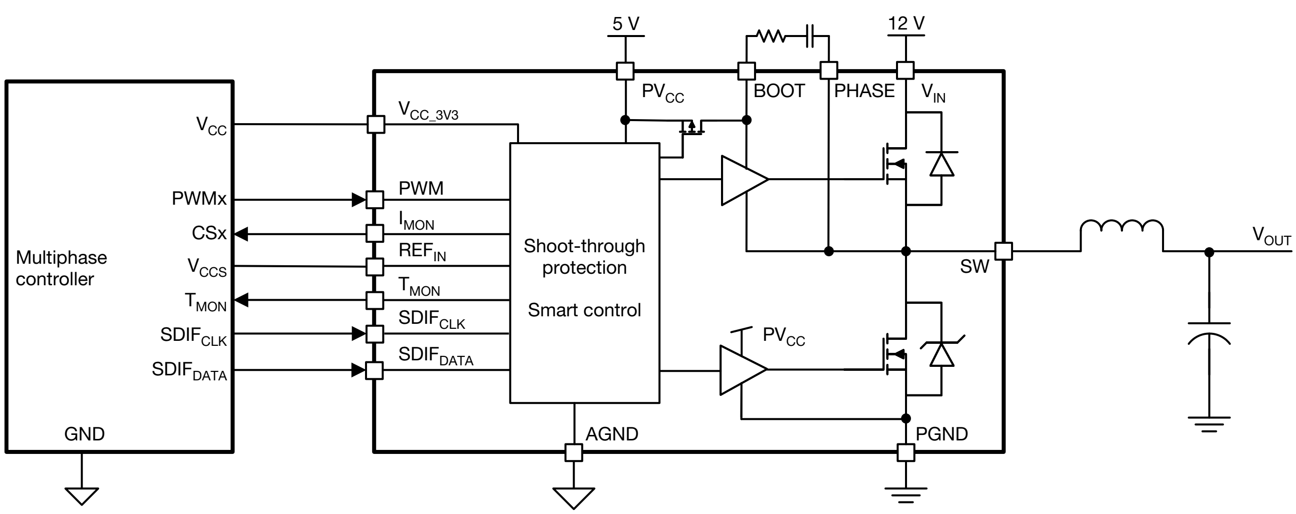



**Fig. 1 - Typical Application Block Diagram**

## FUNCTIONAL BLOCK DIAGRAM

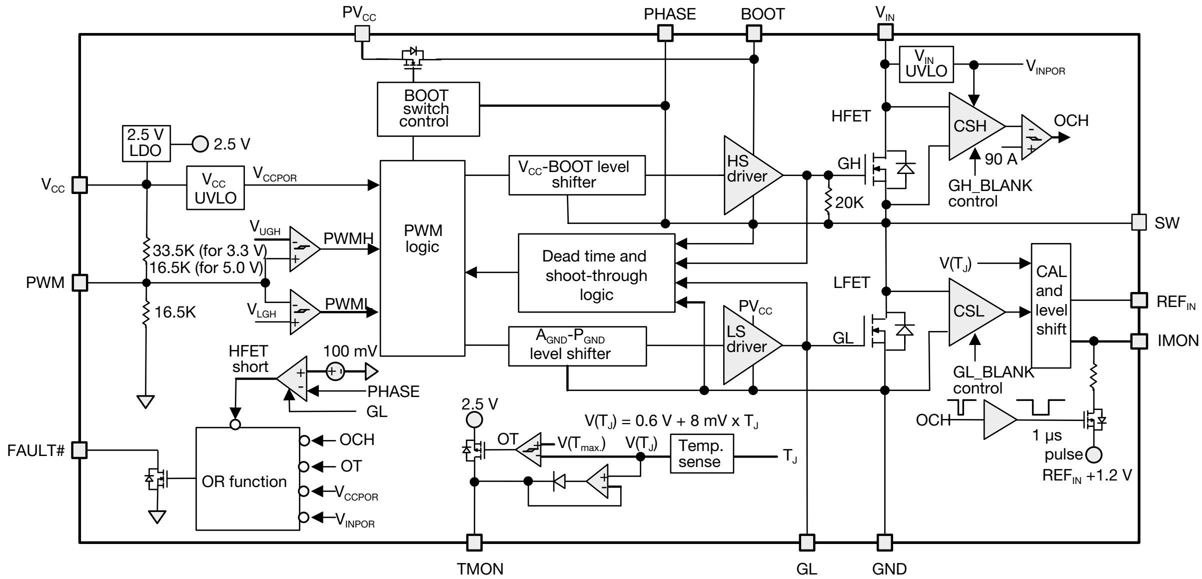



**Fig. 2 - Functional Block Diagram**

| ORDERING INFORMATION | | | | |
|---|---|---|---|---|
| **PART NUMBER** | **MARKING CODE** | **TEMPERATURE RANGE (°C)** | **PWM INPUT (V)** | **PACKAGE (RoHS-compliant)** |
| SiC575ACD-T1-GE3 | SiC575A | -40 to +125 | 3.3 | MLP24-45L |

## PINOUT CONFIGURATION

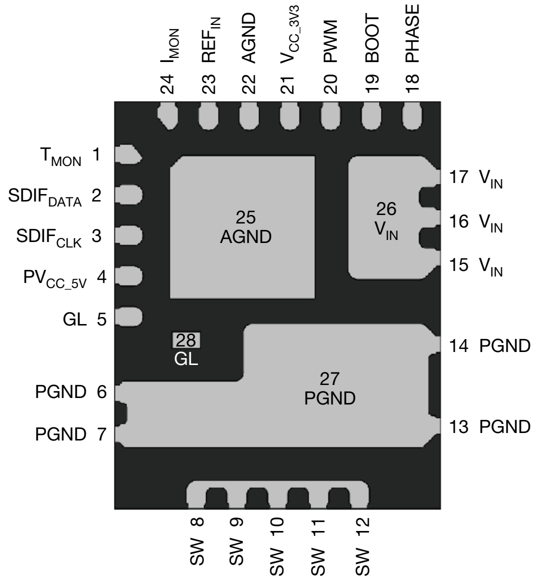



**Fig. 3 - Pinout Configuration**

| PIN CONFIGURATION | | |
|---|---|---|
| **PIN NUMBER** | **NAME** | **FUNCTION** |
| 1 | $T_{MON}$ | Temperature monitor output. For multiphase, the $T_{MON}$ pins can be connected together as a common bus; the highest voltage (representing the highest temperature) is sent to the PWM controller. $T_{MON}$ is pulled high ($V_{CC\_3V3}$) to indicate an over-temperature fault. $T_{MON}$ can be turned off or used for other functions via serial digital interface. No more than 470 pF total capacitance can be directly connected across the $T_{MON}$ and GND pins; with a series resistor, a higher capacitance load is |
| 2 | $SDIF_{DATA}$ | Serial digital interface data input and output; connect 1 kΩ to 3.3 V |
| 3 | $SDIF_{CLK}$ | Serial digital interface clock input |
| 4 | $PV_{CC\_5V}$ | +5 V logic and gate drive bias supply; place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to $A_{GND}$ |
| 5, 28 | GL | No connect (this is a low side gate driver output (GL), optional to monitor for system debugging) |
| 6, 7, 13, 14 | $P_{GND}$ | Power ground (source connection of low side MOSFET) |
| 8, 9, 10, 11, 12 | SW | Switching junction node between HFET source and LFET drain; connect directly to output inductor |
| 15, 16, 17 | $V_{IN}$ | Input of power stage (to drain of high side MOSFET); place at least two ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across $V_{IN}$ and $P_{GND}$; for optimal performance, place as many vias as possible in the bottom side $V_{IN}$ paddle |
| 18 | PHASE | Return of boot capacitor; internally connected to $SW_{node}$ so no external routing required for SW connection |
| 19 | BOOT | Floating bootstrap supply pin for the upper gate drive; place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R) in close proximity across BOOT and PHASE pins |
| 20 | PWM | PWM input of gate driver, compatible with 3.3 V tri-state PWM signal |
| 21 | $V_{CC\_3V3}$ | +3.3 V logic bias supply; place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to GND |
| 22,25 | AGND | $A_{GND}$ of driver IC |
| 23 | $REF_{IN}$ | Input for external reference voltage for $I_{MON}$ signal; this voltage should be between 0.8 V and 1.3 V; connect $REF_{IN}$ to the appropriate current sense input of the controller; place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to $A_{GND}$ |
| 24 | $I_{MON}$ | Current monitor output, referenced to $REF_{IN}$; pulls low to indicate ZCD in DCM mode; connect the $I_{MON}$ output to the appropriate current sense input of the controller; no more than 56 pF capacitance can be directly connected across the $I_{MON}$ and $REF_{IN}$ pins |

| ABSOLUTE MAXIMUM RATINGS | | | | |
|---|---|---|---|---|
| ELECTRICAL PARAMETER | SYMBOL | CONDITIONS | LIMIT | UNIT |
| Supply voltage | $V_{CC\_3V3}$ | | -0.3 to +4.3 | V |
| Supply voltage | $PV_{CC}$ | | -0.3 to +6 | |
| Input supply voltage | $V_{IN}$ | | -0.3 to +30 | |
| Phase, SW voltage | $V_{PH-GND}$, $V_{SW-GND}$ | GND - 10 V, < 20 ns pulse width, 10 μJ | -0.3 to +45 | |
| BOOT voltage | $V_{BOOT\_GND}$ | | -0.3 to +50 | |
| Other I/O pin voltage | | | -0.3 to $V_{CC}$ + 0.3 | |
| Continuous current | | | 20 | A |
| Pulse current | | 50% duty cycle | 40 | |
| Maximum instantaneous power dissipation | | | 100 | W |
| Maximum continuous power dissipation | | | 15 | |
| Maximum junction temperature | | | 150 | °C |
| Maximum storage temperature rang | | | -50 to +150 | |

**Note**

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

| RECOMMENDED OPERATING RANGE | | | | |
|---|---|---|---|---|
| ELECTRICAL PARAMETER | MINIMUM | TYPICAL | MAXIMUM | UNIT |
| Operating junction temperature range | -40 | - | 125 | °C |
| Supply voltage ($V_{CC\_3V3}$) | 3.135 | - | 3.465 | V |
| Supply voltage ($PV_{CC}$) | - | 5 ± 5 % | - | |
| Input supply voltage ($V_{IN}$) | 4.5 | - | 21 | |

| THERMAL INFORMATION | | |
|---|---|---|
| THERMAL RESISTANCE | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
| PowerPAK MLP24-45L [1][2][3] | 10.7 | 1.6 |

**Notes**

[1] $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features

[2] For $\theta_{JC}$, the case temperature location is the center of the exposed metal pad on the package underside

[3] These ratings vary with PCB layout and operating condition, and limited by device temperature and thermal shutdown trip point

| **ELECTRICAL SPECIFICATIONS** (recommended operating conditions, unless otherwise noted. $T_J$ = -40 °C to +125 °C) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **LIMITS** | | | **UNIT** |
| | | | **MIN.** [1] | **TYP.** | **MAX.** [1] | |
| **$V_{CC}$ SUPPLY CURRENT** | | | | | | |
| Logic standby current | $I_{VCC\_3V3}$ | PWM = mid-level voltage | - | 1.7 | - | mA |
| Gate drive standby current | $I_{PVCC}$ | PWM = mid-level voltage | - | 3.6 | - | μA |
| Logic operational current | $I_{VCC\_3V3}$ | PWM = 300 kHz | - | 1.7 | - | mA |
| Gate drive operation current | $I_{PVCC}$ | PWM = 300 kHz | - | 6.3 | - | mA |
| **POWER-ON RESET AND ENABLE** | | | | | | |
| $PV_{CC}$ rising POR threshold | | | 3.63 | 4.2 | 4.79 | V |
| $PV_{CC}$ falling POR threshold | | | 3.4 | 3.9 | 4.4 | V |
| $PV_{CC\_3V3}$ rising POR threshold | | | - | 2.7 | 3.1 | V |
| $PV_{CC\_3V3}$ falling POR threshold | | | 2.1 | 2.45 | - | V |
| $PV_{CC\_3V3}$ POR delay to operation | | | - | 250 | - | μs |
| **3.3 V PWM INPUT** | | | | | | |
| Mid-point lower gate falling threshold | | $V_{CC\_3V3}$ = 3.3 V, $PV_{CC}$ = 5 V | - | 1 | - | V |
| Mid-Point lower gate rising threshold | | $V_{CC\_3V3}$ = 3.3 V, $PV_{CC}$ = 5 V | - | 0.8 | - | V |
| Mid-Point upper gate rising threshold | | $V_{CC\_3V3}$ = 3.3 V, $PV_{CC}$ = 5 V | - | 2.44 | - | V |
| Mid-Point upper gate falling threshold | | $V_{CC\_3V3}$ = 3.3 V, $PV_{CC}$ = 5 V | - | 2.39 | - | V |
| Mid-point shutdown window | | $V_{CC\_3V3}$ = 3.3 V, $PV_{CC}$ = 5 V | 1.14 | - | 2.3 | V |
| **CURRENT MONITOR AND PROTECTION** | | | | | | |
| REFIN voltage range | | | 0.8 | 1.2 | 1.3 | V |
| $I_{OUT}$ closed loop current gain accuracy with renesas digital multiphase controller $V_{CC\_3V3}$ = 3.3 V, $PV_{CC}$ = 5 V | | ≥ 10 A, $T_J$ = +0 °C to +125 °C | - | ±3 | - | % |
| | | ≥ 10 A, $T_J$ = -40 °C to +0 °C | - | ±5 | - | % |
| $I_{MON}$ high at over-temperature | | | - | 3.26 | - | V |
| **TEMPERATURE MONITOR** | | | | | | |
| Over-temperature rising threshold | | | - | 150 | - | °C |
| Over-temperature falling threshold | | | - | 130 | - | °C |
| Over-temperature hysteresis | | | - | 18 | - | °C |
| Temperature coefficient | | | - | 0.008 | - | mV/K |
| $T_{MON}$ voltage at +25 °C temperature | | $V(T_J) = 0.6\ V + (8\ mV \times T_J)$ | - | 0.80 | - | V |
| **BOOTSTRAP DIODE** | | | | | | |
| Forward voltage drop | | | - | 84 | - | mV |
| On-resistance | $R_F$ | | - | 17 | - | Ω |

**Notes**

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design

(2) These ratings vary with PCB layout and operating condition, and limited by SPS temperature and thermal shutdown trip point

(3) Limits apply across the operating temperature range

## TIMING DIAGRAM

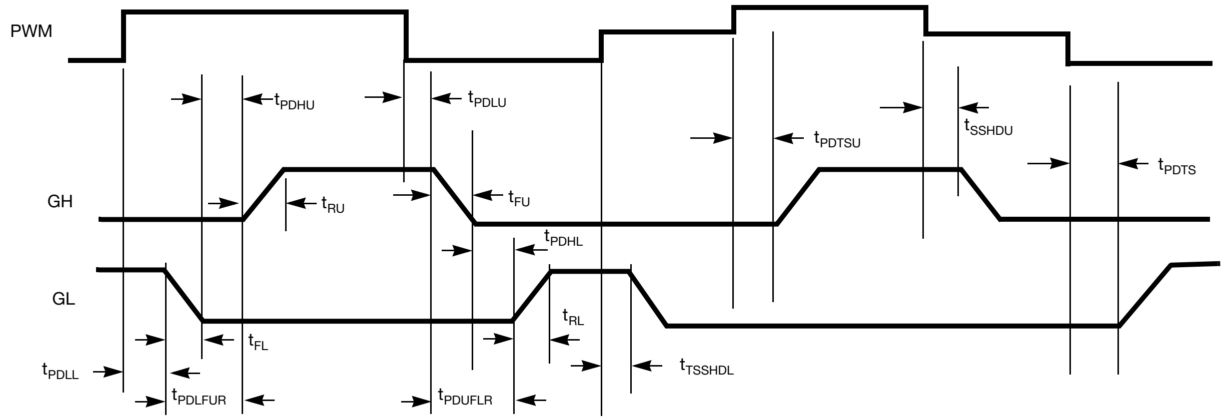



**Fig. 4 - Timing Diagram**

## TYPICAL CHARACTERISTICS ($P_{VCC}$ = 5 V, $T_A$ = 25 °C, unless otherwise stated)

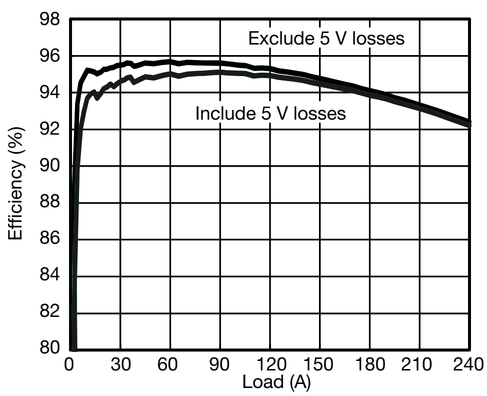



**Fig. 5 - 1.8 V $V_{OUT}$ Power Stage Efficiency ($V_{IN}$ = 12 V, $f_{SW}$ = 500 kHz; $L_{OUT}$ = 0.18 μH/0.17mΩ/FP1008-180-R; Auto-Phase Enabled in 6-Phase Operation)**

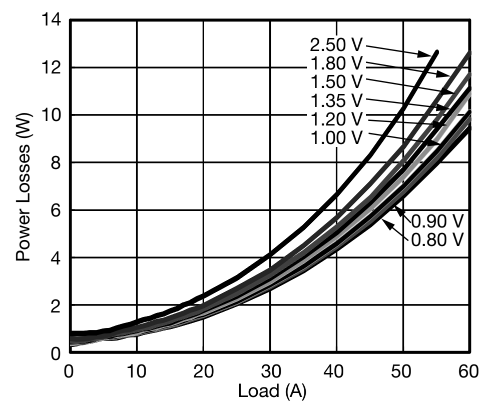



**Fig. 7 - Power Dissipation ($V_{IN}$ = 12 V, $f_{SW}$ = 500 kHz; $L_{OUT}$ = 0.18 μH/0.17mΩ/FP1008-180-R**

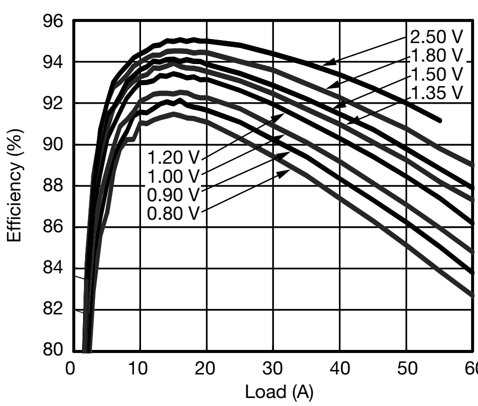



**Fig. 6 - Power Stage Efficiency ($V_{IN}$ = 12 V, $f_{SW}$ = 500 kHz; $L_{OUT}$ = 0.18 μH/0.17mΩ/FP1008-180-R**

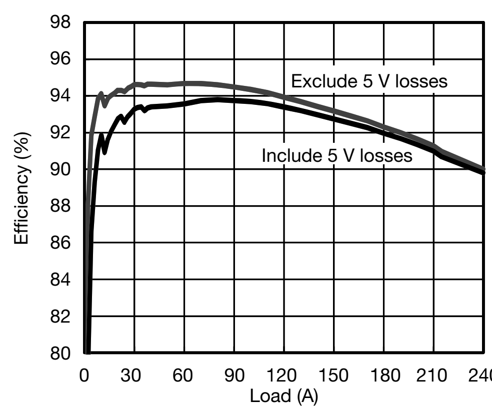



**Fig. 8 - 1.2 V Power Stage Efficiency ($V_{IN}$ = 12 V, $f_{SW}$ = 500 kHz; $L_{OUT}$ = 0.18 μH/0.17mΩ/FP1008-180-R; Auto-Phase Enabled in 6-Phase Operation)**

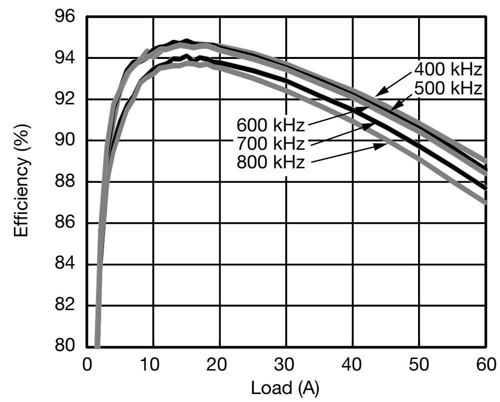



**Fig. 9 - Power Stage Efficiency ($V_{IN}$ = 12 V, $f_{SW}$ = 500 kHz; $L_{OUT}$ = 0.18 µH/0.17mΩ/FP1008-180-R**

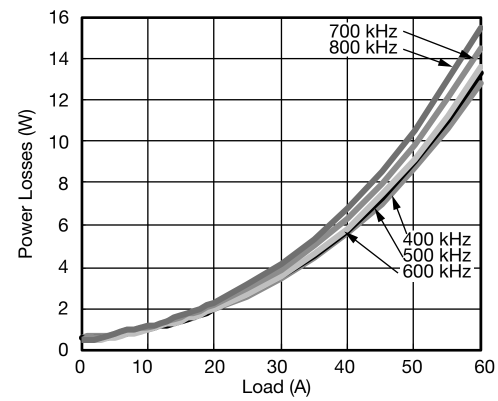



**Fig. 10 - Power Dissipation ($V_{IN}$ = 12 V, $f_{SW}$ = 500 kHz; $L_{OUT}$ = 0.18 µH/0.17mΩ/FP1008-180-R**

## DETAILED OPERATIONAL DESCRIPTION

The SiC575A is an optimized driver and power stage solution for high density synchronous DC/DC power conversion. It includes high performance GH and GL drivers, an NFET controlled to function as a bootstrap diode, and MOSFET pair optimized for high switching frequency buck voltage regulators. It also includes advanced power management features - accurate current and temperature reporting outputs.

### Power-On Reset (POR)

The $V_{CC\_3V3}$ voltage rise is monitored during initial start-up. If the rising $V_{CC\_3V3}$ voltage exceeds 2.7 V (typical), and the rising $PV_{CC5}$ voltage exceeds 4.13 V normal operation of the driver is enabled after correct initialization by the controller. The PWM signals are passed through to the gate drivers, the $T_{MON}$ output is valid and the $I_{MON}$ - $REF_{IN}$ output starts at zero, and becomes valid on the first GL signal. The driver operation is disabled if either $V_{CC\_3V3}$ or $PV_{CC5}$ drops below its falling threshold.

### Shoot-Through Protection

Prior to POR, the undervoltage protection function is activated and both GH and GL are held active low (HFET and LFET off). If the driver has no bias voltage applied (either $V_{CC\_3V3}$ or $PV_{CC}$ are missing) and is unable to actively hold the MOSFETs off, an integrated 20 kΩ resistor from the upper MOSFET gate to source helps keep the HFET device in its off state. This shoot-through protection can be especially critical in applications in which the input voltage rises before the SiC575A $V_{CC\_3V3}$ and $PV_{CC}$ supplies. After POR (the rising thresholds; see electrical specifications), and 210 µs delay, the PWM and LGCTRL signals are used to control both high side and low-side MOSFETs.

SiC575A's dead time control is optimized for high efficiency and guarantees that simultaneous conduction of both FETs cannot occur.

### Tri-State PWM Input

SiC575A supports a 3.3 V PWM tri-level input and is compatible with the multiphase controllers using 3.3 V PWM logic ($V_{CC}$ and $V_{CC\_3V3}$ of the controller should share the same rail). If the pin is pulled into the tri-state window and remains there for a set hold-off time, the driver forces both MOSFETs to their off states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands.

This feature is used by the PWM controllers as a method of forcing both MOSFETs off. Proper functionality of the driver and power stage is not guaranteed if used without an appropriate controller approved by Vishay.

### Bootstrap Function

The SiC575A features an internal NFET that is controlled to function as a bootstrap diode. A high quality ceramic capacitor should be placed in close proximity across the BOOT and PHASE pins. The bootstrap capacitor can range between 0.1 µF to 0.22 µF (0402 to 0603 and X5R to X7R) for normal buck switching applications. A boot resistor can be used in series with the capacitor as MOSFET performance and operating conditions dictate.

### Serial Digital Interface (SDIF) Bus

The SDIF is a two-wire bus consisting of a clock and data line, designed for communication between the digital multiphase controller and compatible smart power stages. SDIF_CLK operates unidirectionally, from controller to power stage, in a push-pull configuration that is held low when not in use. SDIF_DAT is a bidirectional line configured as an open drain pin connected to $V_{CC\_3V3}$ through a single 1 kΩ pull-up resistor placed near the controller. Typically, the bus operates at 1 MHz with frequencies up to 2 MHz allowed.

During operation, SDIF primarily optimizes the system level power consumption by commanding power stages into one of several power states based on CPU activity. The bus also gives permission for a power stage to report its temperature on the $T_{MON}$ pin back to the controller. This allows for individual power stage temperatures to be monitored rather than only the maximum temperature as is commonly implemented in other designs. Additionally, the controller reads calibration data from the power stage at startup to optimize the inductor current information reported on the $I_{MON}$ pin.

### Current Monitoring

LFET current is monitored and a signal proportional to that current is output on the $I_{MON}$ pin (relative to the $REF_{IN}$ pin) without thermal and $V_{CC\_3V3}$ compensations, which are done inside the controller after SDIF bus polls the information from SPS. The $I_{MON}$ and $REF_{IN}$ pins should be connected to the appropriate current sense input pin of the controller. This method does not require external $R_{SENSE}$ or DCR sensing of inductor current.

Fig. 13 depicts the low side current sense concept. After the falling edge of PWM, there are two delays; one that represents the expected propagation delay from PWM to GH/SW, and a second blanking delay to allow time for the transition to settle; typical total time is ~ 350 ns. The $I_{MON}$ output approximates the actual $I_L$ waveform.

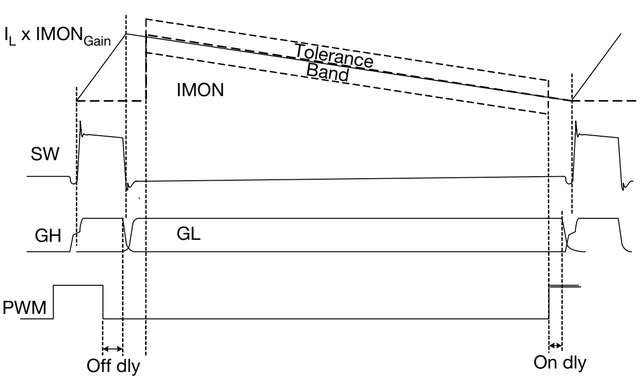



**Fig. 11 - LFET Current Sample Diagram**

The HFET current is not monitored in the same way, so no valid measured current is available while PWM is high (and the short delays before and after). During this time, the $I_{MON}$ will output the last valid LFET current before the sampling stopped. On start-up after POR, the $I_{MON}$ will output zero (relative to $REF_{IN}$, which represents zero current) until the switching begins, and then the current can be properly measured.

### Thermal Monitoring

The SiC575A monitors its internal temperature and provides a signal proportional to that temperature on the $T_{MON}$ pin. $T_{MON}$ has a voltage of 600 mV at 0 °C and reflects temperature at 8 mV/°C. The $T_{MON}$ output is valid after the proper command from the controller over the SDIF bus.

In a multiphase application each $T_{MON}$ pin is tied together and a single signal is routed back to the controller. However, each SiC575A only reports its temperature after the appropriate command is sent over the SDIF bus. This allows for individual phase temperature readings instead of simply the maximum temperature at any given time.

If an over-temperature fault occurs, the $I_{MON}$ pin is pulled high to 3.3 V.

### Thermal Protection

If the internal temperature exceeds the over-temperature trip point (+140 °C typical), the $T_{MON}$ pin is pulled to 3.3 V and no other action is taken on-chip. The $T_{MON}$ will remain in the fault mode, until the junction temperature drops below +130 °C typical; at that point, the $T_{MON}$ resumes normal operation.

### FAULT Reporting

Over-temperature detection will pull the $T_{MON}$ pin to a high (fault) level, such that the PWM controller should quickly recognize it as out of the normal range.

The fault reporting and respective SPS response are summarized in Table 1.

**TABLE 1 - FAULT REPORTING SUMMARY**

| FAULT EVENT | $T_{MON}$ | RESPONSE |
|---|---|---|
| OT | HIGH | Wait for input from controller |
| $PV_{CC}$ UVLO | $I_{MON}$ - $REF_{IN}$ = 0 V | Switching stops while in UVLO; when above $PV_{CC5}$ POR, after 210 µs: GH and GL follow PWM, $T_{MON}$ is valid, and $I_{MON}$ - $REF_{IN}$ is valid after GL first goes low |
| $V_{CC\_3V3}$ UVLO | $I_{MON}$ - $REF_{IN}$ = 0 V | Switching stops while in UVLO; driver requires reinitialization from controller to resume normal operation |

## PCB LAYOUT CONSIDERATIONS

Proper PCB layout will reduce noise coupling to other circuits, improve thermal performance, and maximize the efficiency. The following is meant to lead to an optimized layout:

- Place multiple 10 μF or greater ceramic capacitors directly at device between $V_{IN}$ and $P_{GND}$. This is the most critical decoupling and reduced parasitic inductance in the power switching loop. This will reduce overall electrical stress on the device as well as reduce coupling to other circuits. Best practice is to place the decoupling capacitors on the same PCB side as the device. For a design with tight space requirements, these decoupling capacitors can be placed under the device, i.e., bottom layer.
- Connect GND to the system GND plane with a large via array as close to the GND pins as design rules allow. This improves thermal and electrical performance.
- Place $PV_{CC}$, $V_{CC}$ and BOOT-PHASE decoupling capacitors at the IC pins.
- Note that the SW plane connecting the SiC575A and inductor must carry full load current and will create resistive loss if not sized properly. However, it is also a very noisy node that should not be oversized or routed close to any sensitive signals. Best practice is to place the inductor as close to the device as possible and thus minimizing the required area for the SW connection. If one must choose a long route of either the $V_{OUT}$ side of the inductor or the SW side, choose the quiet $V_{OUT}$ side. Best practice is to locate the SiC575A as close to the final load as possible and thus avoid noisy or lossy routes to the load.
- The $I_{MON}$ and IREF network and their vias should not sit on the top of the $V_{IN}$ plane, a keep out area is recommended.
- The PCB is the best thermal heatsink material than any top side cooling materials. The PCB always has enough vias to connect $V_{IN}$ and GND planes. Insufficient vias will yield lower efficiency and very poor thermal performance.

| PRODUCT SUMMARY | |
|---|---|
| Part number | SiC575A |
| Description | 40 A smart power stage, 4.5 $V_{IN}$ to 21 $V_{IN}$, 3.3 V PWM with diode emulation mode |
| Input voltage min. (V) | 4.5 |
| Input voltage max. (V) | 21 |
| Current rating (A) | 40 |
| Switch frequency max. (kHz) | 2000 |
| Enable (yes / no) | No |
| Monitoring features | $I_{MON}$, $T_{MON}$ |
| Protection | UVLO, OCP, OTP |
| Light load mode | Diode emulation |
| Pulse-width modulation (V) | 3.3 |
| Package type | PowerPAK MLP24-45L |
| Package size (W, L, H) (mm) | 4.0 x 5.0 x 0.75 |
| Status code | 1 |
| Product type | VRPower (DrMOS) |
| Applications | Computer, industrial, networking |

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