SQS110ENW

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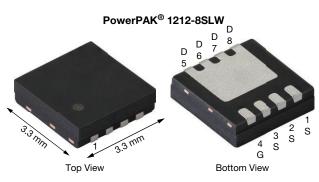
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RoHS

COMPLIANT HALOGEN

FREE

Automotive N-Channel 100 V (D-S) 175 °C MOSFET

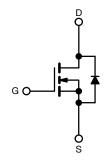


Marking code: Q069

PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0132			
I _D (A) ^e	57			
Configuration	Single			

FEATURES

- TrenchFET[®] Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Wettable flank terminals
- Low thermal resistance with 0.75 mm profile
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



N-Channel MOSFET

ORDERING INFORMATION				
Package	PowerPAK® 1212-8SLW			
Lead (Pb)-free and halogen-free	SQS110ENW (for detailed order number please see <u>www.vishay.com/doc?79771</u>)			

ABSOLUTE MAXIMUM RATINGS (T	_C = 25 °C, unless	otherwise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100	V	
Gate-source voltage		V _{GS}	± 20	v	
Continuous drain surrant f	T _C = 25 °C		57		
Continuous drain current ^e	T _C = 125 °C	ID	33		
Continuous source current (diode conduction) e		I _S	108	А	
Pulsed drain current ^{a, e}		I _{DM}	119		
Single pulse avalanche current		I _{AS}	27		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	36	mJ	
Mauinum annua diasis stiss 8 6	T _C = 25 °C	P _D	119	14/	
Maximum power dissipation ^{a, e}	T _C = 125 °C		39	W	
Operating junction and storage temperature range	e	T _J , T _{stg}	-55 to +175	J°	
Soldering recommendations (peak temperature) c		260	-0		
THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount ^b	R _{thJA}	54	°C/W	
Junction-to-case (drain) ^d		R _{thJC}	1.26	°C/W	

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%$

b. When mounted on 1" square PCB (FR4 material)

c. See solder profile (www.vishay.com/doc?73257). A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

d. As per on JESD51-14

e. Values based on RthJC and TC of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

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PARAMETER	SYMBOL	TES	ST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0, I_D = 250 \ \mu A$		100	-	-	v
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	V _{DS} = V _{GS} , I _D = 250 μA		2.7	4.0	v
Gate-source leakage	I _{GSS}	V _{DS} =	= 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 100 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	$V_{DS} = 100 \text{ V}, \text{ T}_{\text{J}} = 125 ^{\circ}\text{C}$	-	-	50	μA
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	15	-	-	Α
		V _{GS} = 10 V	I _D = 10 A	-	0.0115	0.0132	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.0275	Ω
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0360	
Forward transconductance b	9 _{fs}	V _{DS}	= 15 V, I _D = 18 A	-	65	-	S
Dynamic ^b					•		<u>.</u>
Input capacitance	C _{iss}		V V _{DS} = 25 V, f = 1 MHz	-	2463	3449	pF
Output capacitance	C _{oss}	$V_{GS} = 0 V$		-	239	335	
Reverse transfer capacitance	C _{rss}			-	18	26	
Total gate charge ^c	Qg			-	34	51	
Gate-source charge ^c	Q _{gs}	$V_{GS} = 10 V$ $V_{DS} = 50 V$, $I_{D} = 5 A$	-	11	-	nC	
Gate-drain charge ^c	Q _{gd}			-	6	-	
Gate resistance	Rg	f = 1 MHz		0.4	0.9	1.8	Ω
Turn-on delay time ^c	t _{d(on)}			-	13	20	
Rise time ^c	t _r	$\label{eq:VDD} \begin{array}{l} V_{\text{DD}} = 50 \; \text{V}, \; R_{\text{L}} = 10 \; \Omega \\ I_{\text{D}} \cong 5 \; \text{A}, \; V_{\text{GEN}} = 10 \; \text{V}, \; R_{\text{g}} = 1 \; \Omega \end{array}$		-	3	6	
Turn-off delay time ^c	t _{d(off)}			-	24	36	ns
Fall time ^c	t _f			-	5	9	
Source-Drain Diode Ratings and Charac	teristic ^b	•			•		
Pulsed current ^a	I _{SM}			-	-	350	А
Forward voltage	V _{SD}	I _F = 10 A, V _{GS} = 0 V		-	0.82	1.1	V
Body diode reverse recovery time	t _{rr}	V_{DD} = 80 V, I _F = 5 A, di/dt = 100 A/µs, R = 10 Ω, L = 0.3 mH, pulse width = 2 µs		-	35	70	ns
Body diode reverse recovery charge	Q _{rr}			-	52	104	nC
Reverse recovery fall time	ta			-	30	-	
Reverse recovery rise time	t _b			-	6	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			-	-2.6	-	А

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

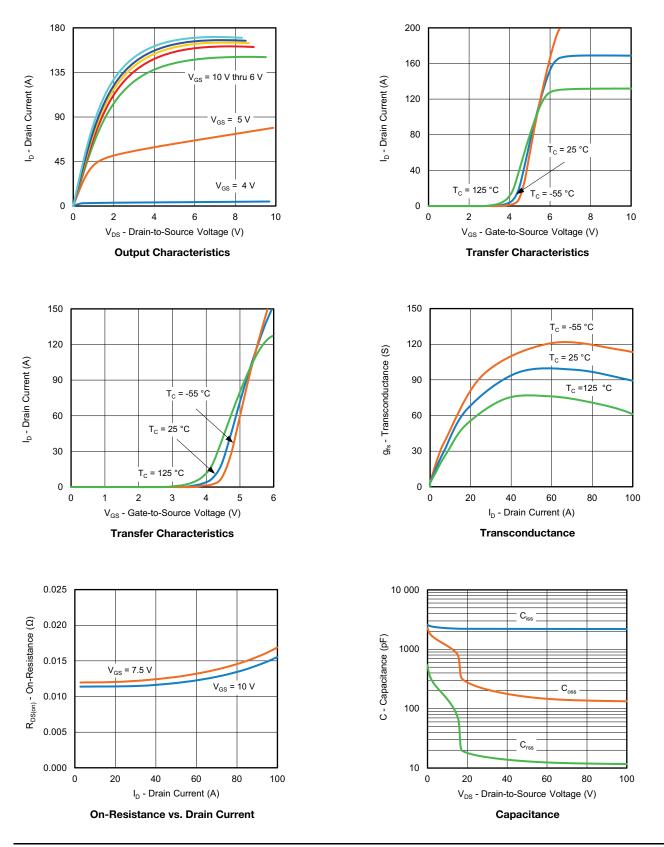
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



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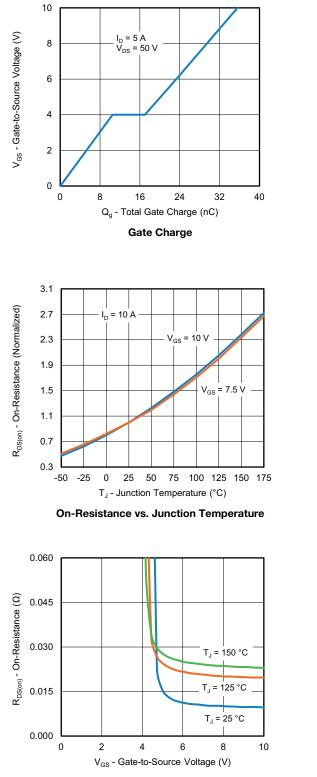
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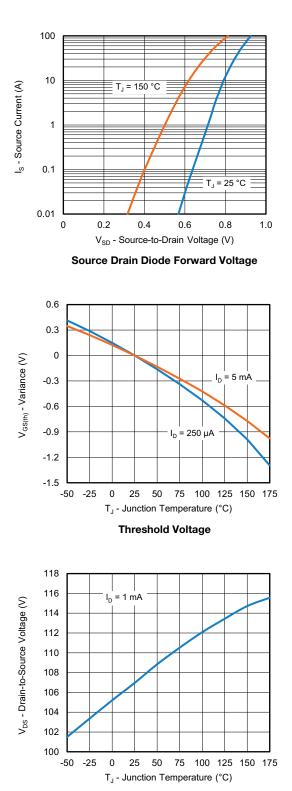
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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



On-Resistance vs. Gate-to-Source Voltage



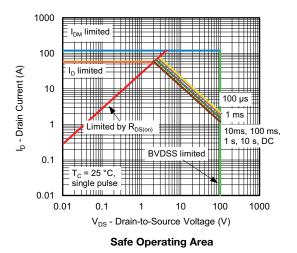
Drain Source Breakdown vs. Junction Temperature

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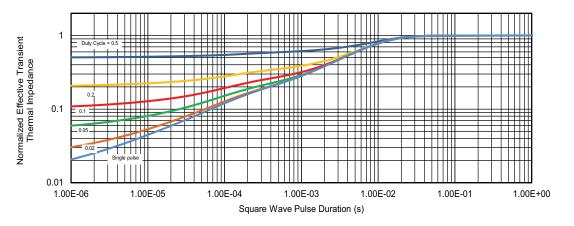
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

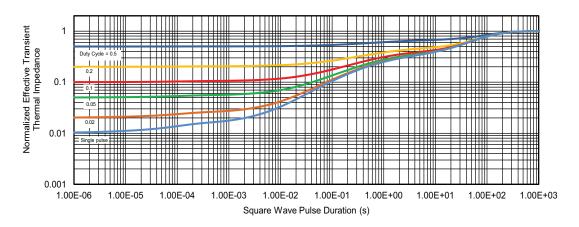


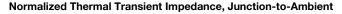
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case





Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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Revision: 01-Jan-2025

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