



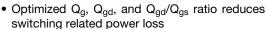
# Dual N-Channel 60 V (D-S) MOSFET



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.029			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.038			
Q <sub>g</sub> typ. (nC)	3.3			
I <sub>D</sub> (A) <sup>a</sup>	8			
Configuration	Dual			

#### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device



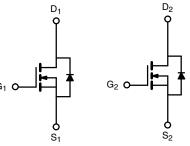
• 100 % R<sub>q</sub> and UIS tested

· Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



### **APPLICATIONS**

- Synchronous rectification
- · Load switch
- Motor drive control
- Battery management



N-Channel MOSFET N-Channel MOSFET

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	Si9634DY-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	60	V
Gate-source voltage		V <sub>GS</sub>	± 20	V
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C		8 a	
	T <sub>C</sub> = 70 °C	1 ,	6.6	
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	6.2 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		5 b, c	•
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	32	A
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		3	
	T <sub>A</sub> = 25 °C	l <sub>S</sub>	1.7 <sup>b, c</sup>	
Single pulse avalanche current	I 0.1 ml I	I <sub>AS</sub>	10	
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	5	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C		3.6	
	T <sub>C</sub> = 70 °C		2.3	14/
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2 b, c	W
	T <sub>A</sub> =70 °C		1.3 <sup>b, c</sup>	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering recommendations (peak temperature) c			260	

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient b, e	≤ 10 s	R <sub>thJA</sub>	50	62.5	°C/W		
Maximum junction-to-foot (drain)	Steady state	$R_{thJF}$	28	35	7 °C/W		

a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. Maximum under steady state conditions is 110 °C/W



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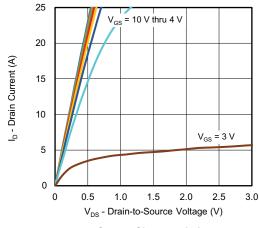
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA	-	33	-	m>\//°C	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA			-	mV/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	-	3	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20$	-	=	100	nA	
Zero gate voltage drain current		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	-	-	1	1	
	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	μA	
Drain-source on-state resistance <sup>a</sup>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	-	0.022	0.029	Ω	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4 A	-	0.029	0.038		
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A	-	23	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	420	-	pF	
Output capacitance	C <sub>oss</sub>		-	92	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	4	-		
Table also de con		$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	-	7.1	11	nC	
Total gate charge	Qg	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	3.3	5		
Gate-source charge	Q <sub>gs</sub>		-	1.7	-		
Gate-drain charge	Q <sub>gd</sub>		-	0.9	-		
Gate resistance	$R_g$	f = 1 MHz	0.3	1.6	3.2	Ω	
Turn-on delay time	t <sub>d(on)</sub>	$\begin{aligned} V_{DD} &= 30 \text{ V}, \text{ R}_L = 6 \Omega, \text{ I}_D \cong 5 \text{ A}, \\ V_{GEN} &= 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	-	10	20		
Rise time	t <sub>r</sub>		-	5	10		
Turn-off delay time	t <sub>d(off)</sub>		-	15	30		
Fall time	t <sub>f</sub>		-	5	10	1	
Turn-on delay time	t <sub>d(on)</sub>		-	12	25	ns	
Rise time	t <sub>r</sub>	$\begin{split} V_{DD} = 30 \text{ V, } R_L = 6  \Omega \text{, } I_D &\cong 5 \text{ A,} \\ V_{GEN} = 4.5 \text{ V, } R_g = 1  \Omega \end{split}$	-	16	35		
Turn-off delay time	t <sub>d(off)</sub>		-	11	25		
Fall time	t <sub>f</sub>		-	5	10		
<b>Drain-Source Body Diode Characteristi</b>	cs						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C -	-	8			
Pulse diode forward current	I <sub>SM</sub>		-	-	32	A	
Body diode voltage	$V_{SD}$	I <sub>S</sub> = 2 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	14	30	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>		-	10	20	nC	
Reverse recovery fall time	t <sub>a</sub>	$I_F = 5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	8	-		
Reverse recovery rise time	t <sub>b</sub>		-	6	-	ns	

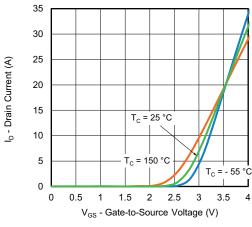
#### **Notes**

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

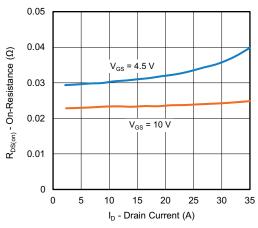


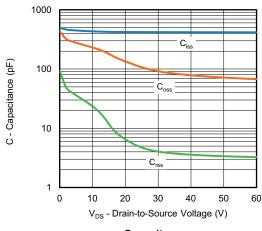






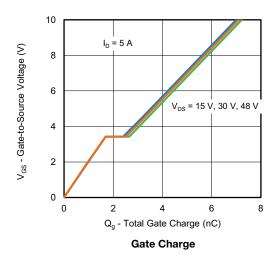


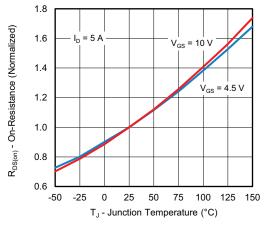




On-Resistance vs. Drain Current and Gate Voltage

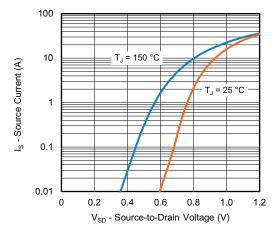
Capacitance



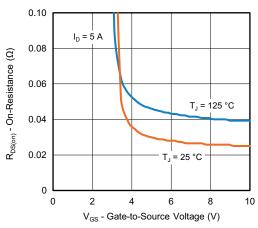


On-Resistance vs. Junction Temperature

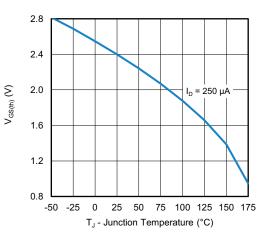




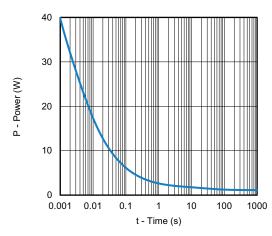
Source-Drain Diode Forward Voltage



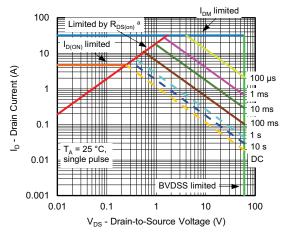
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



Single Pulse Power, Junction-to-Ambient

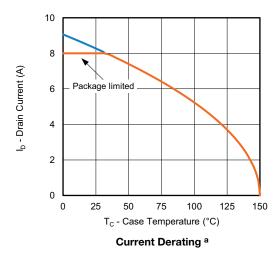


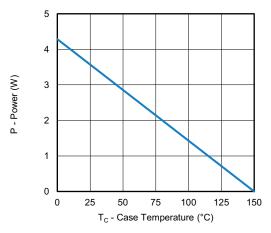
Safe Operating Area, Junction-to-Ambient

#### Note

a.  $V_{GS} > minimum V_{GS}$  at which  $R_{DS(on)}$  is specified





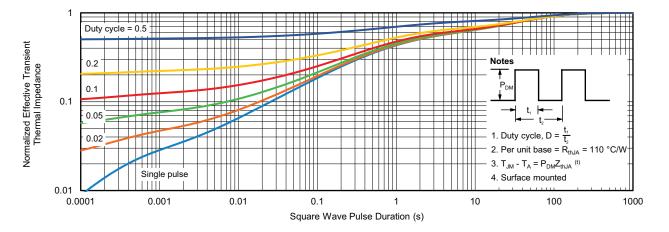


Power, Junction-to-Case

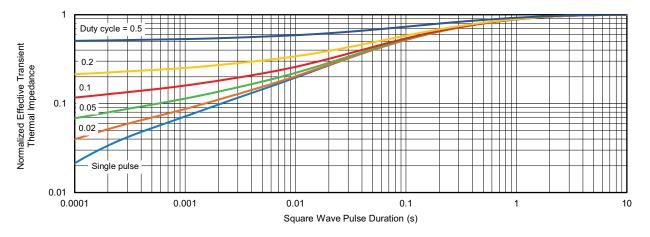
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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