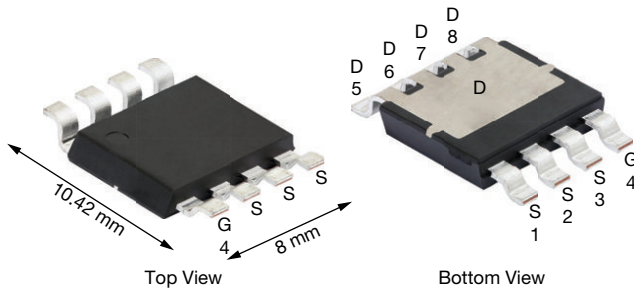
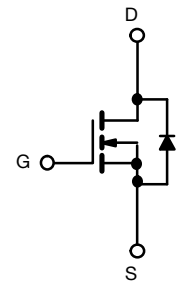


Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8LR

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.00124
I_D (A) ^e	345
Configuration	Single
Package	PowerPAK 8 x 8LR

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ^e	I_D	$T_C = 25$ °C	345
		$T_C = 125$ °C	199
Continuous source current (diode conduction) ^e	I_S	252	A
Pulsed drain current ^a	I_{DM}	791	
Single pulse avalanche current	I_{AS}	48	
Single pulse avalanche energy	E_{AS}	115.2	mJ
Maximum power dissipation ^{a, e}	P_D	$T_C = 25$ °C	277
		$T_C = 125$ °C	92
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	44	°C/W
Junction-to-case (drain) ^d	R_{thJC}	0.54	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per JESD51-14
- Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system



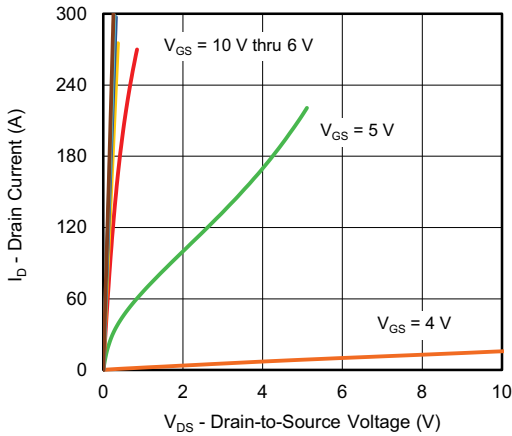
SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	3	3.5	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	200	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	330	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	100	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	-	0.00100	0.00124	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.00200	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.00240	
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 60\text{ A}$		-	150	-	S
Dynamic ^b							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	5360	6975	pF
Output capacitance	C_{oss}			-	2070	2700	
Reverse transfer capacitance	C_{rss}			-	167	215	
Total gate charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 20\text{ A}$	-	92	130	nC
Gate-source charge ^c	Q_{gs}			-	26	-	
Gate-drain charge ^c	Q_{gd}			-	20.1	-	
Gate resistance	R_g	$f = 1\text{ MHz}$		0.65	1.59	2.56	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	18.5	26	ns
Rise time ^c	t_r			-	18	25	
Turn-off delay time ^c	$t_{d(off)}$			-	37	52	
Fall time ^c	t_f			-	14	20	
Source-Drain Diode Ratings and Characteristics ^b							
Reverse recovery time	t_{rr}	$V_{DD} = 32\text{ V}, I_{FM} = 15\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}$		-	59	-	ns
Reverse recovery charge	Q_{rr}			-	69	-	nC
Reverse recovery current	I_{RM}			-	2	3.2	A
Pulsed current ^a	I_{SM}			-	-	791	A
Forward voltage	V_{SD}	$I_F = 50\text{ A}, V_{GS} = 0$		-	0.8	1.1	V

Notes

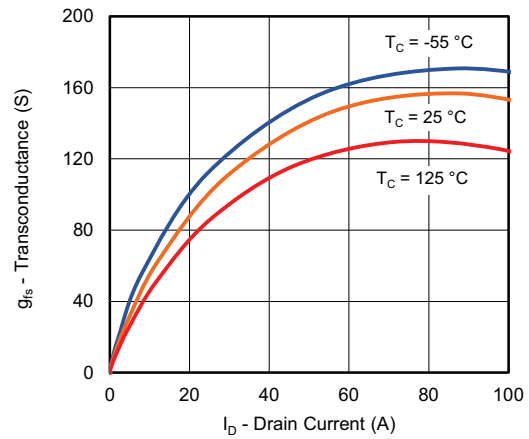
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\text{ }\%$
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

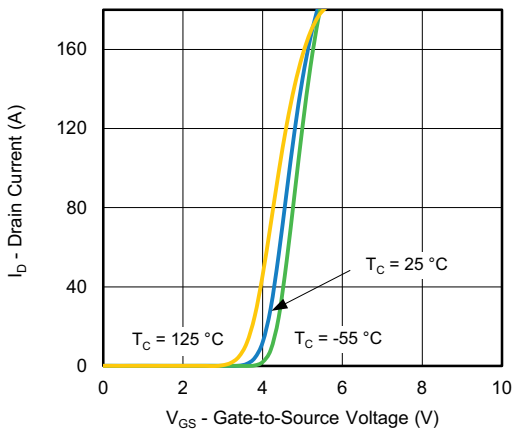
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



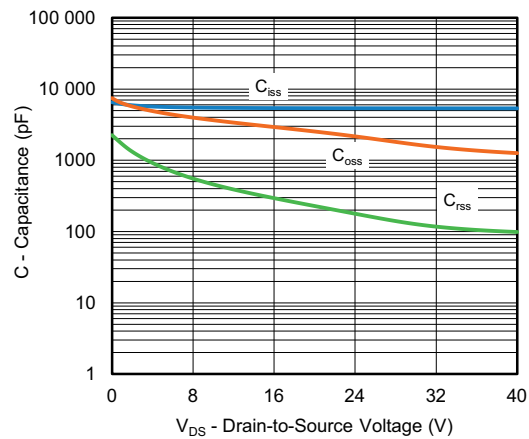
Output Characteristics



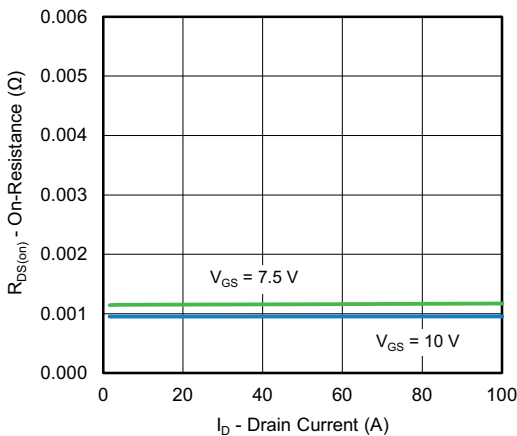
Transconductance



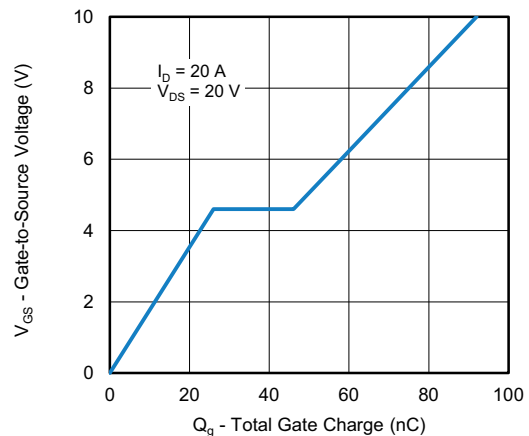
Transfer Characteristics



Capacitance



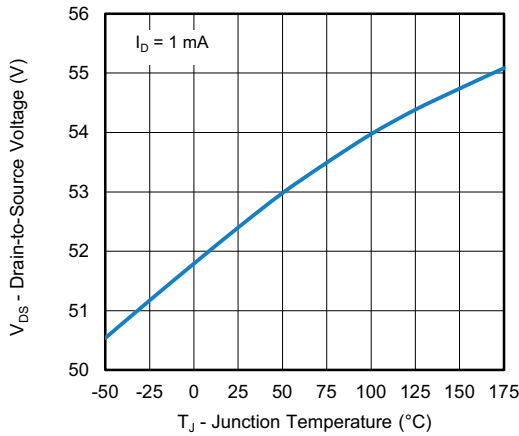
On-Resistance vs. Drain Current



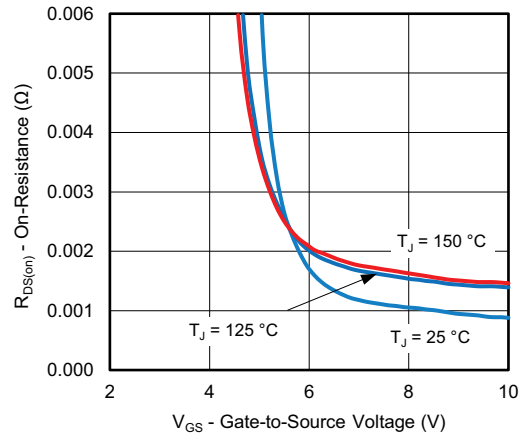
Gate Charge



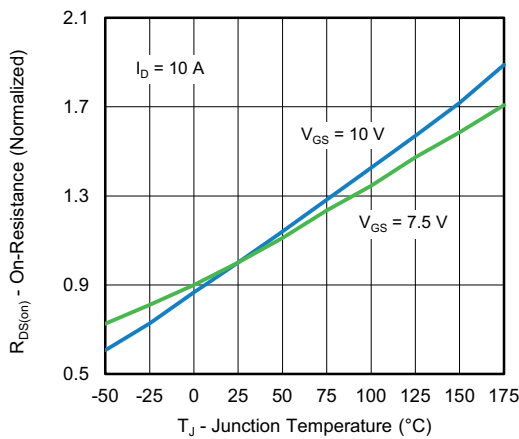
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



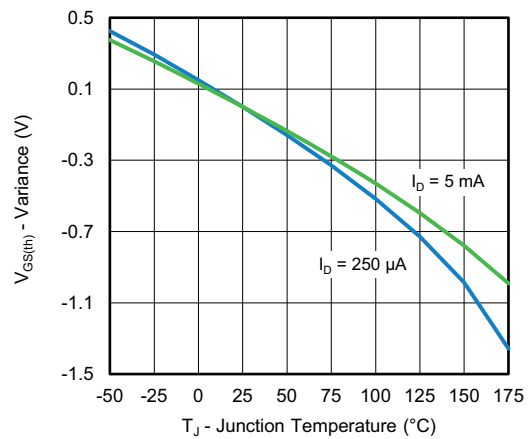
Drain Source Breakdown vs. Junction Temperature



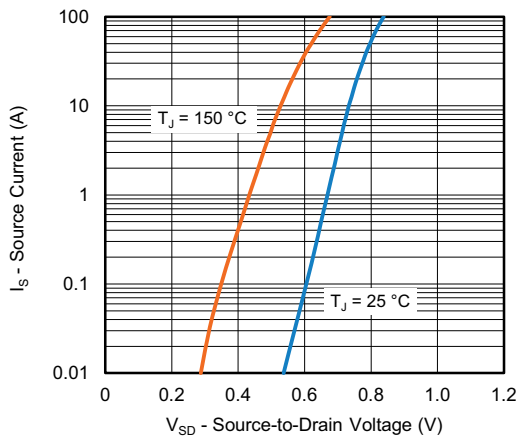
On-Resistance vs. Gate-to-Source Voltage



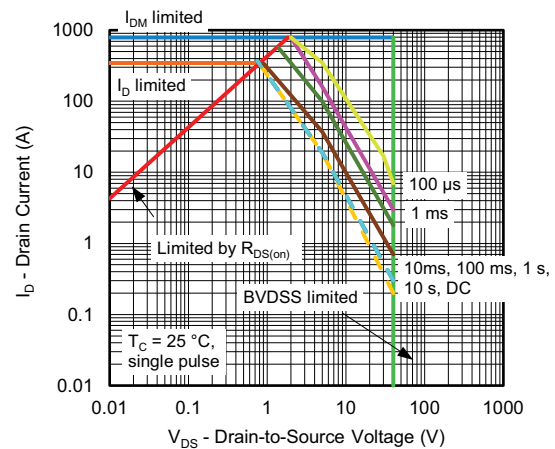
On-Resistance vs. Junction Temperature



Threshold Voltage



Source Drain Diode Forward Voltage



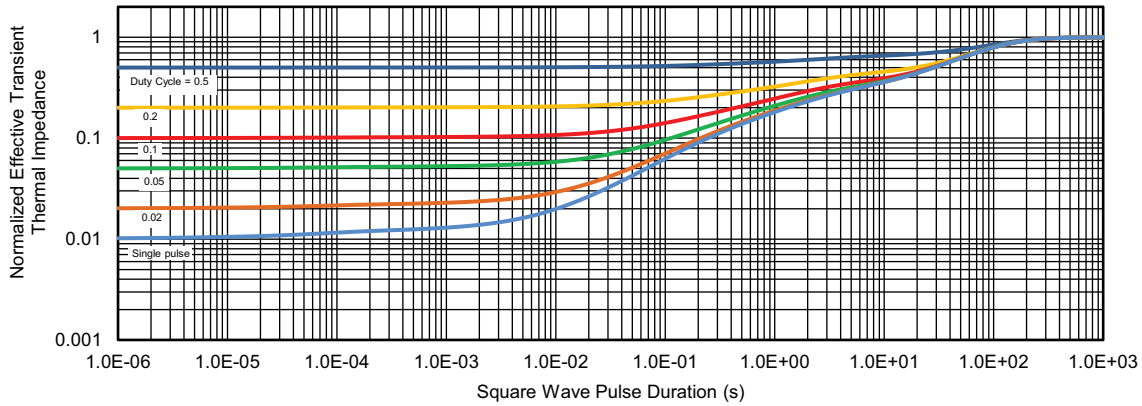
Safe Operating Area

Note

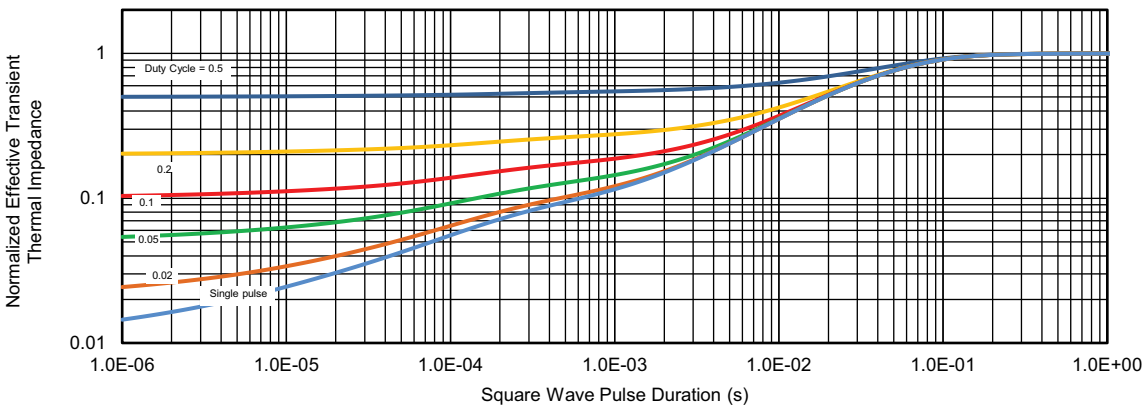
- a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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