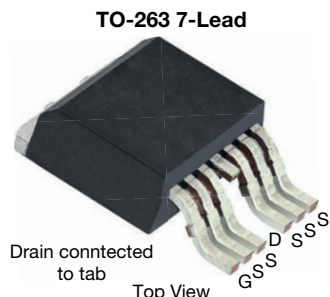


# N-Channel 100 V (D-S) MOSFET



## FEATURES

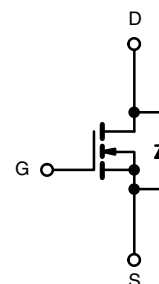
- TrenchFET® Gen IV power MOSFET
- Maximum 175 °C junction temperature
- 100 %  $R_g$  and UIS tested
- Very low  $Q_{gd}$  reduces power loss from passing trough  $V_{plateau}$
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- Power supply  
- Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing / e-fuse



N-Channel MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00383
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0045
$Q_g$ typ. (nC)	84
$I_D$ (A) <sup>d</sup>	150
Configuration	Single

## ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263-7L)
Lead (Pb)-free and halogen-free	SUM70042M-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	100	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	150 <sup>d</sup>
		$T_C = 70$ °C	150 <sup>d</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	500	A
Avalanche current	$I_{AS}$	60	A
Single avalanche energy <sup>a</sup>	$E_{AS}$	180	mJ
Maximum power dissipation <sup>a</sup>	$P_D$	$T_C = 25$ °C	375 <sup>b</sup>
		$T_C = 125$ °C	125 <sup>b</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient (PCB mount) <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-case (drain)	$R_{thJC}$	0.4	°C/W

### Notes

- Duty cycle  $\leq 1$  %
- See SOA curve for voltage derating
- When mounted on 1" square PCB (FR4 material)
- Package limited



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA	100	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	3.8	
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	150	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	5	mA
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.00316	0.00383	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 15 A	-	0.00341	0.0045	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	-	68	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V, f = 1 MHz	-	6750	-	pF
Output capacitance	C <sub>oss</sub>		-	620	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	18	-	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	84	126	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>		-	35	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	9	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.7	1.5	2.6	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	21	42	ns
Rise time <sup>c</sup>	t <sub>r</sub>		-	10	20	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	41	82	
Fall time <sup>c</sup>	t <sub>f</sub>		-	11	22	
Drain-Source Body Diode Ratings and Characteristics <sup>b</sup> (T <sub>C</sub> = 25 °C)						
Pulsed current (t = 100 μs)	I <sub>SM</sub>		-	-	500	A
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.74	1.2	V
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs	-	61	120	ns
Peak reverse recovery charge	I <sub>RM(REC)</sub>		-	4.8	9.5	A
Reverse recovery charge	Q <sub>rr</sub>		-	0.150	0.30	μC

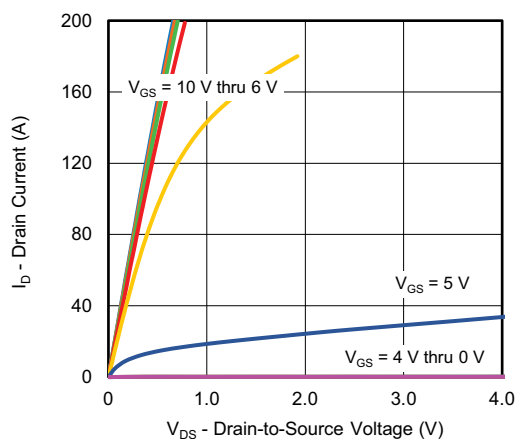
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

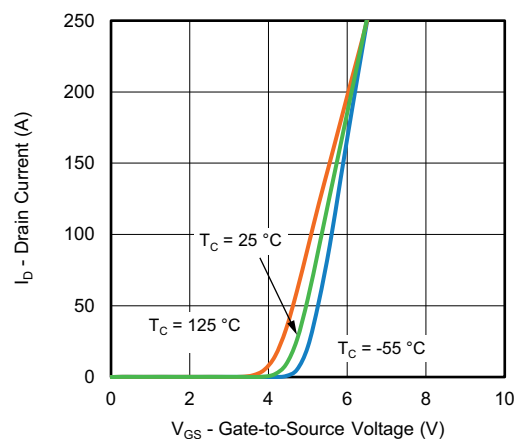
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



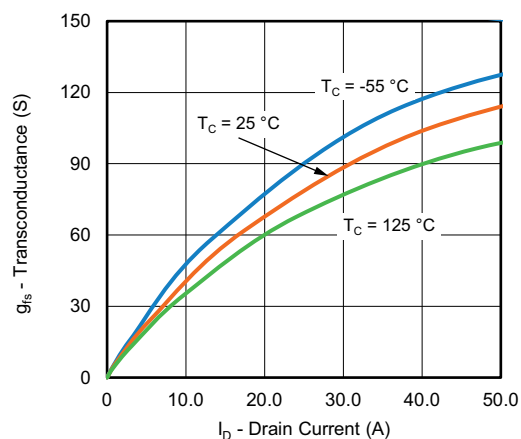
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



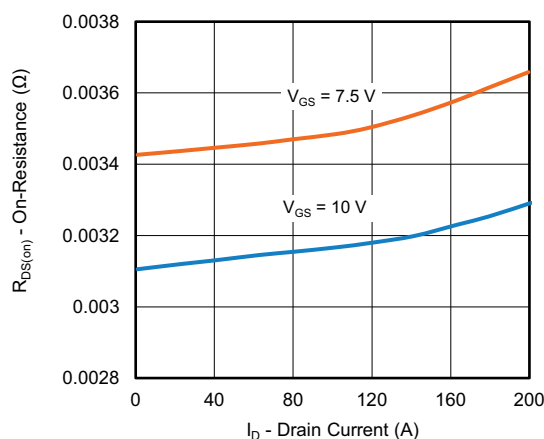
**Output Characteristics**



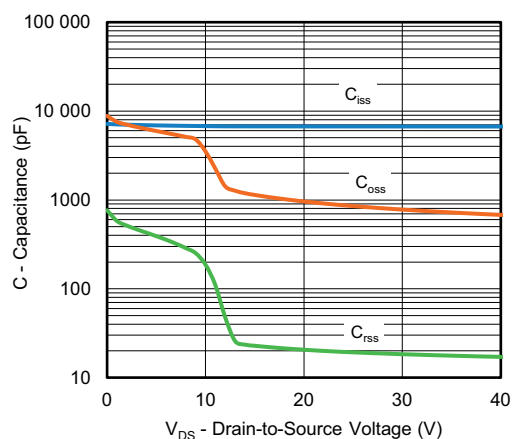
**Transfer Characteristics**



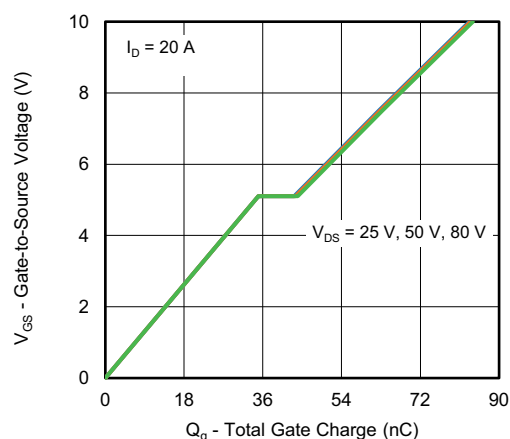
**Transconductance**



**On-Resistance vs. Drain Current**



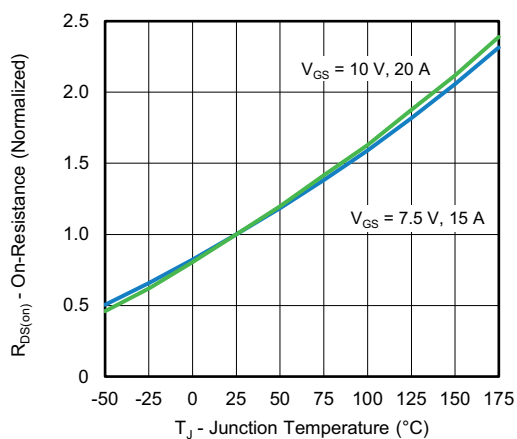
**Capacitance**



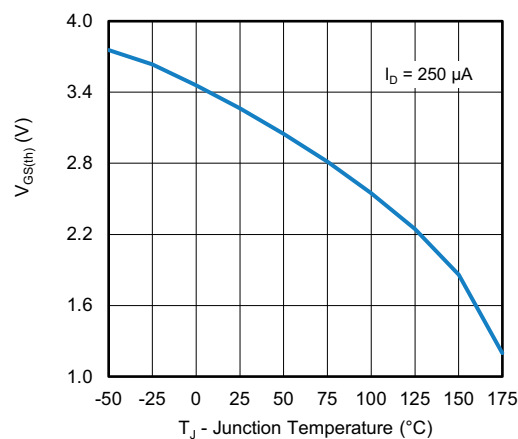
**Gate Charge**



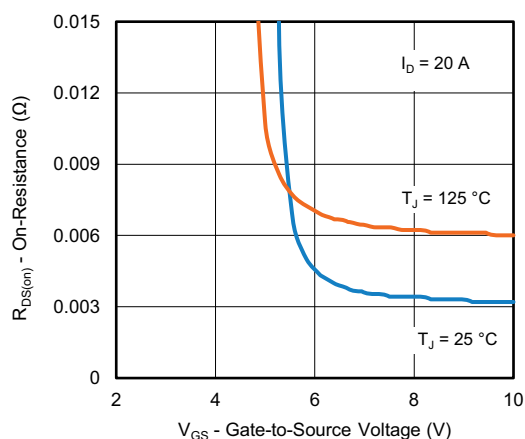
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



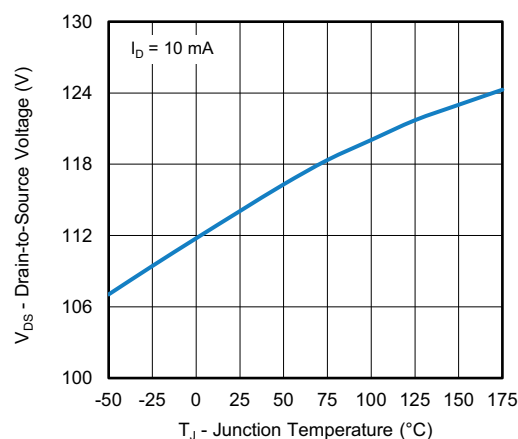
**On-Resistance vs. Junction Temperature**



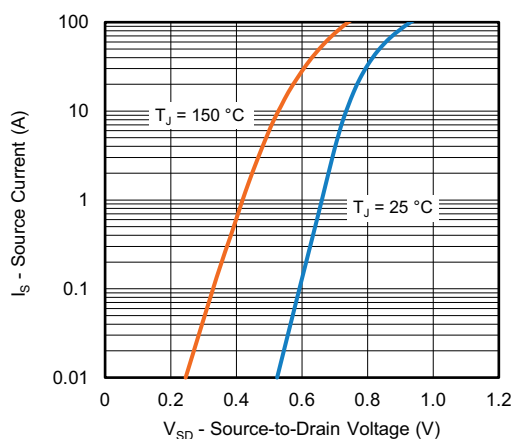
**Threshold Voltage**



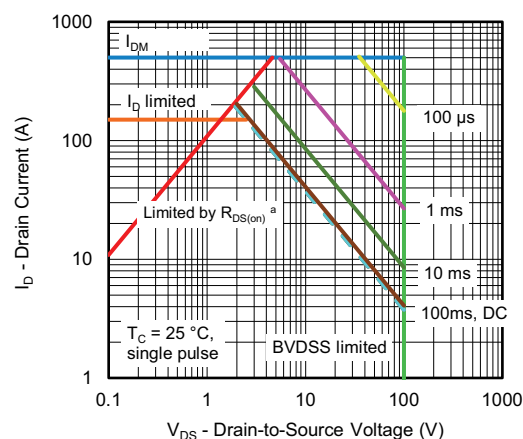
**On-Resistance vs. Gate-to-Source Voltage**



**Drain Source Breakdown vs. Junction Temperature**



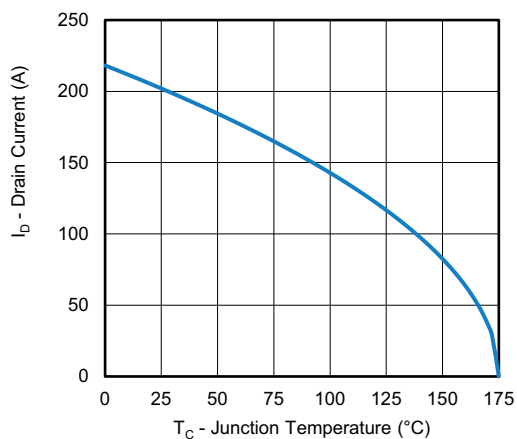
**Source Drain Diode Forward Voltage**



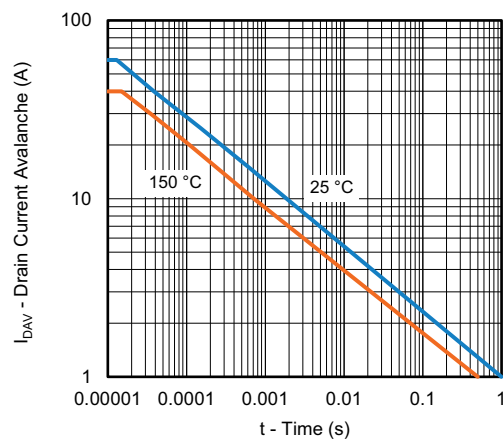
**Safe Operating Area**

**Note**

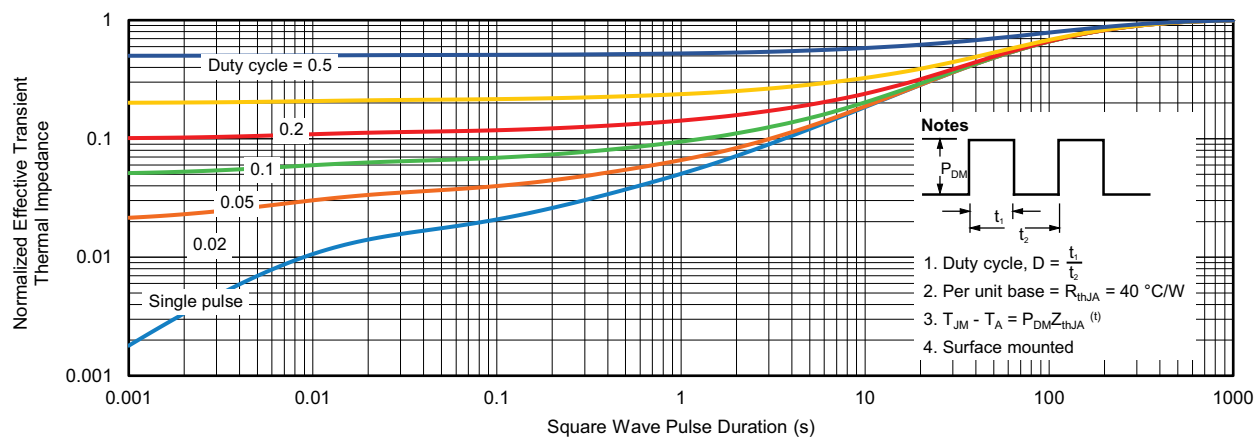
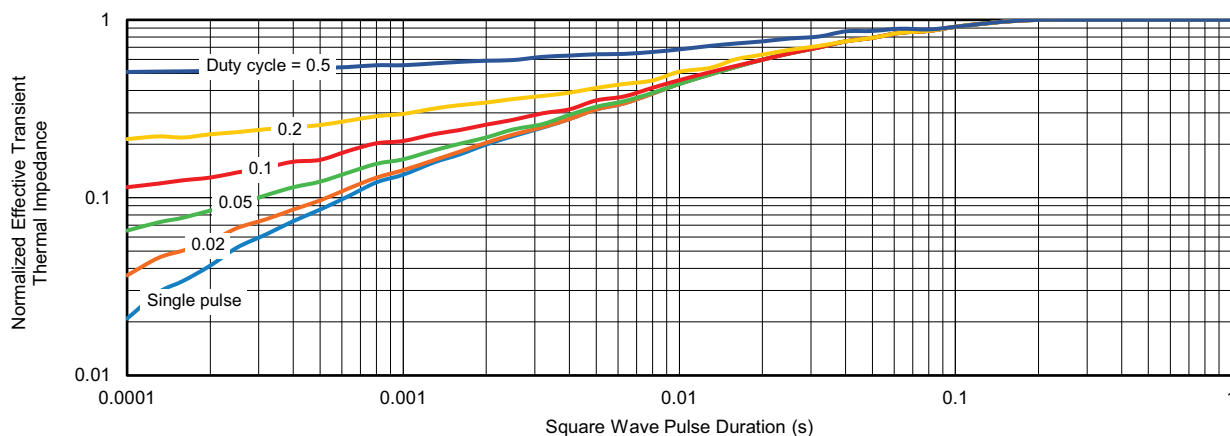
- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



Current De-Rating vs. Junction Temperature



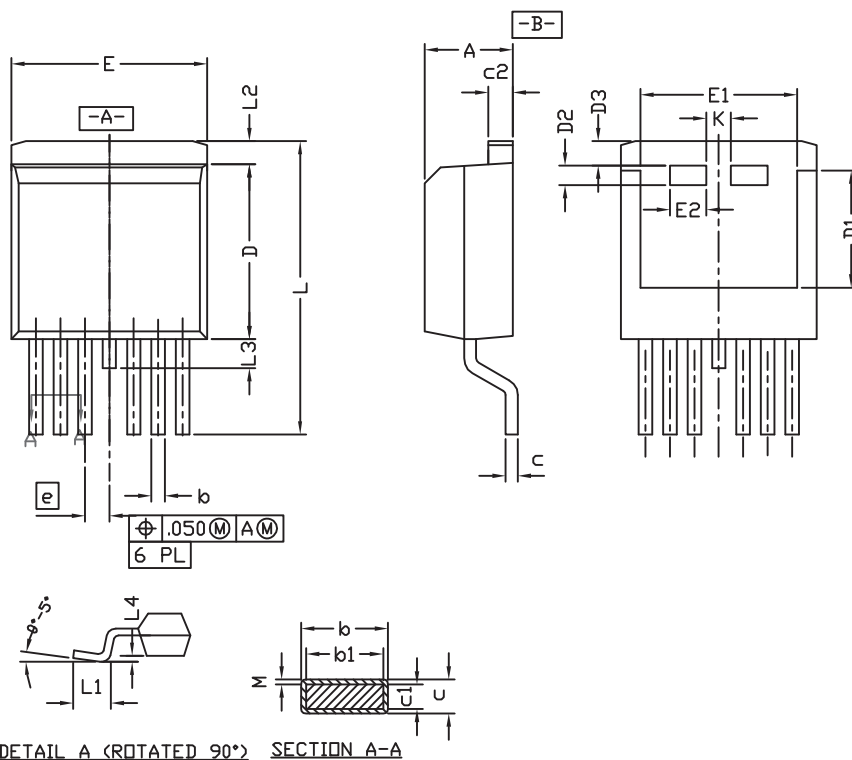
Avalanche Current vs. Time

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case****Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions


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## D<sup>2</sup>PAK (TO-263-7L) Case Outline

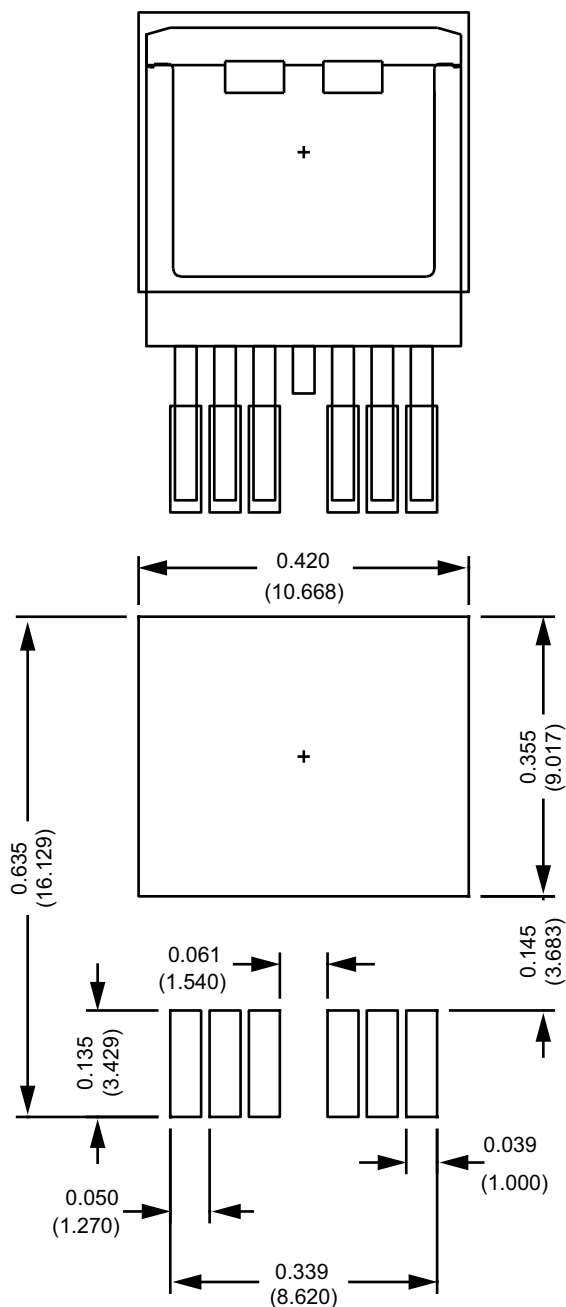


### Notes

1. Plane B includes maximum features of heat sink tab and plastic
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils
3. Pin to pin coplanarity max. 4 mils
4. Lead thickness 25 mils
5. For SUM part numbers lead thickness is 24 mils to 29 mils
6. For reference only
7. Use inches as the primary measurement
8. This feature is only for SUM

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.990
b1	0.020	0.035	0.508	0.889
c* SUB	0.012	0.018	0.305	0.457
c* SUM	0.022	0.028	0.559	0.711
c1	0.018	0.025	0.457	0.635
c2	0.045	0.055	1.143	1.397
D	0.340	0.380	8.636	9.652
D1	0.260	0.280	6.604	7.112
D2	0.046	0.050	1.168	1.270
D3	0.045	0.055	1.143	1.397
E	0.380	0.410	9.652	10.414
E1	0.245	-	6.223	-
E2	0.072	0.078	1.829	1.981
	0.050 BSC		1.27 BSC	
K	0.045	0.055	1.143	1.397
L	0.575	0.625	14.605	15.875
L1	0.090	0.110	2.286	2.794
L2	0.040	0.055	1.016	1.397
L3	0.050	0.070	1.270	1.778
L4	0.010 BSC		0.254 BSC	
M	-	0.002	-	0.050
ECN: T22-0410-Rev. D, 19-Sep-2022				
DWG: 6006				

## Recommended Land Pattern D<sup>2</sup>PAK (TO-263-7L)







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