

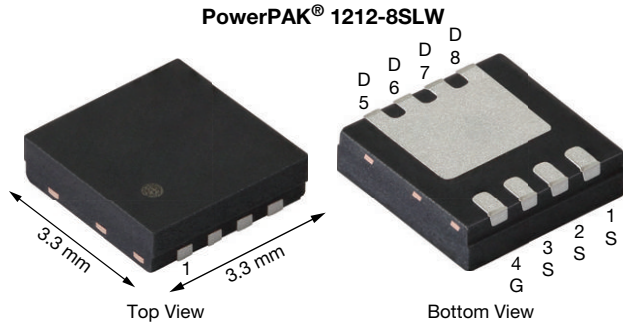
# Automotive N-Channel 72 V (D-S) 175 °C MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

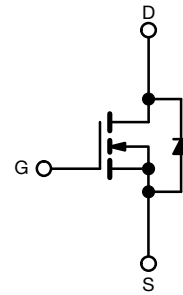
## FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>g</sub> and UIS tested
- Wettable flank terminals
- Low thermal resistance with 0.75 mm profile
- Material categorization:  
for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



Marking code: Q079

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	72
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.0095
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.0120
I <sub>D</sub> (A) <sup>a</sup>	54
Configuration	Single



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK® 1212-8SLW
Lead (Pb)-free and halogen-free	SQS178ELNW (for detailed order number please see <a href="http://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	V <sub>DS</sub>	72	V		
Gate-source voltage	V <sub>GS</sub>	± 20			
Continuous drain current <sup>a</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	54	A	
		T <sub>C</sub> = 125 °C	31		
Continuous source current (diode conduction) <sup>a</sup>	I <sub>S</sub>	59			
Pulsed drain current <sup>a, b</sup>	I <sub>DM</sub>	115			
Single pulse avalanche current	I <sub>AS</sub>	21			
Single pulse avalanche energy	E <sub>AS</sub>	22	mJ		
Maximum power dissipation <sup>a, b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	65	W	
		T <sub>C</sub> = 125 °C	21		
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		
Soldering recommendations (peak temperature) <sup>c</sup>		260			

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction-to-ambient	R <sub>thJA</sub>	54	°C/W	
Junction-to-case (drain) <sup>e</sup>	R <sub>thJC</sub>	2.3		

### Notes

- Values based on R<sub>thJC</sub> and T<sub>C</sub> of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- When mounted on 1" square PCB (FR4 material)
- As per on JESD51-14



SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	72	-	-	V	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2	1.7	2.5		
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA	
Zero gate voltage drain current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 72\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 72\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 72\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	20	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$	$I_D = 10\text{ A}$	-	0.0095	0.012	$\Omega$
		$V_{GS} = 10\text{ V}$		-	0.007	0.0095	
		$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0178	
		$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0220	
Forward transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 55\text{ A}$		-	76	-	S
<b>Dynamic <sup>b</sup></b>							
Input capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	1522	2131	$\mu\text{F}$
Output capacitance	$C_{OSS}$			-	264	370	
Reverse transfer capacitance	$C_{RSS}$			-	9	15	
Total gate charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 36\text{ V}, I_D = 4\text{ A}$	-	26	39	nC
Gate-source charge <sup>c</sup>	$Q_{gs}$			-	5	-	
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	5	-	
Gate resistance	$R_g$	f = 1 MHz		0.3	1.0	1.6	$\Omega$
Turn-on delay time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 36\text{ V}, R_L = 14.4\text{ }\Omega,$ $I_D \cong 2.5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	10	15	ns
Rise time <sup>c</sup>	$t_r$			-	3	6	
Turn-off delay time <sup>c</sup>	$t_{d(off)}$			-	23	35	
Fall time <sup>c</sup>	$t_f$			-	9	14	
<b>Source-Drain Diode Ratings and Characteristic <sup>b</sup></b>							
Pulsed current <sup>a</sup>	$I_{SM}$			-	-	115	A
Forward voltage	$V_{SD}$	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$		-	0.82	1.1	V
Body diode reverse recovery time	$t_{rr}$	$V_{DD} = 58\text{ V}, I_{FM} = 3.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $R = 10\text{ }\Omega, L = 0.3\text{ mH}, \text{ pulse width} = 2\text{ }\mu\text{s}$		-	30	60	ns
Body diode reverse recovery charge	$Q_{rr}$			-	23	46	nC
Reverse recovery fall time	$t_a$			-	15	-	
Reverse recovery rise time	$t_b$			-	15	-	ns
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-1.3	-	A

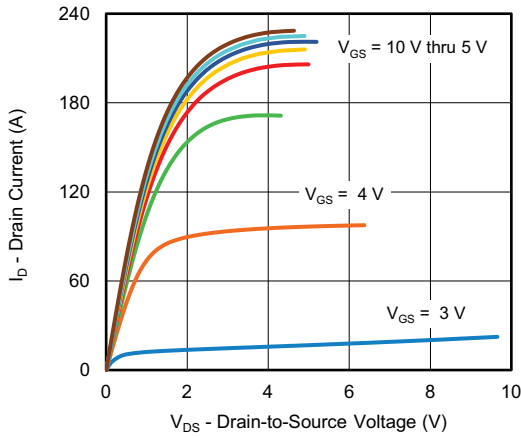
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

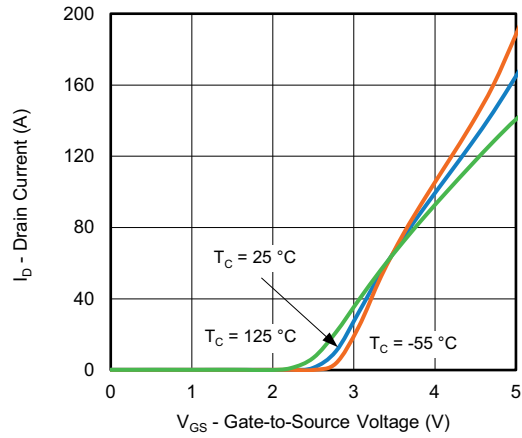
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



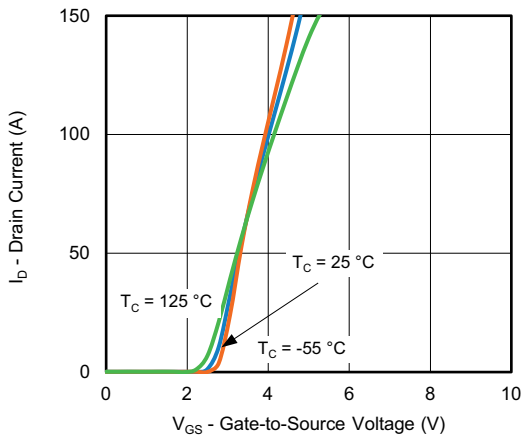
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



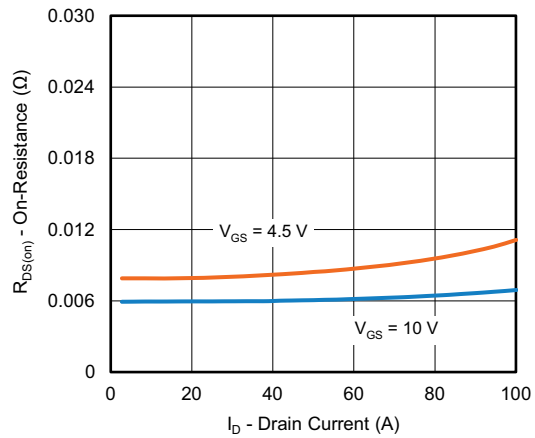
Output Characteristics



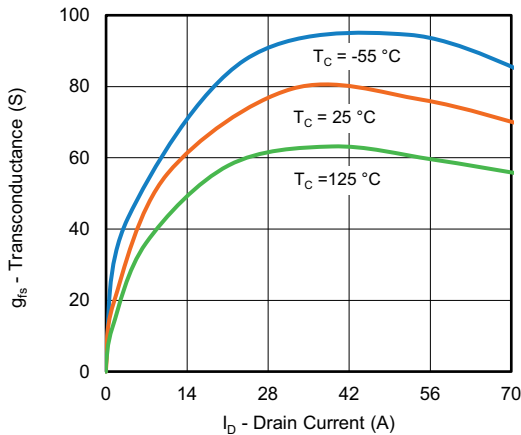
Transfer Characteristics



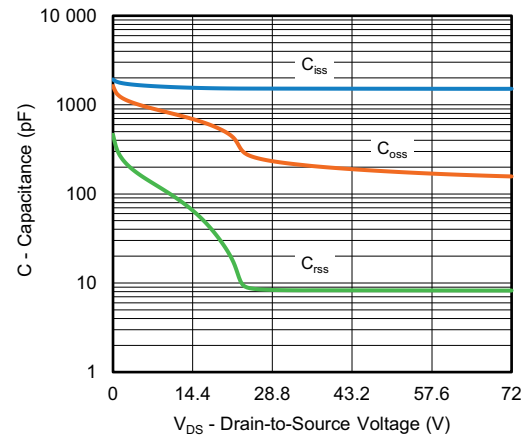
Transfer Characteristics



On-Resistance vs. Drain Current



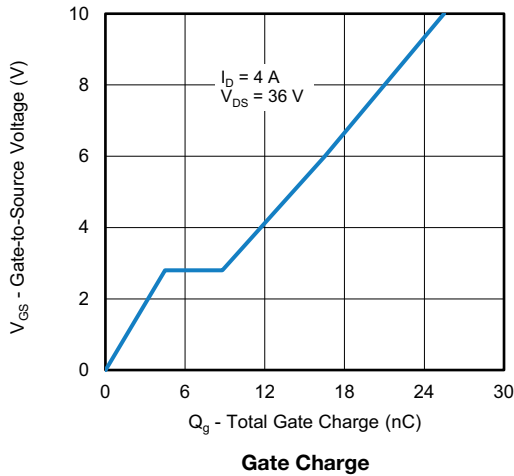
Transconductance



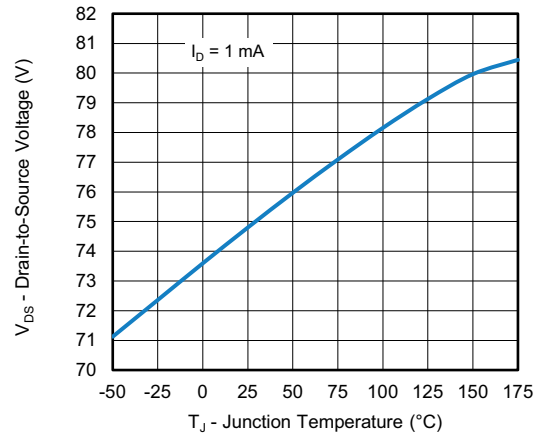
Capacitance



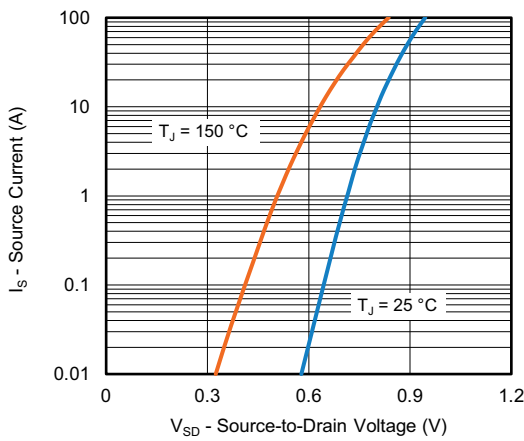
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



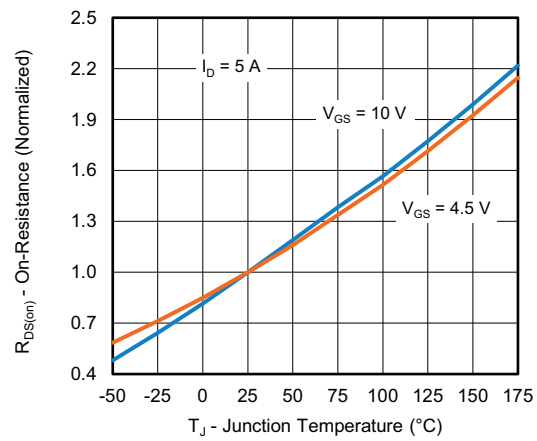
Gate Charge



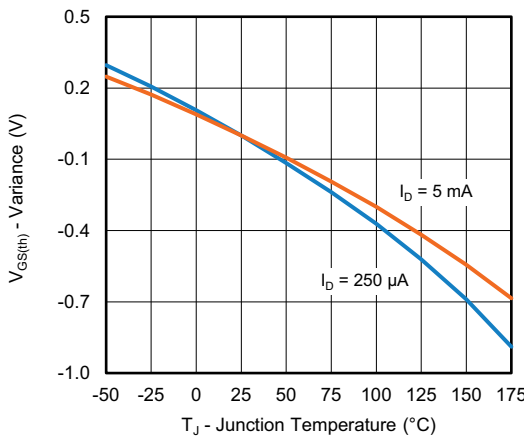
Drain Source Breakdown vs. Junction Temperature



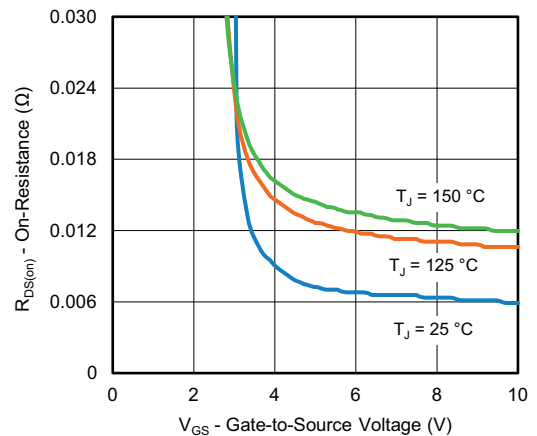
Source Drain Diode Forward Voltage



On-Resistance vs. Junction Temperature



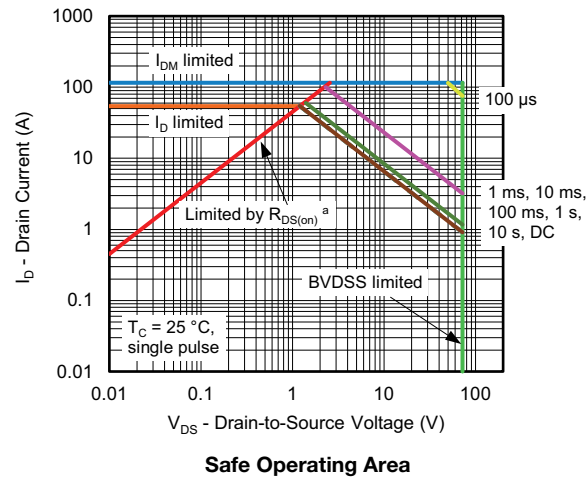
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

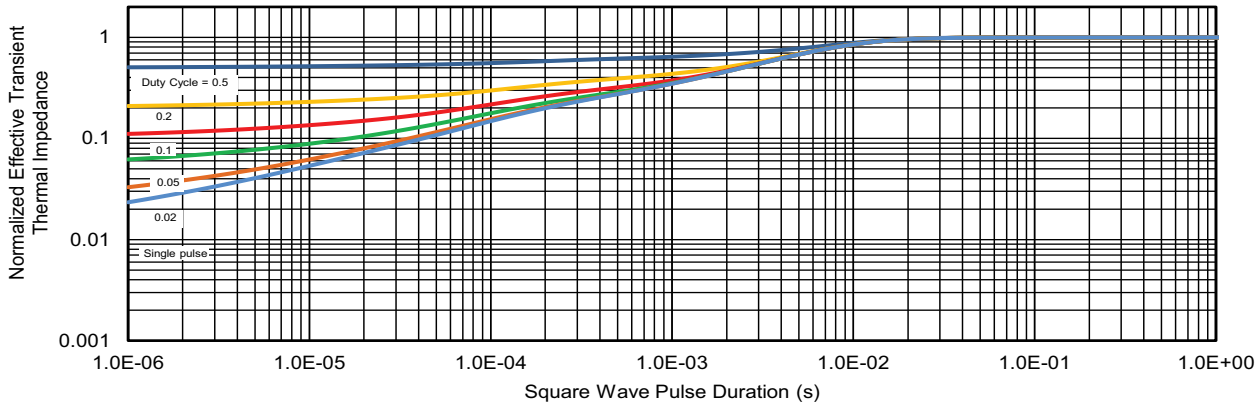


**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

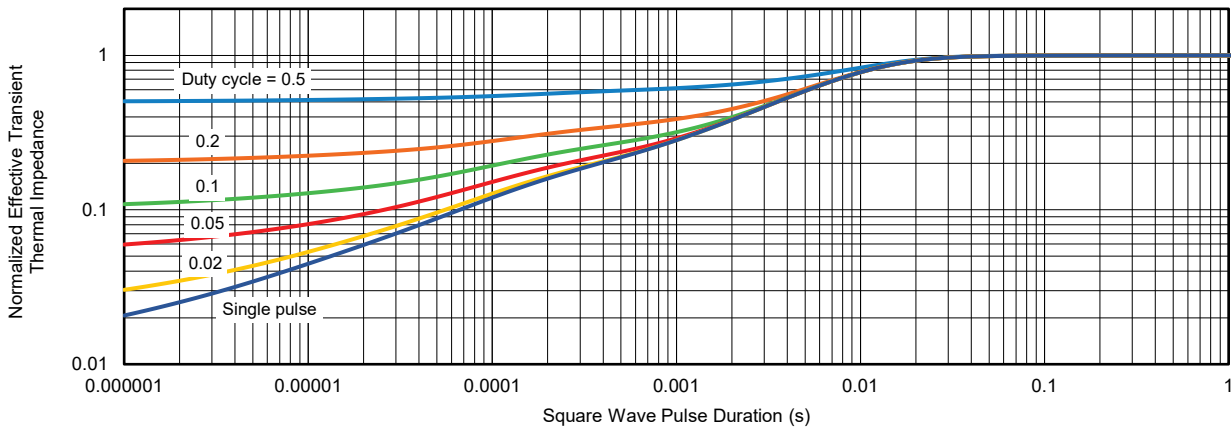


**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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