

## N-Channel 30 V (S1-S2) MOSFET

### DESCRIPTION

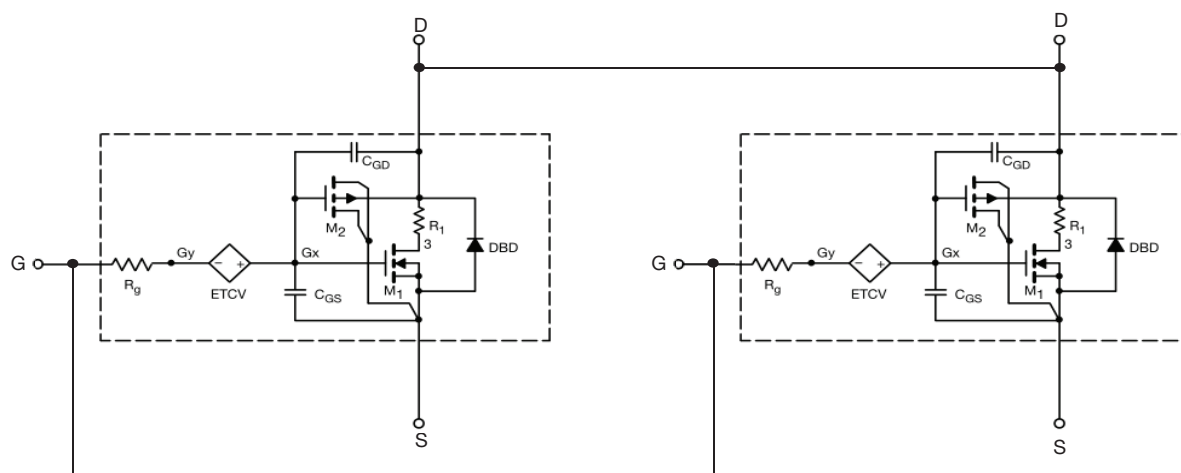
The attached SPICE model describes the typical electrical characteristics of the N-Channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +150 °C temperature ranges under the pulsed -12 V to +16 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +150 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



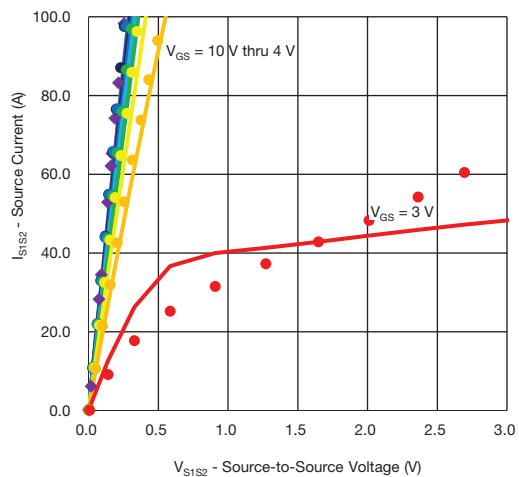
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>S1S2</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.6	-	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>S1S2</sub> = 7 A	0.0029	0.0030	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>S1S2</sub> = 5 A	0.0044	0.0043	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>S1S2</sub> = 35 A	193	115	S
Dynamic <sup>b</sup>					
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	2598	2600	pF
Output capacitance	C <sub>oss</sub>		1073	1100	
Reverse transfer capacitance	C <sub>rss</sub>		74	65	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A	40	40	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	18	19	
Gate-drain charge	Q <sub>gd</sub>		6.6	7.2	
			3.9	4.7	
Drain-source body diode characteristics					
Input capacitance	t <sub>rr</sub>	I <sub>F</sub> = 5 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	29	38	ns
Output capacitance	Q <sub>rr</sub>		27	28	nC
Reverse transfer capacitance	t <sub>a</sub>		19	20	ns
Gate-source threshold voltage	t <sub>b</sub>		10	17	

**Notes**

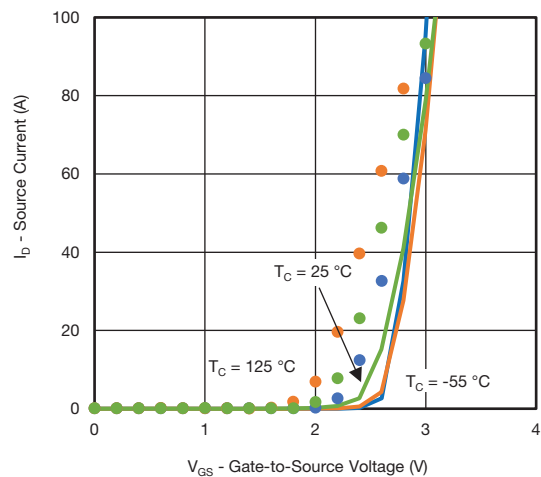
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing



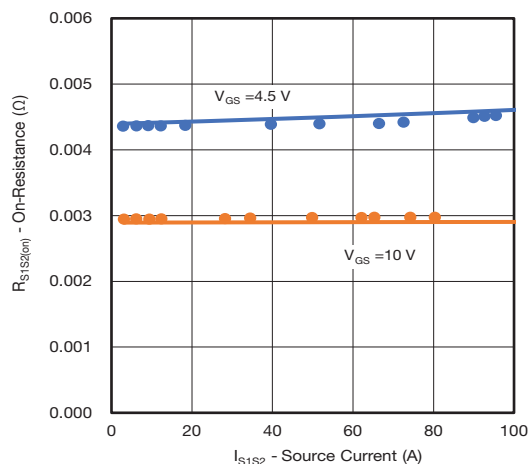
## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)



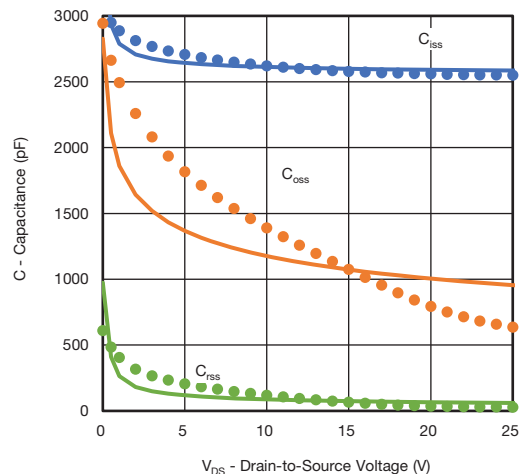
Output Characteristics



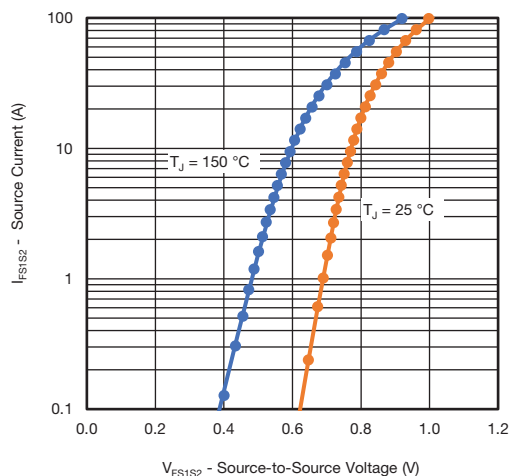
Transfer Characteristics



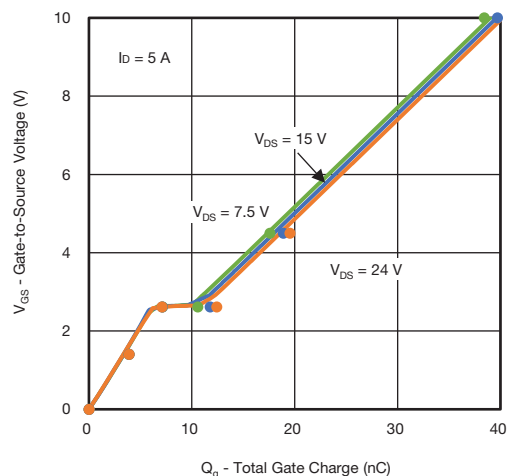
On-Resistance vs. Source Current and Gate Voltage



Capacitance



Source-Drain Diode Forward Voltage



Gate Charge

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