Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® 1212-8W Single Top View **Bottom View**

Marking code: Q080

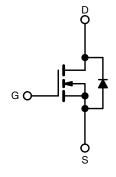
PRODUCT SUMMARY				
V _{DS} (V)	40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0079			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0105			
I _D (A)	16			
Configuration	Single			

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS COMPLIANT HALOGEN **FREE**



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK® 1212-8W
Lead (Pb)-free and halogen-free	SQS488CENW
Leau (FD)-II ee aliu lialogeli-II ee	(for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	V	
Gate-source voltage		V _{GS}	± 20		
Continuous drain current ^a	T _C = 25 °C	- I _D	16		
	T _C = 125 °C		16		
Continuous source current (diode conduction) ^a		Is	16	Α	
Pulsed drain current ^b		I _{DM}	64		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	19		
Single pulse avalanche energy	L = U.T IIII	E _{AS}	18	mJ	
Maximum power dissipation	T _C = 25 °C	D-	39.47	- W	
	T _C = 125 °C	P _D	13.16		
Operating junction and storage temperature range Soldering recommendations (peak temperature) d, e		T _J , T _{stg}	-55 to +175	°C	
			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount c	R _{thJA}	81	°C/W	
Junction-to-case (drain)		R_{thJC}	3.8]	

Notes

- a. Package limited
 b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
 c. When mounted on 1" square PCB (FR4 material)
 d. See solder profile (www.vishav.com/doc?73257). The PowerPAK 1212-8W is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		40	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$		1.5	2.0	2.5		
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1		
Zero gate voltage drain current		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	=-	-	50	μA	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150		
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 \text{ V}$	15	-	-	Α	
		V _{GS} = 10 V	I _D = 10 A	-	0.0064	0.0079		
	Б	V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.0118		
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0140	Ω	
		V _{GS} = 4.5 V	I _D = 10 A	-	0.0087	0.0105		
Forward transconductance b	9 _{fs}	V _{DS}	= 15 V, I _D = 10 A	-	50	-	S	
Dynamic ^b		•						
Input capacitance	C _{iss}		V _{GS} = 0 V V _{DS} = 25 V, f = 1 MHz	-	1318	1850	рF	
Output capacitance	C _{oss}	$V_{GS} = 0 V$		-	321	450		
Reverse transfer capacitance	C _{rss}			-	31	43		
Total gate charge ^c	Qg			-	22	35	nC	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_D = 4 \text{ A}$	-	4	-		
Gate-drain charge ^c	Q _{gd}				3.7	-		
Gate resistance	R _g	f = 1 MHz		0.5	1.0	1.5	Ω	
Turn-on delay time ^c	t _{d(on)}				11	18	ns	
Rise time ^c	t _r	V_{DD} = 20 V, R_L = 5 Ω $I_D \cong$ 4 A, V_{GEN} = 10 V, R_g = 1 Ω		-	3	5		
Turn-off delay time ^c	t _{d(off)}			-	20	30		
Fall time ^c	t _f			-	4	7		
Source-Drain Diode Ratings and Charact	eristic ^b							
Pulsed current ^a	I _{SM}			-	-	64	Α	
Forward voltage	V _{SD}	I _F = 10 A, V _{GS} = 0 V		-	0.82	1.1	V	
Body diode reverse recovery time	t _{rr}	I _F = 5 A, di/dt = 100 A/μs		-	24	48	ns	
Body diode reverse recovery charge	Q _{rr}			-	12	24	nC	
Reverse recovery fall time	ta			-	11	-		
Reverse recovery rise time	t _b			-	13	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			_	-0.9	-	Α	

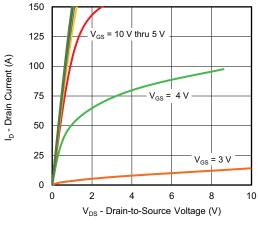
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

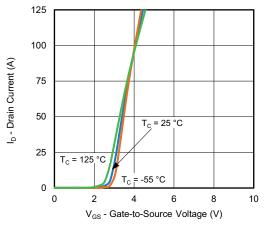
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



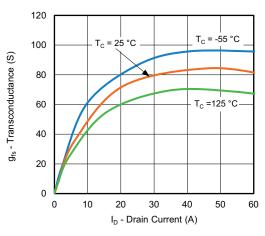
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



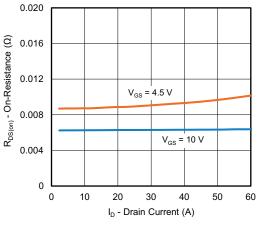




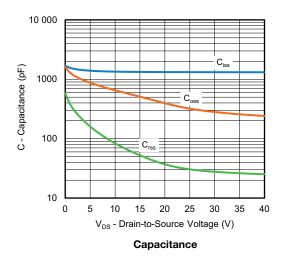
Transfer Characteristics

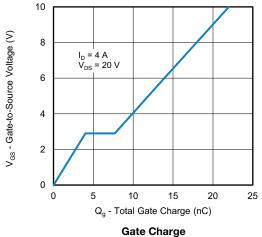


Transconductance



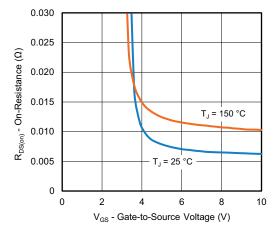
On-Resistance vs. Drain Current



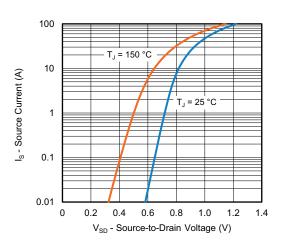




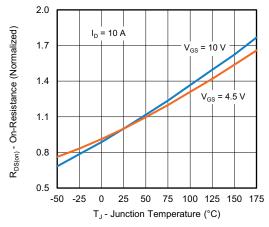
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



On-Resistance vs. Gate-to-Source Voltage

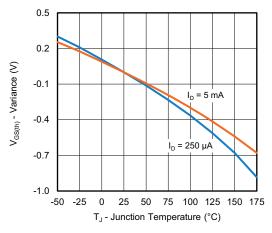


Source Drain Diode Forward Voltage

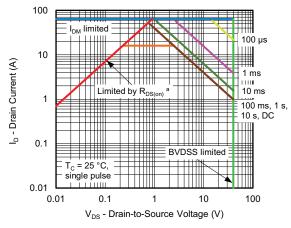


On-Resistance vs Junction Temperature

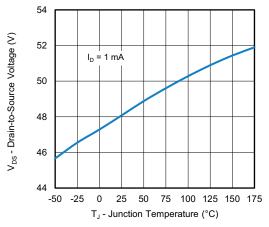
Note a. $V_{GS} > minimum V_{GS}$ at which $R_{DS(on)}$ is specified



Threshold Voltage



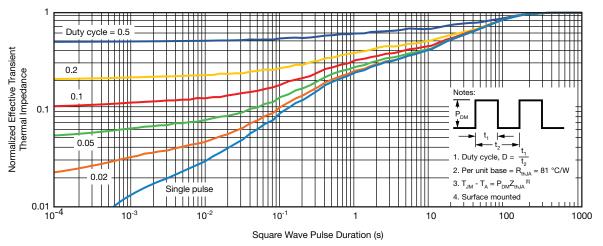
Safe Operating Area



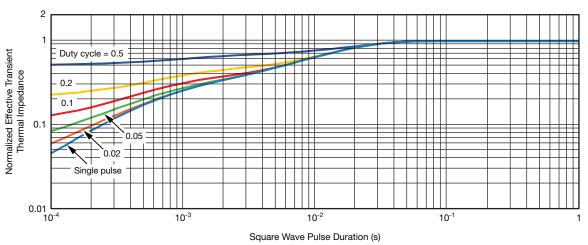
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62236.



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