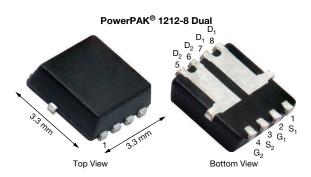


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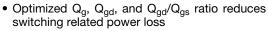
Dual N-Channel 40-V (D-S) MOSFET

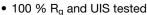


PRODUCT SUMMARY				
V _{DS} (V)	40			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.012			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.017			
Q _g typ. (nC)	4.7			
I _D (A) a	34			
Configuration	Dual			

FEATURES

- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device





• Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

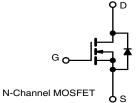


RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- · Load switch
- · Motor drive control
- · Battery management



ORDERING INFORMATION				
Package	PowerPAK 1212-8			
Lead (Pb)-free and halogen-free	SiS9446DN-T1-GE3			

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	V	
Gate-source voltage		V _{GS}	+20 / -16	V	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		34		
	T _C = 70 °C		24		
	T _A = 25 °C	I _D	11.3 ^{b, f}		
	T _A = 70 °C		9 ь	Α	
Pulsed drain current (t = 100 µs)		I _{DM}	60	A	
Continuous source-drain diode current	T _C = 25 °C	,	21		
	T _A = 25 °C	l _S	2.4 ^b		
Single pulse avalanche current		I _{AS}	13		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	8.2	mJ	
Maximum power dissipation	T _C = 25 °C		23		
	T _C = 70 °C	1 _ 🗆	13	,	
	T _A = 25 °C	P _D	2.6 ^{b, f}	W	
	T _A =70 °C		1.7 b, f		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) c			260		

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient b, e	t ≤ 10 s	R_{thJA}	38	48	°C/W		
Maximum junction-to-case (drain)	Steady state	R _{th.IC}	4.3	5.4	C/VV		

Notes

- a. $T_C = 25$ °C
- b. Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 94 $^{\circ}$ C / W t = 10 s

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA	-	26	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-4.5	-		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.1	-	2.3	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20 \text{ / } -16 \text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current		V _{DS} = 40 V, V _{GS} = 0 V	-	-	1		
	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 70 °C	-	-	10	μA	
Davis and a state of the same	5	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	0.0098	0.012		
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	i	0.0137	0.017	Ω	
Forward transconductance a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ A}$	i	40	-	S	
Dynamic ^b				<u>'</u>		•	
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	720	-	pF	
Output capacitance	C _{oss}		i	160	-		
Reverse transfer capacitance	C _{rss}		-	19	-		
Total coloredo o	0	Vps = 20 V, Vcs = 10 V, Ip = 10 A	-	10.2	16	nC	
Total gate charge	Q_g		i	4.7	7.1		
Gate-source charge	Q _{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	2.7	-		
Gate-drain charge	Q _{gd}		i	0.7	-		
Gate resistance	R_g	f = 1 MHz	0.6	3	6	Ω	
Turn-on delay time	t _{d(on)}		-	10	20		
Rise time	t _r	V_{DD} = 20 V, R_L = 2 Ω , $I_D \cong 10$ A,	-	5	10		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	15	30		
Fall time	t _f		-	5	10	1	
Turn-on delay time	t _{d(on)}		-	14	30	ns	
Rise time	t _r	V_{DD} = 20 V, R_L = 2 Ω , $I_D \cong 10$ A,	-	90	180		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	13	30		
Fall time	t _f		-	6	15		
Drain-Source Body Diode Characteristi	cs						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	21		
Pulse diode forward current	I _{SM}		-	-	60	A	
Body diode voltage	V_{SD}	$I_S = 5 A, V_{GS} = 0 V$	-	0.85	1.1	٧	
Body diode reverse recovery time	t _{rr}		-	13	30	ns	
Body diode reverse recovery charge	Q _{rr}		-	5	10	nC	
Reverse recovery fall time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	5	-		
Reverse recovery rise time	t _b		-	8	-	ns	

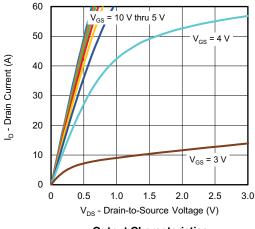
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

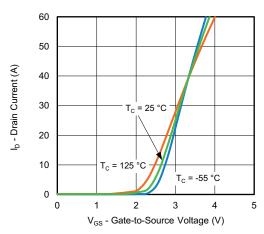
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



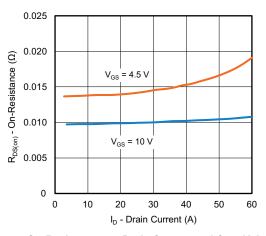
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



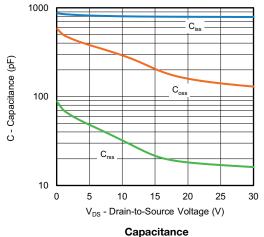
Output Characteristics



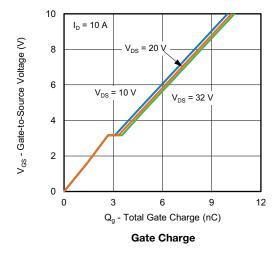
Transfer Characteristics

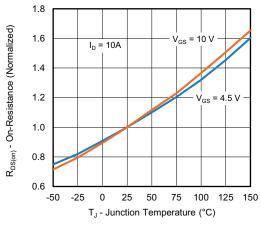


On-Resistance vs. Drain Current and Gate Voltage



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On-Resistance vs. Junction Temperature



0.04

0.03

0.02

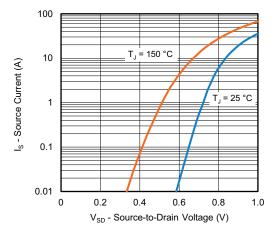
0.01

0

2

R_{DS(on)} - On-Resistance (Ω)

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Source-Drain Diode Forward Voltage



 $\label{eq:VGS} V_{GS} \mbox{ - Gate-to-Source Voltage (V)}$ $\mbox{On-Resistance vs. Gate-to-Source Voltage}$

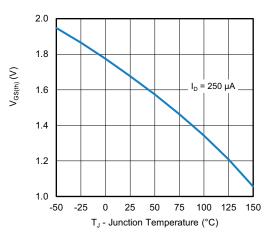
6

 $T_J = 125$ °C

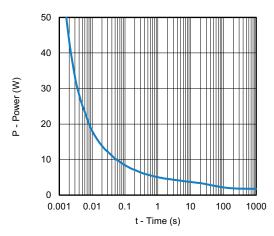
8

10

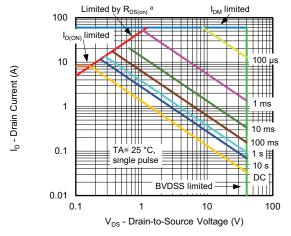
T_J = 25 °C



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



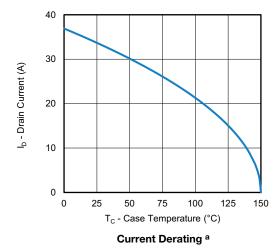
Safe Operating Area, Junction-to-Ambient

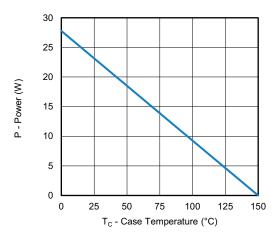
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





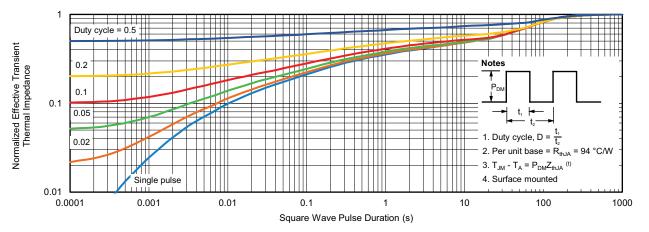
Power, Junction-to-Case

Note

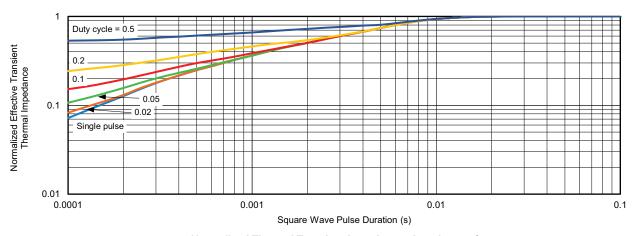
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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