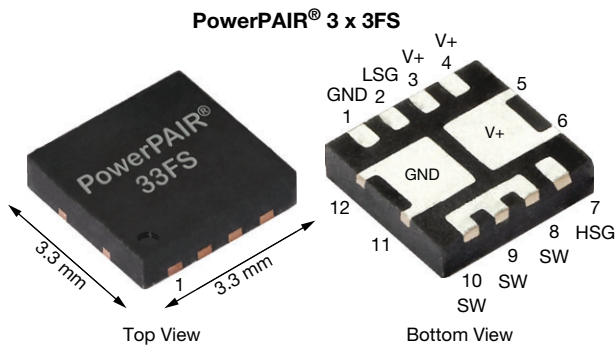


Dual N-Channel 80 V (D-S) MOSFET



FEATURES

- TrenchFET® Gen IV power MOSFET
- Symmetric dual n-channel
- Flip chip technology optimal thermal design
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized $R_{DS} - Q_g$ and $R_{DS} - Q_{gd}$ FOM elevates efficiency for high frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

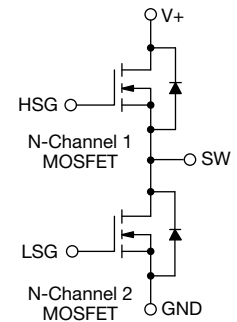


RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	80
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.019
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0238
Q_g typ. (nC)	7.1
I_D (A)	36 ^a
Configuration	Dual

APPLICATIONS

- Synchronous buck
- Half bridge
- POL
- Telecom DC/DC



ORDERING INFORMATION	
Package	PowerPAIR 3 x 3FS
Lead (Pb)-free and halogen-free	SiZF4800LDT-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	36
		$T_C = 70$ °C	29
		$T_A = 25$ °C	10 ^{b, c}
		$T_A = 70$ °C	8 ^{b, c}
Pulsed drain current ($t = 100$ μ s)	I_{DM}	40	A
Continuous source current (MOSFET diode conduction)	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	4.1 ^{b, c}
Single pulse avalanche current	I_{AS}	16	mJ
Single pulse avalanche energy	E_{AS}	13	
Maximum power dissipation	P_D	$T_C = 25$ °C	56.8
		$T_C = 70$ °C	36.4
		$T_A = 25$ °C	4.5 ^{b, c}
		$T_A = 70$ °C	2.9 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)		260	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s



THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	22	28	°C/W	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.7	2.2		

Notes

- a. Surface mounted on 1" x 1" FR4 board
b. Maximum under steady state conditions is 64 °C/W

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	80	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1	-	2	
Gate-source leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 80$ V, $V_{GS} = 0$ V	-	-	1	μ A
		$V_{DS} = 80$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	-	-	5	
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 10$ A	-	0.0160	0.019	Ω
		$V_{GS} = 4.5$ V, $I_D = 5$ A	-	0.0185	0.0238	
Forward transconductance ^a	g_{fs}	$V_{DS} = 10$ V, $I_D = 25$ A	-	50	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 40$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	950	-	pF
Output capacitance	C_{oss}		-	110	-	
Reverse transfer capacitance	C_{rss}		-	10	-	
C_{rss}/C_{iss} ratio			-	0.010	0.020	
Total gate charge	Q_g	$V_{DS} = 40$ V, $V_{GS} = 10$ V, $I_D = 10$ A	-	15	23	nC
Gate-source charge	Q_{gs}	$V_{DS} = 40$ V, $V_{GS} = 4.5$ V, $I_D = 10$ A	-	7.1	11	
Gate-drain charge	Q_{gd}		-	3.1	-	
Gate resistance	R_g		$f = 1$ MHz	0.20	0.95	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 40$ V, $R_L = 4$ Ω , $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω	-	10	20	ns
Rise time	t_r		-	5	10	
Turn-off delay time	$t_{d(off)}$		-	17	35	
Fall time	t_f		-	5	10	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 40$ V, $R_L = 4$ Ω , $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω	-	13	25	
Rise time	t_r		-	17	35	
Turn-off delay time	$t_{d(off)}$		-	16	30	
Fall time	t_f		-	6	15	
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25$ °C	-	-	52	A
Pulse diode forward current	I_{SM}		-	-	40	
Body diode voltage	V_{SD}	$I_S = 15$ A, $V_{GS} = 0$ V	-	0.85	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C	-	30	60	ns
Body diode reverse recovery charge	Q_{rr}		-	31	60	nC
Reverse recovery fall time	t_a		-	25	-	ns
Reverse recovery rise time	t_b		-	5	-	

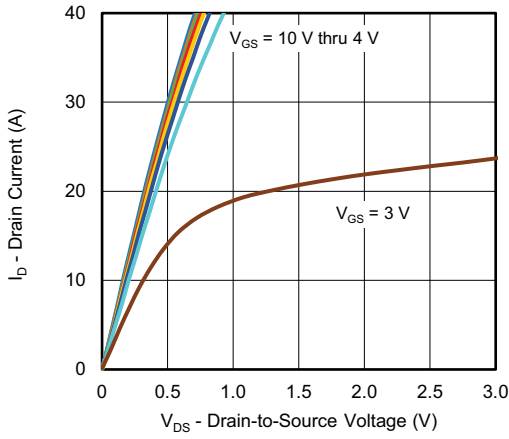
Notes

- a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

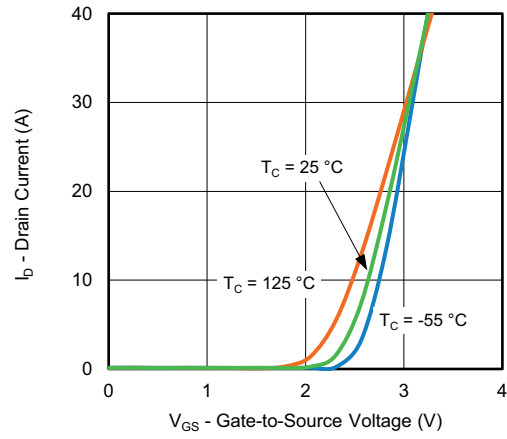
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



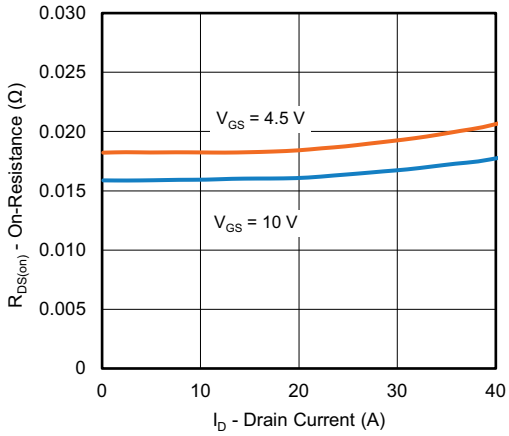
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



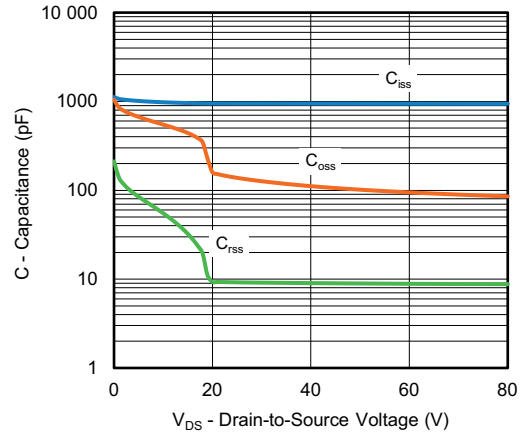
Output Characteristics



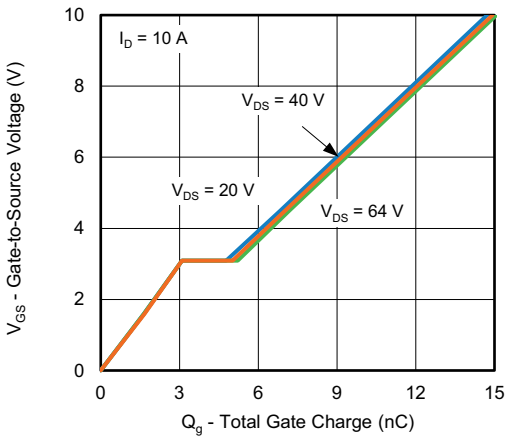
Transfer Characteristics



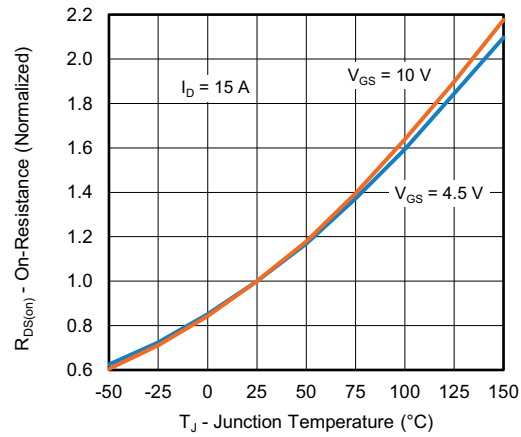
On-Resistance vs. Drain Current and Gate



Capacitance



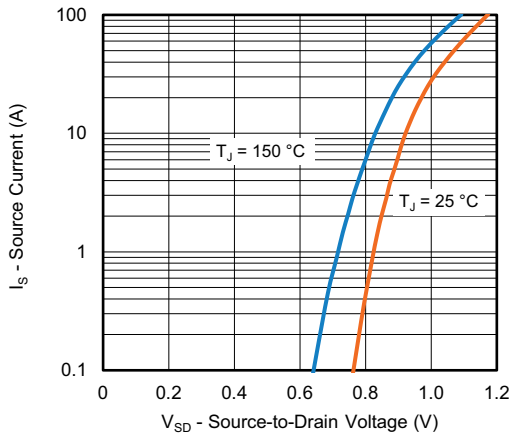
Gate Charge



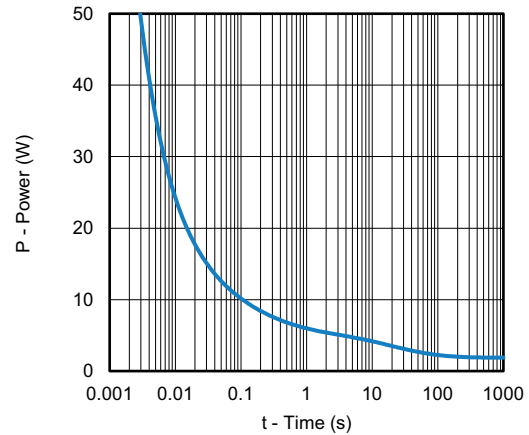
On-Resistance vs. Junction Temperature



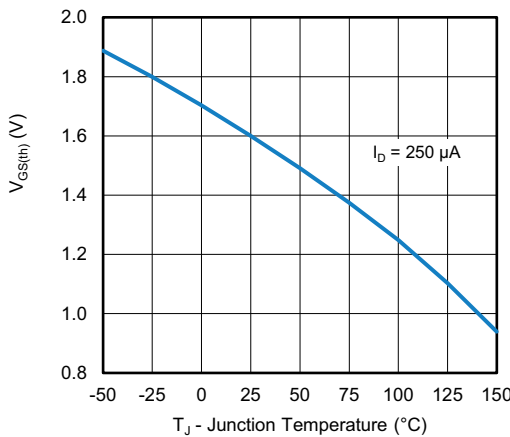
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



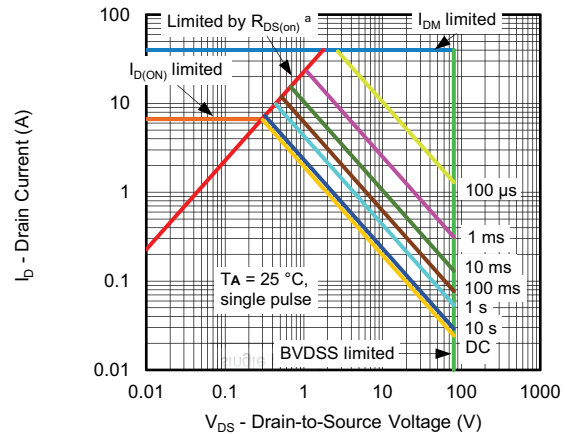
Source-Drain Diode Forward Voltage



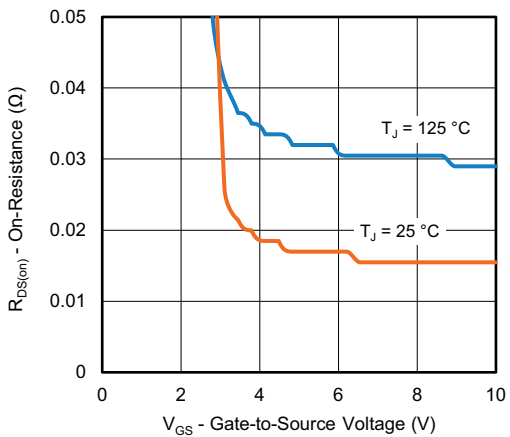
Single Pulse Power



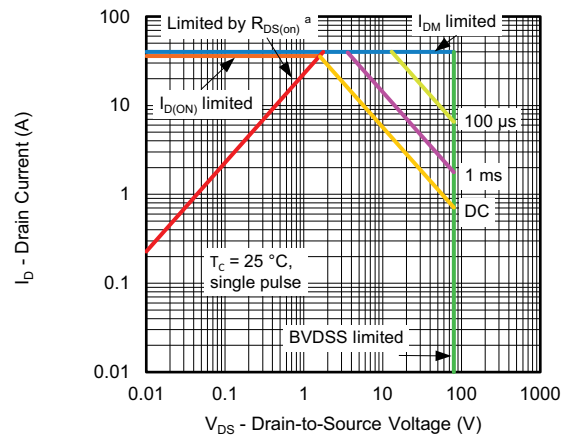
Threshold Voltage



Safe Operating Area, Junction to Ambient



On-Resistance vs. Gate-to-Source Voltage



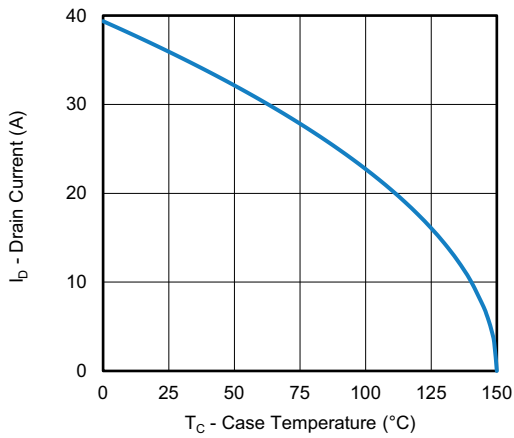
Safe Operating Area, Junction to Case

Note

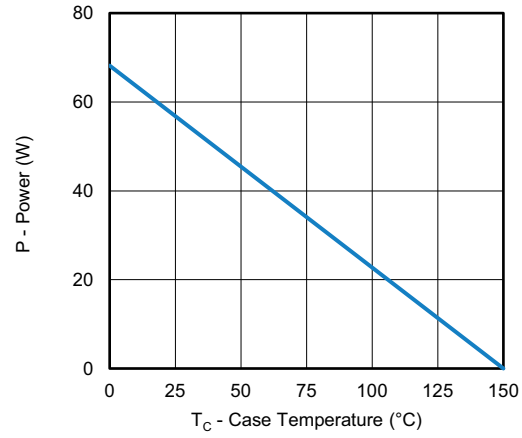
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



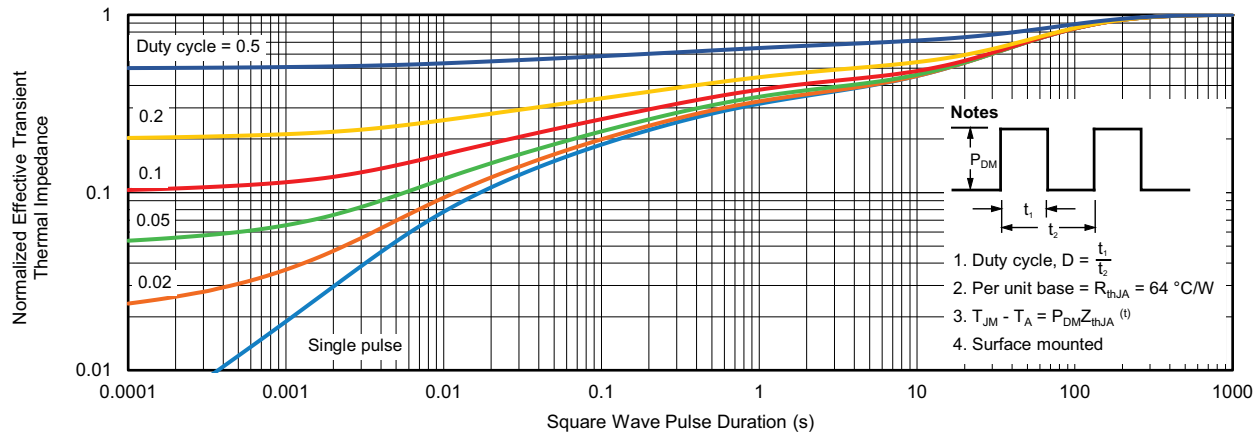
Power, Junction-to-Case

Notes

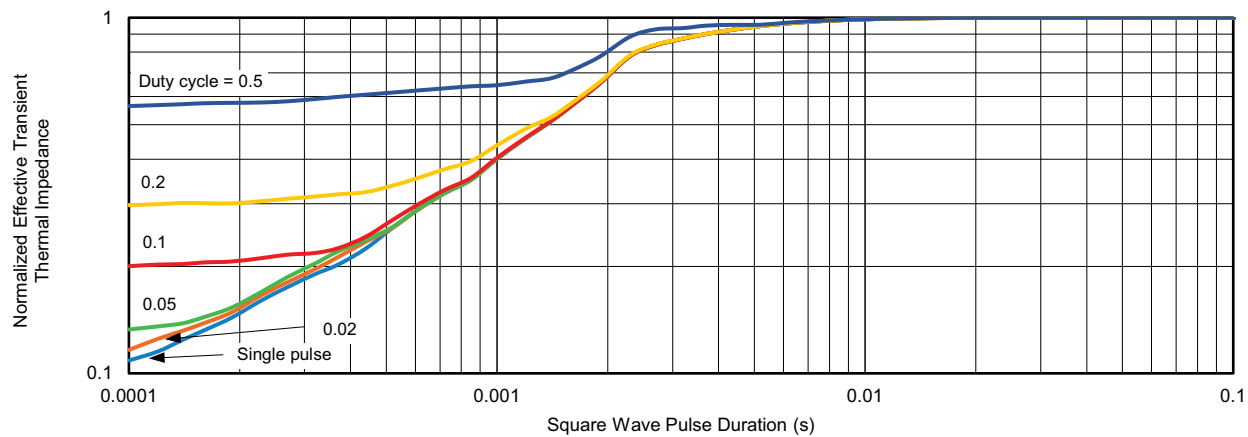
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- b. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



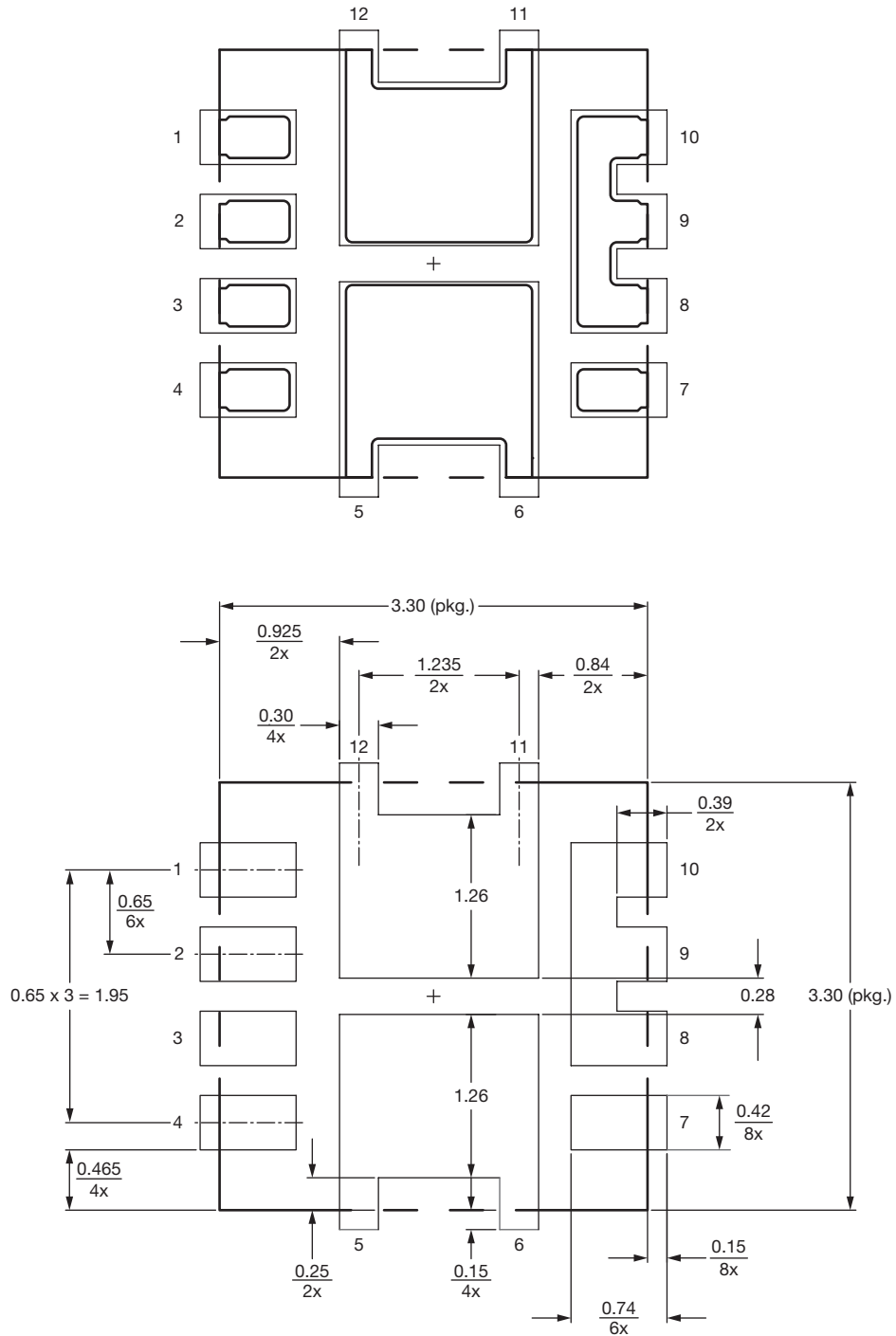
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62251.

Recommended Land Pattern PowerPAIR® 3 x 3FS BWL



Note

- Dimensions in mm

ECN: T23-0180-Rev. B, 16-May-2023
 DWG: 3006



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.