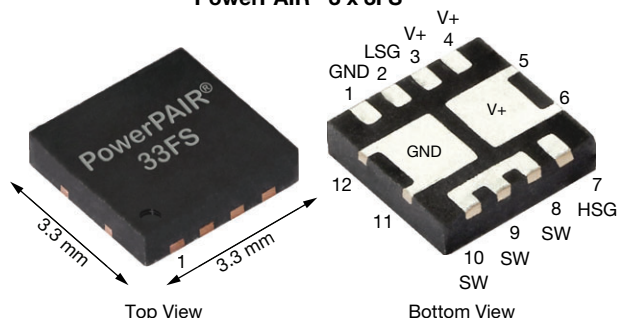


## Dual N-Channel 80 V (D-S) MOSFET

**PowerPAIR® 3 x 3FS**


### FEATURES

- TrenchFET® Gen IV power MOSFET
- Symmetric dual n-channel
- Flip chip technology optimal thermal design
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized  $R_{DS(on)}$  -  $Q_g$  and  $R_{DS(on)}$  -  $Q_{gd}$  FOM elevates efficiency for high frequency switching
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

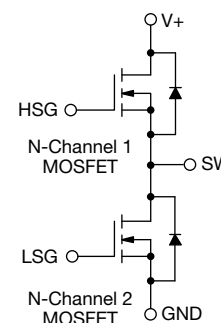

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### PRODUCT SUMMARY

$V_{DS}$ (V)	80
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.019
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0238
$Q_g$ typ. (nC)	7.1
$I_D$ (A)	36 <sup>a</sup>
Configuration	Dual

### APPLICATIONS

- Synchronous buck
- Half bridge
- POL
- Telecom DC/DC



### ORDERING INFORMATION

Package	PowerPAIR 3 x 3FS
Lead (Pb)-free and halogen-free	SiZF4800LDT-T1-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	80	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	36
		$T_C = 70$ °C	29
		$T_A = 25$ °C	10 <sup>b, c</sup>
		$T_A = 70$ °C	8 <sup>b, c</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	40	A
Continuous source current (MOSFET diode conduction)	$I_S$	$T_C = 25$ °C	52
		$T_A = 25$ °C	4.1 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	16	A
Single pulse avalanche energy	$E_{AS}$	13	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	56.8
		$T_C = 70$ °C	36.4
		$T_A = 25$ °C	4.5 <sup>b, c</sup>
		$T_A = 70$ °C	2.9 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature)		260	°C

#### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	22	28	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.7	2.2	

**Notes**

a. Surface mounted on 1" x 1" FR4 board

b. Maximum under steady state conditions is 64 °C/W

**SPECIFICATIONS** ( $T_J = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	-	2	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	5	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	0.0160	0.019	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	-	0.0185	0.0238	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 25 A	-	50	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	950	-	pF
Output capacitance	C <sub>oss</sub>		-	110	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	10	-	
C <sub>rss</sub> /C <sub>iss</sub> ratio			-	0.010	0.020	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	15	23	nC
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	-	7.1	11	
Q <sub>gs</sub>	-		3.1	-		
Q <sub>gd</sub>	-		2	-		
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.20	0.95	1.9	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	10	20	ns
Rise time	t <sub>r</sub>		-	5	10	
Turn-off delay time	t <sub>d(off)</sub>		-	17	35	
Fall time	t <sub>f</sub>		-	5	10	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	13	25	
Rise time	t <sub>r</sub>		-	17	35	
Turn-off delay time	t <sub>d(off)</sub>		-	16	30	
Fall time	t <sub>f</sub>		-	6	15	
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25°C	-	-	52	A
Pulse diode forward current	I <sub>SM</sub>		-	-	40	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 15 A, V <sub>GS</sub> = 0 V	-	0.85	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	30	60	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	31	60	nC
Reverse recovery fall time	t <sub>a</sub>		-	25	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	5	-	

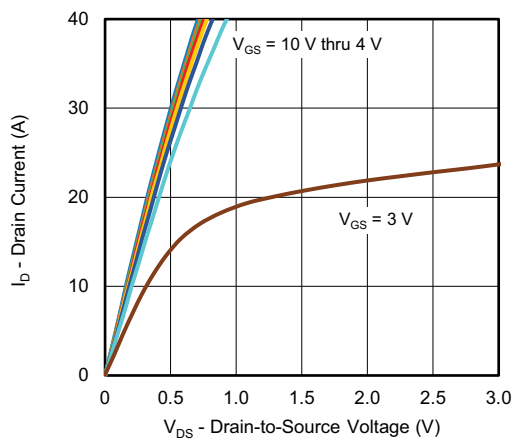
**Notes**a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %

b. Guaranteed by design, not subject to production testing

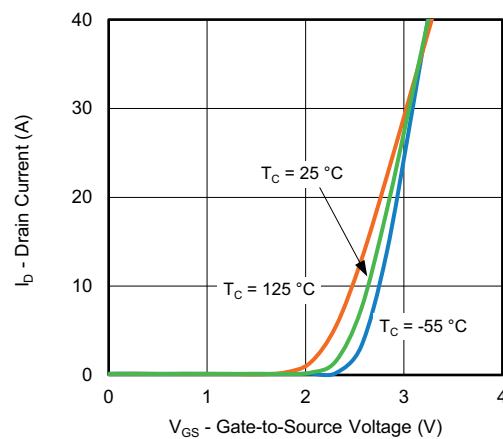
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



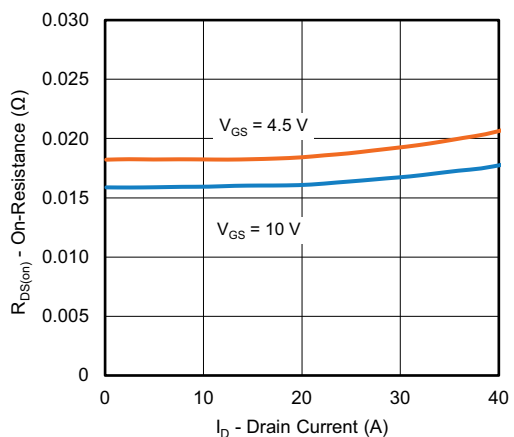
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



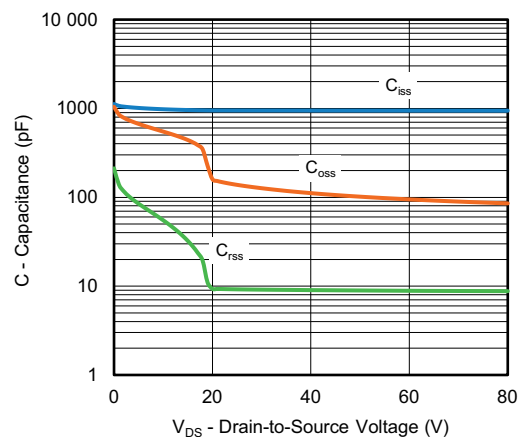
**Output Characteristics**



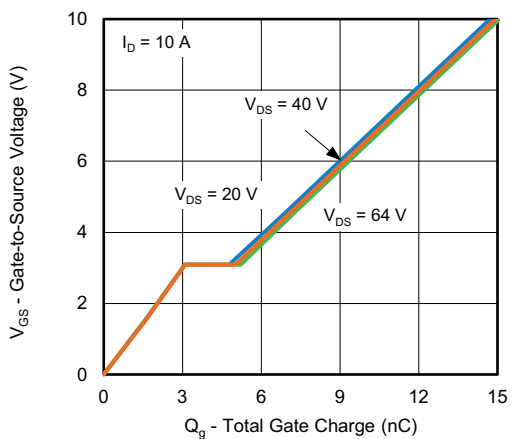
**Transfer Characteristics**



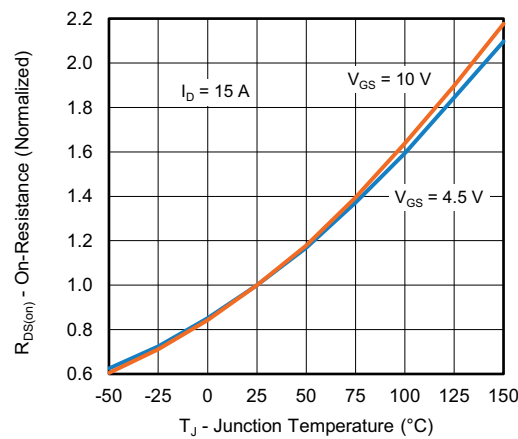
**On-Resistance vs. Drain Current and Gate**



**Capacitance**



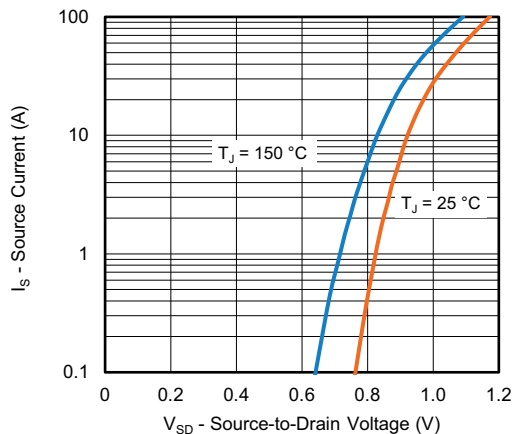
**Gate Charge**



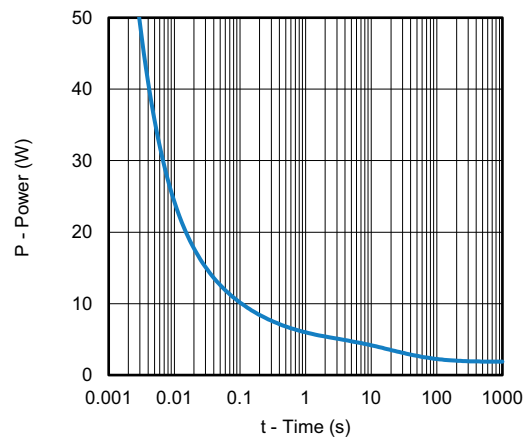
**On-Resistance vs. Junction Temperature**



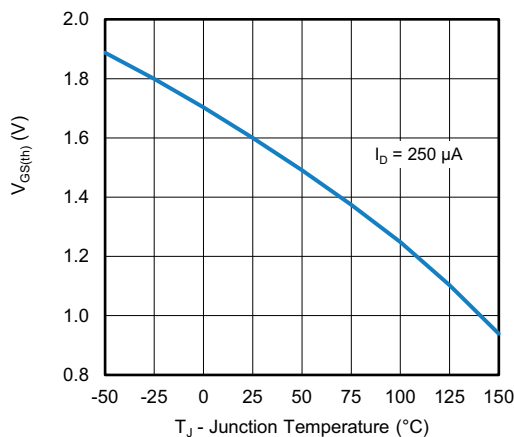
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



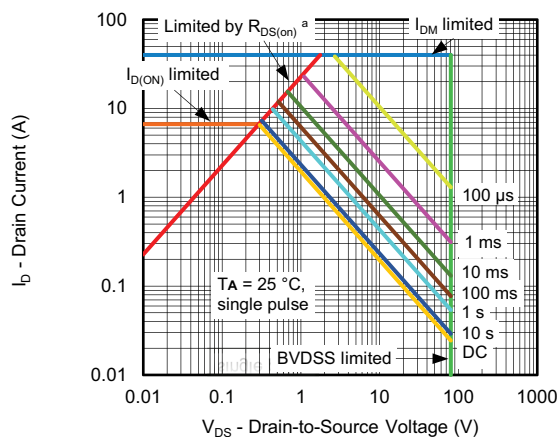
Source-Drain Diode Forward Voltage



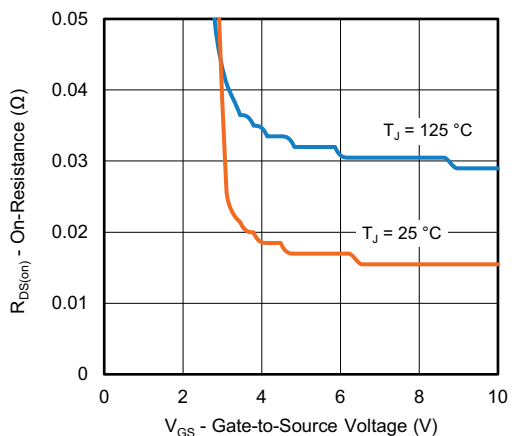
Single Pulse Power



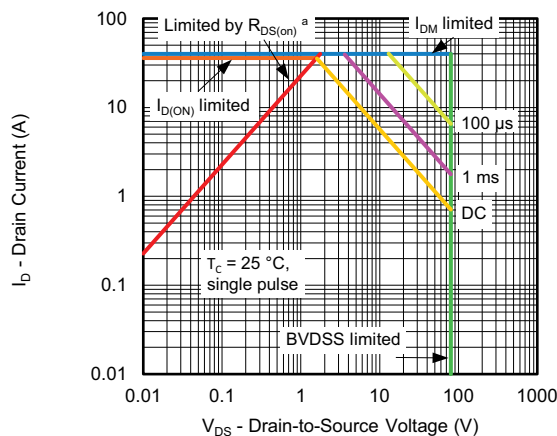
Threshold Voltage



Safe Operating Area, Junction to Ambient



On-Resistance vs. Gate-to-Source Voltage



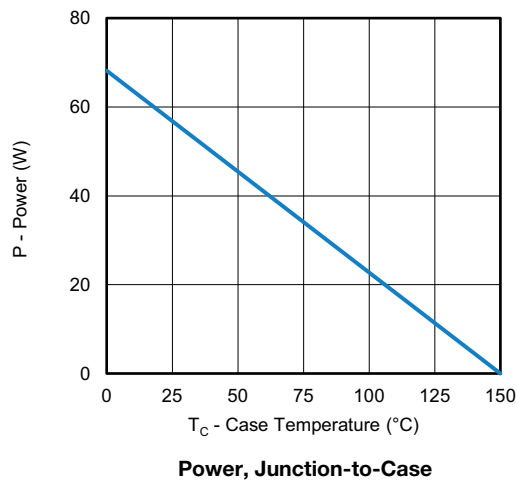
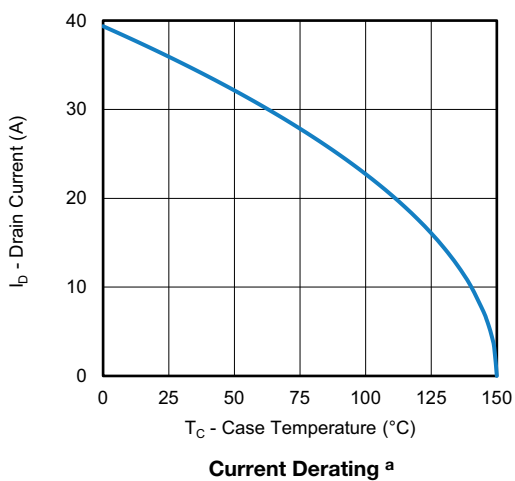
Safe Operating Area, Junction to Case

**Note**

- $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

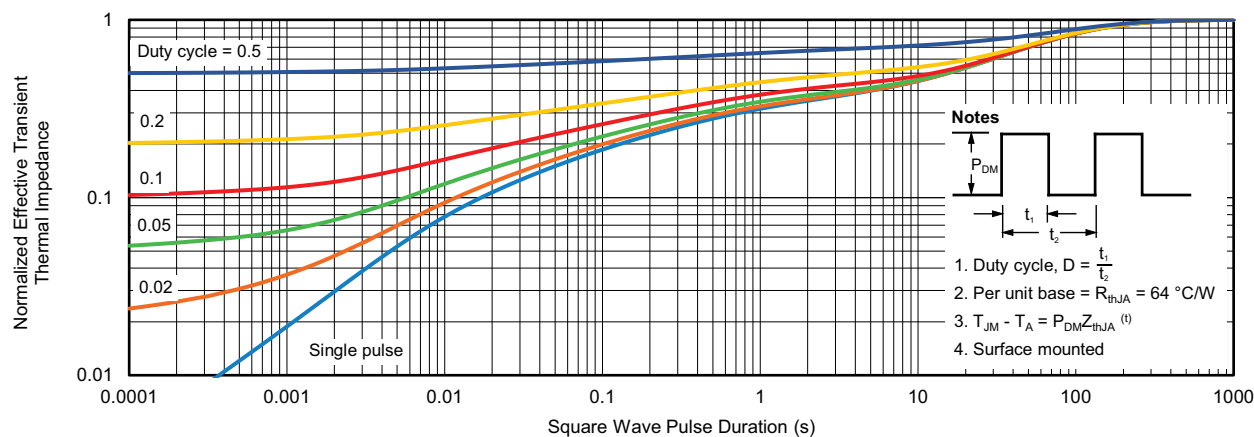


**Notes**

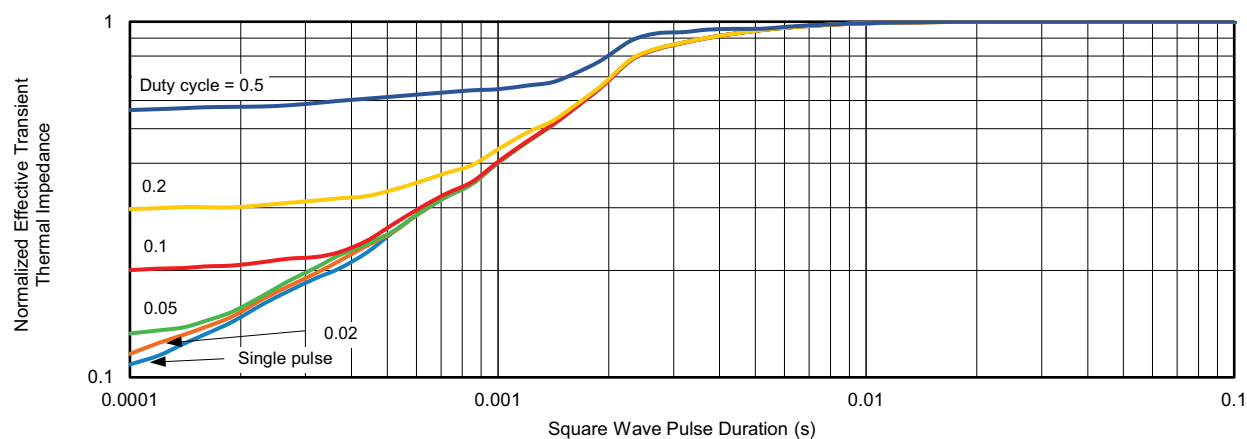
- The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



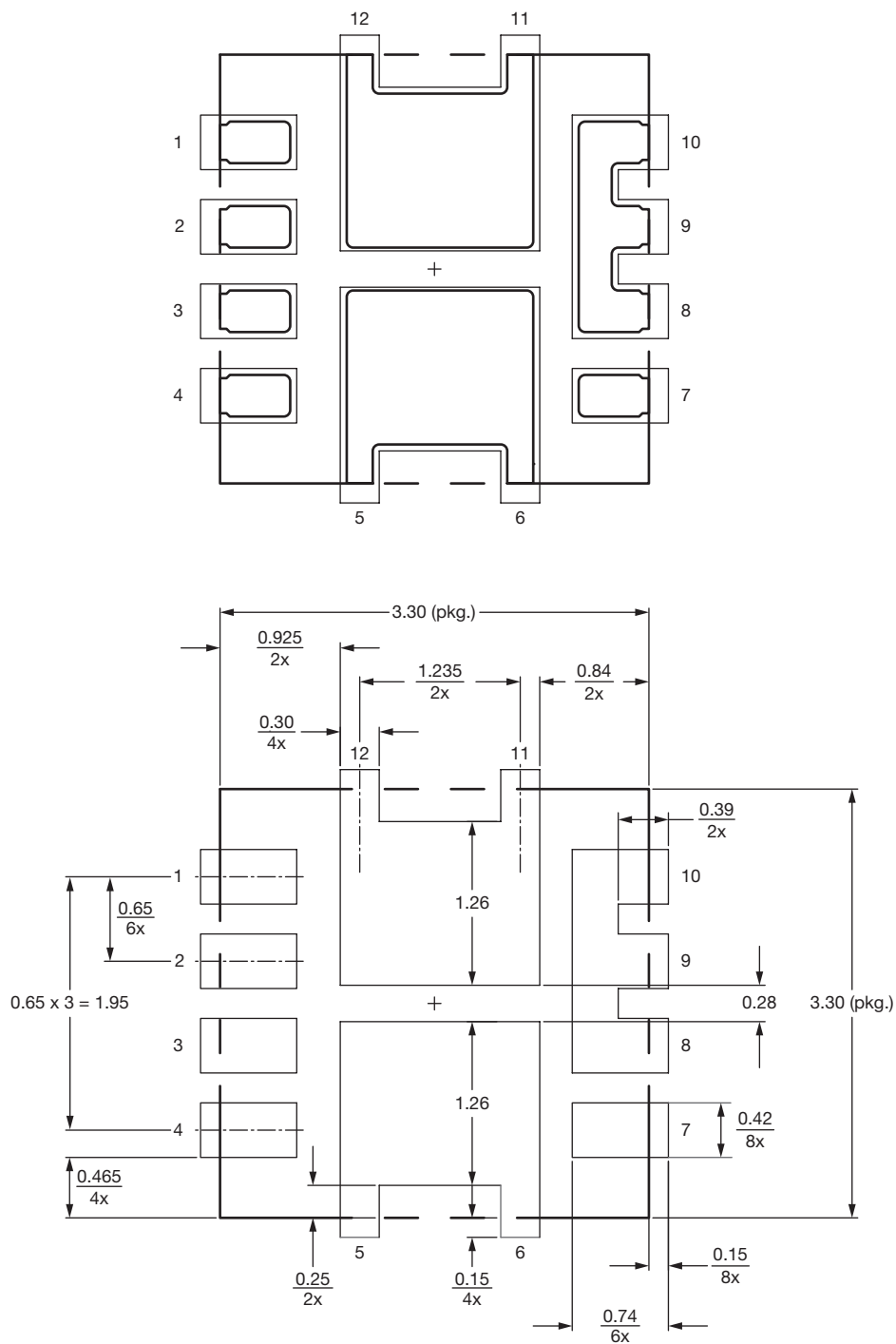
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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## Recommended Land Pattern PowerPAIR® 3 x 3FS BWL


**Note**

- Dimensions in mm

ECN: T23-0180-Rev. B, 16-May-2023  
DWG: 3006



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