N-Channel 100 V (D-S) MOSFET

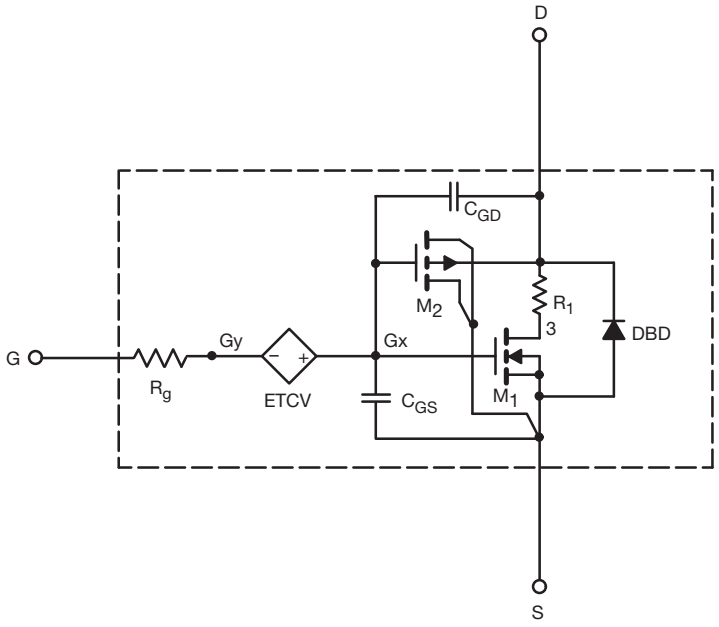
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the N-Channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +150 °C temperature ranges under the pulsed -20 V to +20 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +150 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

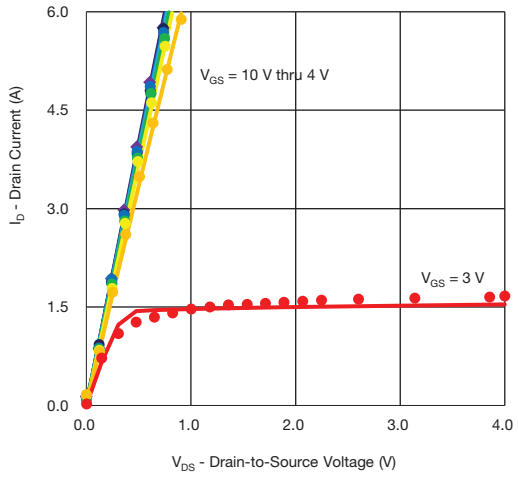
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.1	-	V
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2 A	0.125	0.124	Ω
		V_{GS} = 4.5 V, I_D = 1 A	0.141	0.138	
Forward transconductance [a]	g_{fs}	V_{DS} = 20 V, I_D = 2 A	8	12	S
Dynamic [b]					
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	288	290	pF
Output capacitance	C_{oss}		27	26	
Reverse transfer capacitance	C_{rss}		5	5	
Total gate charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 0.5 A	4.7	4.7	nC
		V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 0.5 A	2.2	2.2	
Gate-source charge	Q_{gs}		0.7	1	
Gate-drain charge	Q_{gd}		0.8	0.5	
Drain-source body diode characteristics					
Body diode voltage	V_{SD}	I_S = 1.6 A	0.84	0.8	V
Body diode reverse recovery time	t_{rr}	I_F = 1.6 A, di/dt = 100 A/µs, T_J = 25 °C	21	21	ns
Body diode reverse recovery charge	Q_{rr}		18	21	nC
Reverse recovery fall time	t_a		17	19	ns
Reverse recovery rise time	t_b		4	2	

Notes

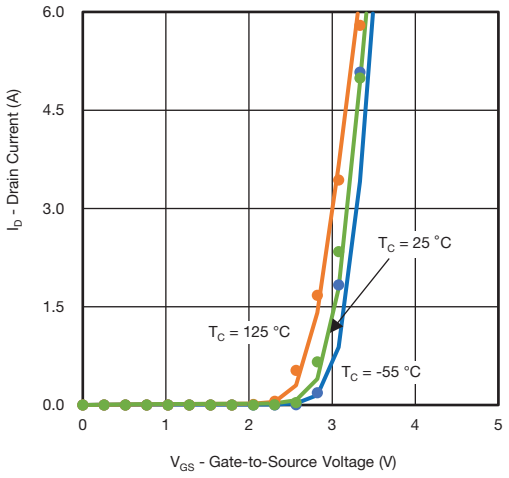
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

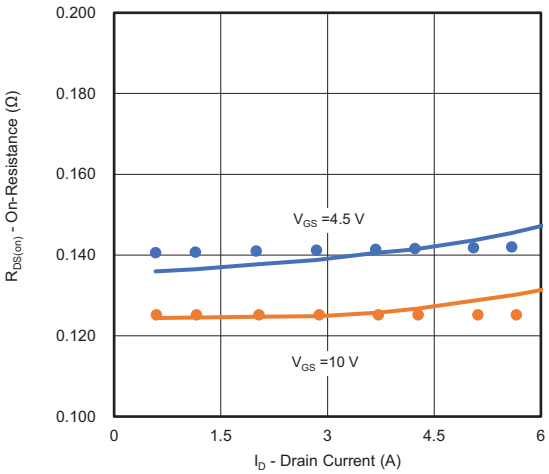
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



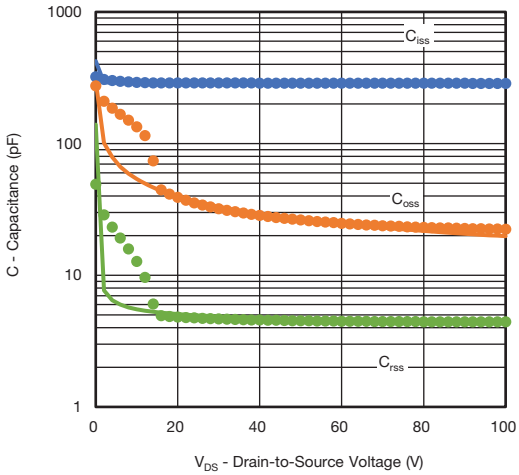
Output Characteristics



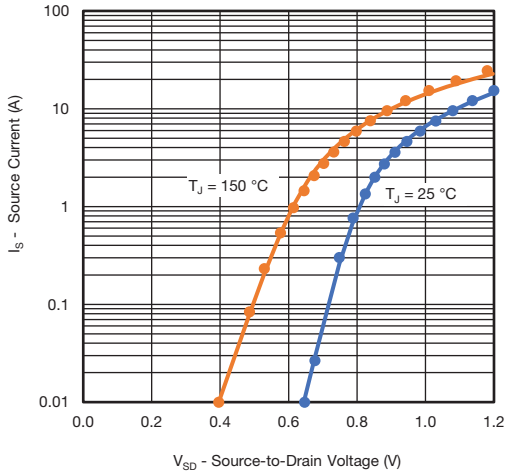
Transfer Characteristics



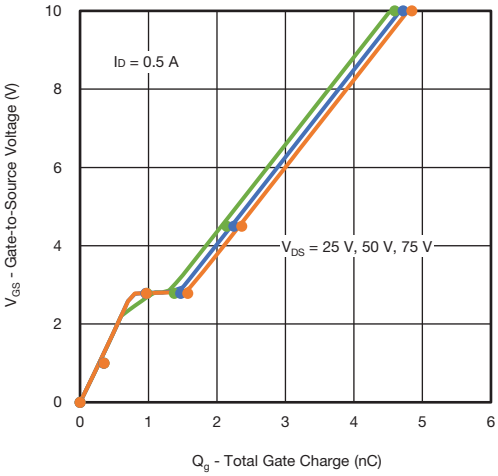
On-Resistance vs. Drain Current (A)



Capacitance



Source-Drain Diode Forward Voltage



Gate Charge