SPICE Device Model Si4534DY



Vishay Siliconix

N- and P-Channel 60 V (D-S) MOSFET

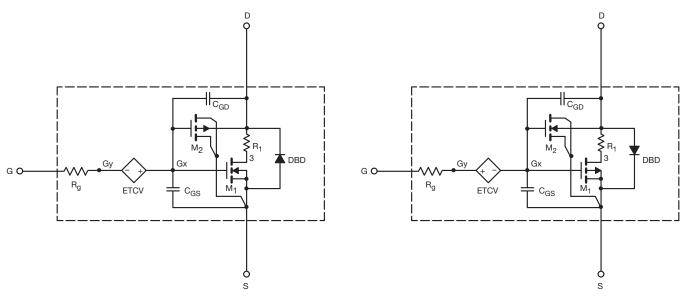
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the N- and P-Channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +150 °C temperature ranges under the pulsed -20 V to +20 V gate drive. The saturated output impedance is best fit gate bias near the threshold voltage. at the A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched Cgd model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N-and P-Channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over the -55 °C to +150 °C temperature range
- · Model the gate charge



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

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SPECIFICATIONS ($T_C = 25$	°C, unless	otherwise noted)				
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATE D DATA	MEASURE D DATA	UNIT
Static						
Gate-source threshold voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_{D}=250\;\mu A$	N-Ch	1.9	-	V
		$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	P-Ch	-2.1	-	V
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	N-Ch	0.022	0.022	Ω
		$V_{GS} = -10 \text{ V}, \text{ I}_{D} = -3.1 \text{ A}$	P-Ch	0.090	0.100	
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	N-Ch	0.033	0.029	
		$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = 3.1 \text{ A}$	P-Ch	0.130	0.126	
Forward transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 10 \text{ A}$	N-Ch	21	23	S
		V _{DS} = -15 V, I _D = -3.1 A	P-Ch	7.8	8.5	
Dynamic ^b	•	·				
Input capacitance	C _{iss}	N-Channel V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	421	420	pF
			P-Ch	621	650	
Output capacitance	C _{oss}		N-Ch	91	92	
		P-Channel	P-Ch	98	95	
Reverse transfer capacitance	C _{rss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ N-Ch 4	4	4		
			P-Ch 59	60		
Total gate charge	Qg	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	N-Ch	7.3	7.1	nC
		$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -3.1 \text{ A}$	P-Ch	14.2	14.5	
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	N-Ch	3.3	3.3	
		$V_{DS} = -30 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.1 \text{ A}$	P-Ch	7	8	
Gate-source charge	Q _{gs}	N-Channel	N-Ch	1.4	1.7	
Gate-source charge	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	P-Ch	2.5	2.2	
Gate-drain charge	Q _{gd}	P-Channel	N-Ch	0.8	0.9	
Gate-drain charge	Q _{qd}	$V_{DS} = -30 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.1 \text{ A}$	P-Ch	3.0	3.7	
Drain-source body diode character	istics					
Body diode voltage	V _{SD}	I _S = 2 A	N-Ch	0.8	0.8	v
Body diode voltage		I _S = -2 A	P-Ch	-0.79	-0.8	
Body diode reverse recovery time	t _{rr}	N-Channel	N-Ch	14	14	ns
Body diode reverse recovery time			P-Ch	26	30	
Body diode reverse recovery charge	Q _{rr}	$I_F = 5 A$ di/dt = 100 A/µs, T _J = 25 °C	N-Ch	5	10	nC
Body diode reverse recovery charge			P-Ch	25	35	
Reverse recovery fall time	t _a	P-Channel I _F = -2 A di/dt = 100 A/µs, T _J = 25 °C	N-Ch	8	8	ns
Reverse recovery fall time			P-Ch	19	16	
Reverse recovery rise time	t _b		N-Ch	6	6	
Reverse recovery rise time			P-Ch	7	14	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

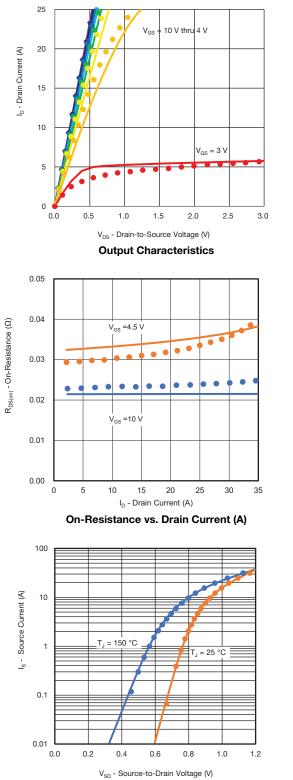
b. Guaranteed by design, not subject to production testing

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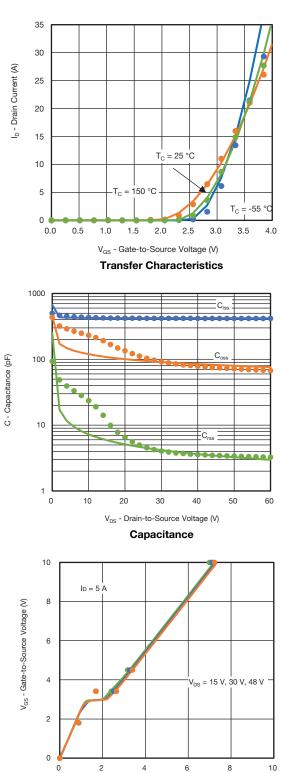


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COMPARISON OF MODEL WITH MEASURED DATA (N-CHANNEL) (T_J = 25 °C, unless otherwise noted)



Source-Drain Diode Forward Voltage



-

Q_a - Total Gate Charge (nC)

Gate Charge

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T_C = 25 °C

T_C = -55 °C

4

5

6

T_C = 150 °C

2

1

3

V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics

С

30

Capacitance

V_{DS} - Drain-to-Source Voltage (V)

.

9

Q_a - Total Gate Charge (nC)

Gate Charge

V_{DS} = 30 V

12

40

50

60

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COMPARISON OF MODEL WITH MEASURED DATA (P-CHANNEL) (T_J = 25 °C, unless otherwise noted)

25

20

15

10

5

0

0

1000

100

10

10

8

6

4

2

0

0

V_{GS} - Gate-to-Source Voltage (V)

0

10

ID = 3.1 A

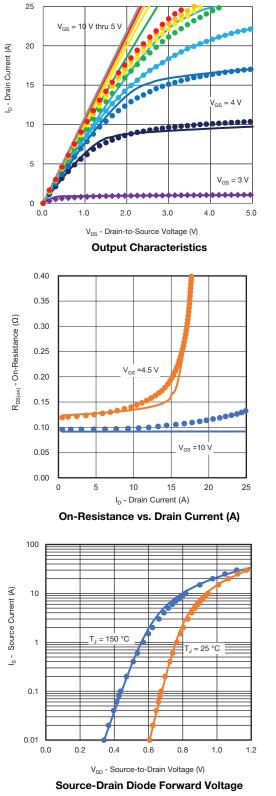
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6

20

C - Capacitance (pF)

I_D - Drain Current (A)



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S23-0438-Rev. A, 12-Jun-2023

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