# N- and P-Channel 60 V (D-S) MOSFET

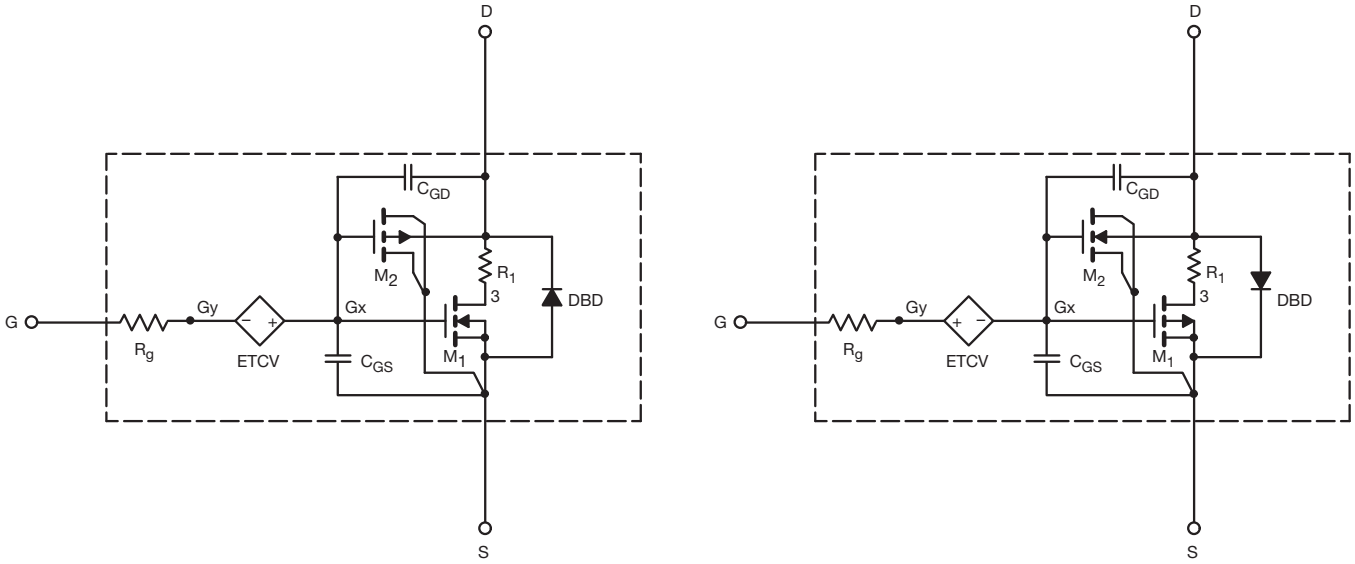
## DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the N- and P-Channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +150 °C temperature ranges under the pulsed -20 V to +20 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## CHARACTERISTICS

- N-and P-Channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +150 °C temperature range
- Model the gate charge

## SUBCIRCUIT MODEL SCHEMATIC




**Note**

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

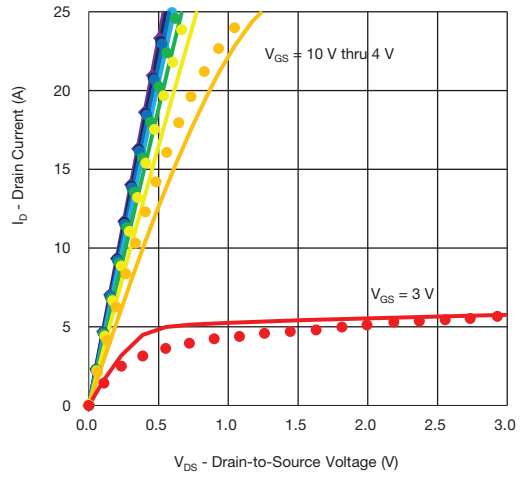
| **SPECIFICATIONS** ($T_C$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **SIMULATED DATA** | **MEASURED DATA** | **UNIT** |
| **Static** | | | | | | |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | N-Ch | 1.9 | - | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | P-Ch | -2.1 | - | V |
| Drain-source on-state resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 5 A | N-Ch | 0.022 | 0.022 | Ω |
| | | $V_{GS}$ = -10 V, $I_D$ = -3.1 A | P-Ch | 0.090 | 0.100 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 4 A | N-Ch | 0.033 | 0.029 | |
| | | $V_{GS}$ = -4.5 V, $I_D$ = 3.1 A | P-Ch | 0.130 | 0.126 | |
| Forward transconductance [a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 10 A | N-Ch | 21 | 23 | S |
| | | $V_{DS}$ = -15 V, $I_D$ = -3.1 A | P-Ch | 7.8 | 8.5 | |
| **Dynamic [b]** | | | | | | |
| Input capacitance | $C_{iss}$ | N-Channel $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, f = 1 MHz<br>P-Channel $V_{DS}$ = -15 V, $V_{GS}$ = 0 V, f = 1 MHz | N-Ch | 421 | 420 | pF |
| | | | P-Ch | 621 | 650 | |
| Output capacitance | $C_{oss}$ | | N-Ch | 91 | 92 | |
| | | | P-Ch | 98 | 95 | |
| Reverse transfer capacitance | $C_{rss}$ | | N-Ch | 4 | 4 | |
| | | | P-Ch | 59 | 60 | |
| Total gate charge | $Q_g$ | $V_{DS}$ = 30 V, $V_{GS}$ = 10 V, $I_D$ = 5 A | N-Ch | 7.3 | 7.1 | nC |
| | | $V_{DS}$ = -30 V, $V_{GS}$ = -10 V, $I_D$ = -3.1 A | P-Ch | 14.2 | 14.5 | |
| | | $V_{DS}$ = 30 V, $V_{GS}$ = 4.5 V, $I_D$ = 5 A | N-Ch | 3.3 | 3.3 | |
| | | $V_{DS}$ = -30 V, $V_{GS}$ = -4.5 V, $I_D$ = -3.1 A | P-Ch | 7 | 8 | |
| Gate-source charge | $Q_{gs}$ | N-Channel $V_{DS}$ = 30 V, $V_{GS}$ = 4.5 V, $I_D$ = 5 A<br>P-Channel $V_{DS}$ = -30 V, $V_{GS}$ = -4.5 V, $I_D$ = -3.1 A | N-Ch | 1.4 | 1.7 | |
| Gate-source charge | $Q_{gs}$ | | P-Ch | 2.5 | 2.2 | |
| Gate-drain charge | $Q_{gd}$ | | N-Ch | 0.8 | 0.9 | |
| Gate-drain charge | $Q_{gd}$ | | P-Ch | 3.0 | 3.7 | |
| **Drain-source body diode characteristics** | | | | | | |
| Body diode voltage | $V_{SD}$ | $I_S$ = 2 A | N-Ch | 0.8 | 0.8 | V |
| Body diode voltage | | $I_S$ = -2 A | P-Ch | -0.79 | -0.8 | |
| Body diode reverse recovery time | $t_{rr}$ | N-Channel $I_F$ = 5 A di/dt = 100 A/µs, $T_J$ = 25 °C<br>P-Channel $I_F$ = -2 A di/dt = 100 A/µs, $T_J$ = 25 °C | N-Ch | 14 | 14 | ns |
| Body diode reverse recovery time | | | P-Ch | 26 | 30 | |
| Body diode reverse recovery charge | $Q_{rr}$ | | N-Ch | 5 | 10 | nC |
| Body diode reverse recovery charge | | | P-Ch | 25 | 35 | |
| Reverse recovery fall time | $t_a$ | | N-Ch | 8 | 8 | ns |
| Reverse recovery fall time | | | P-Ch | 19 | 16 | |
| Reverse recovery rise time | $t_b$ | | N-Ch | 6 | 6 | |
| Reverse recovery rise time | | | P-Ch | 7 | 14 | |

**Notes**

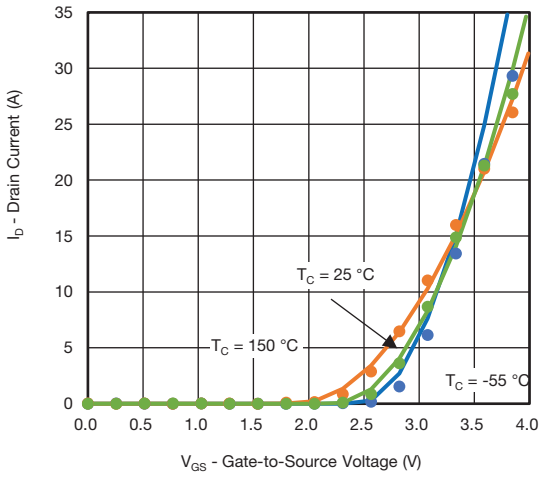
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

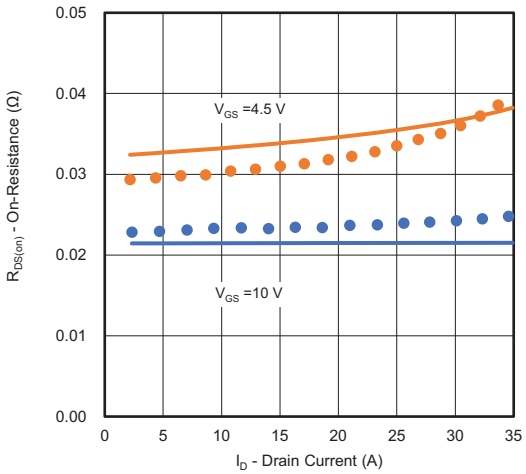
## COMPARISON OF MODEL WITH MEASURED DATA (N-CHANNEL) ($T_J$ = 25 °C, unless otherwise noted)



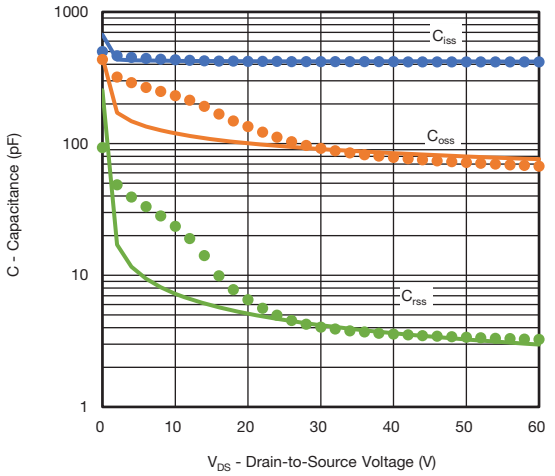

**Output Characteristics**



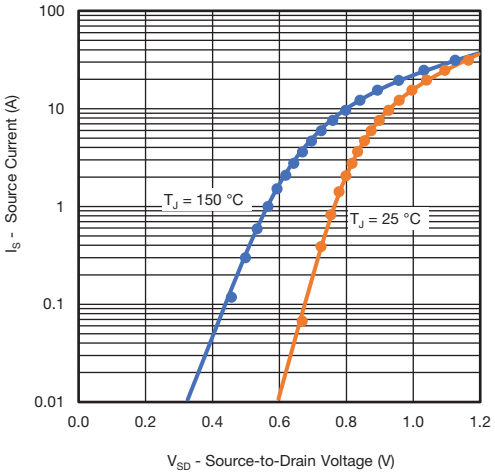

**Transfer Characteristics**



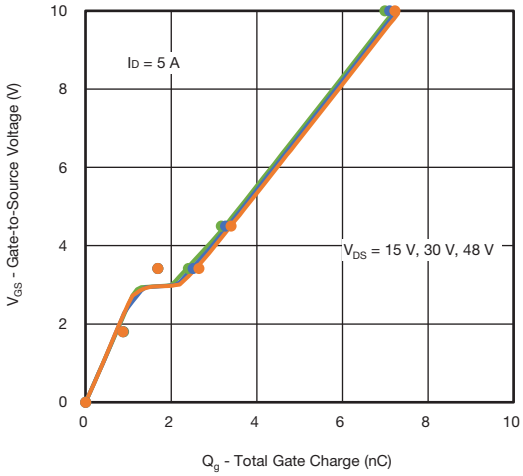

**On-Resistance vs. Drain Current (A)**




**Capacitance**

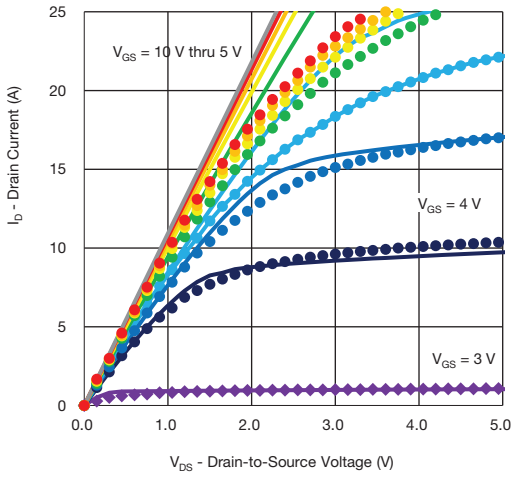



**Source-Drain Diode Forward Voltage**

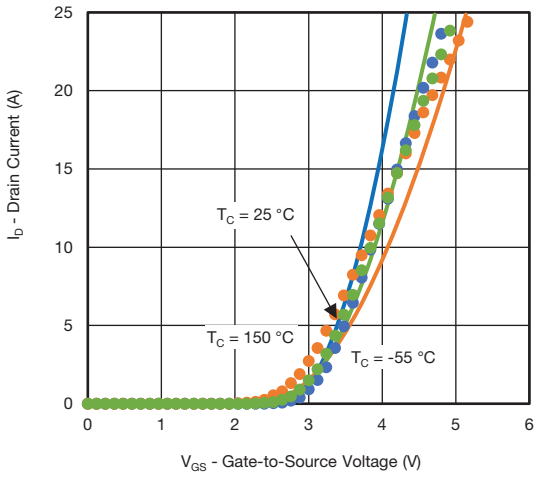



**Gate Charge**

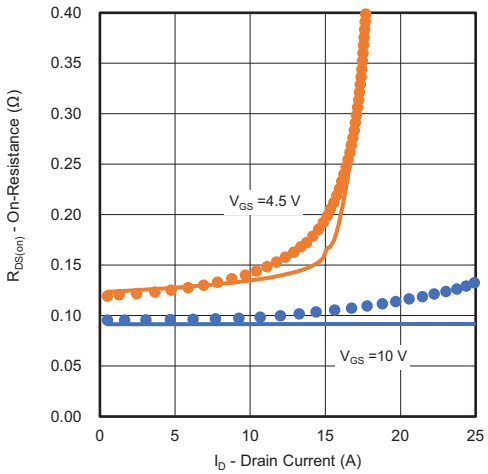
## COMPARISON OF MODEL WITH MEASURED DATA (P-CHANNEL) ($T_J$ = 25 °C, unless otherwise noted)



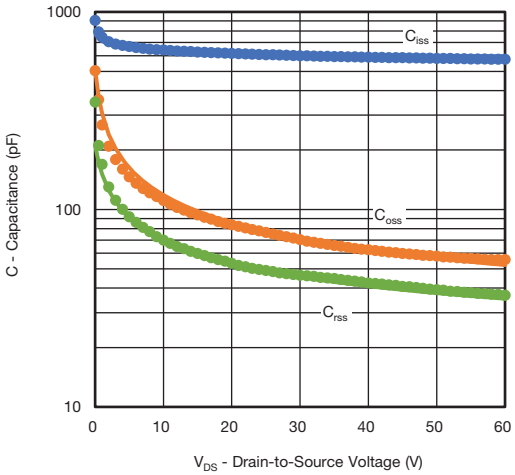

**Output Characteristics**



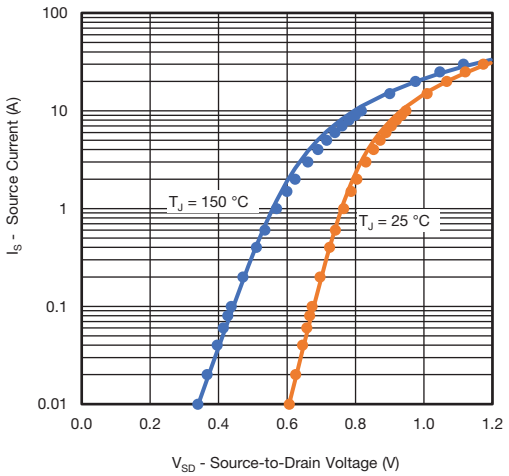

**Transfer Characteristics**



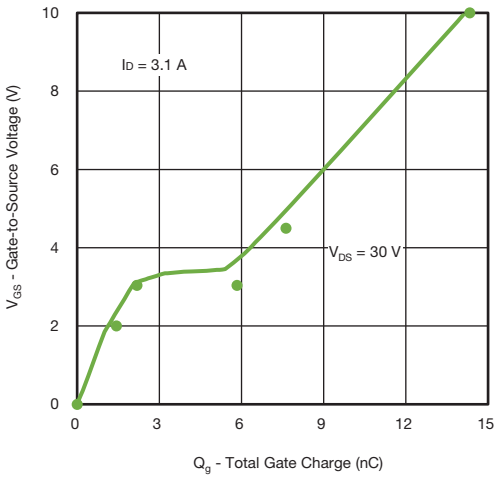

**On-Resistance vs. Drain Current (A)**




**Capacitance**




**Source-Drain Diode Forward Voltage**




**Gate Charge**