

## N-Channel 100 V (D-S) MOSFET

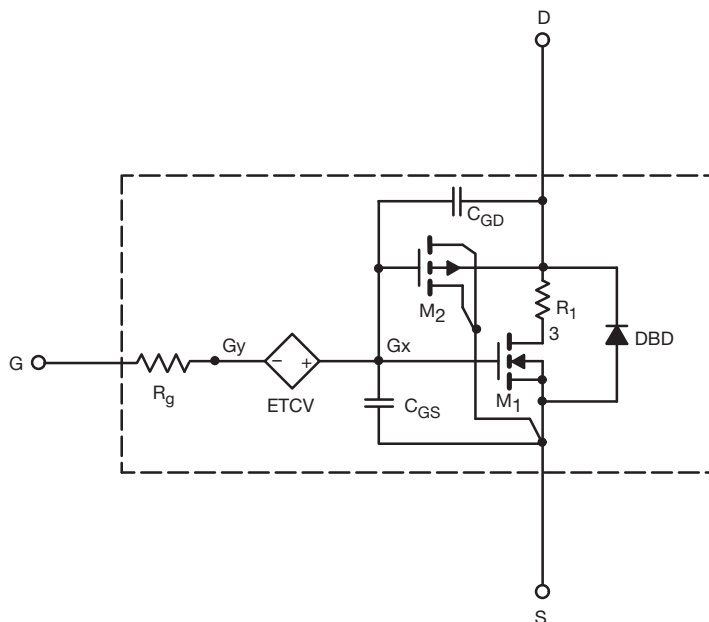
### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the N-Channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +150 °C temperature ranges under the pulsed -20 V to +20 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +150 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



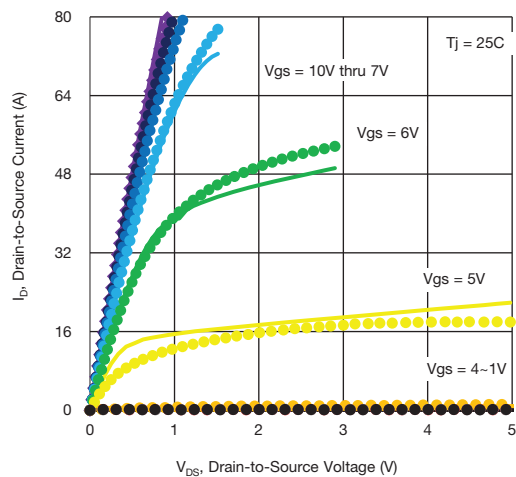
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.93	-	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	0.0100	0.0103	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 10 A	0.0120	0.0123	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	27	25	S
Dynamic <sup>b</sup>					
Input capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	964	920	pF
Output capacitance	C <sub>oss</sub>		254	370	
Reverse transfer capacitance	C <sub>rss</sub>		7.5	8.2	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	12.7	12.8	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 10 A	9.7	9.7	
Gate-drain charge	Q <sub>gd</sub>		4	4.9	
			1.6	1.4	
Drain-source body diode characteristics					
Body diode voltage	V <sub>SD</sub>	I <sub>F</sub> = 5 A, V <sub>GS</sub> = 0 V	0.77	0.77	V

**Notes**

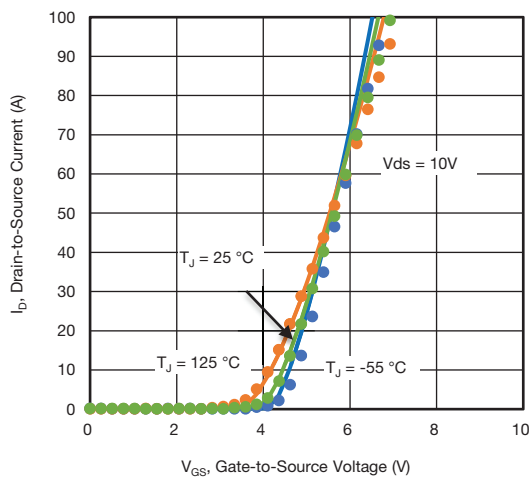
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing



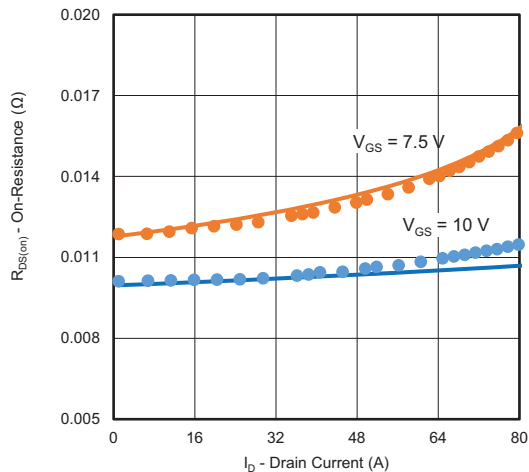
## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)



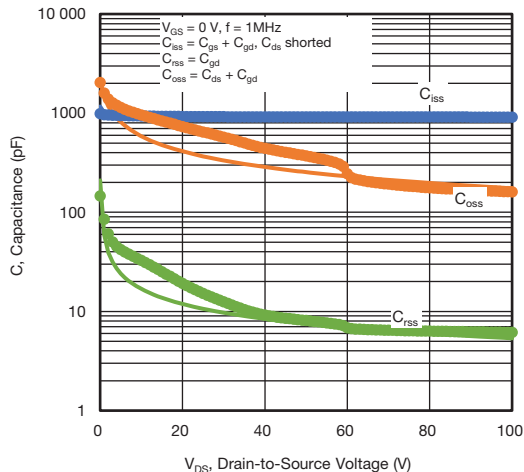
Output Characteristics



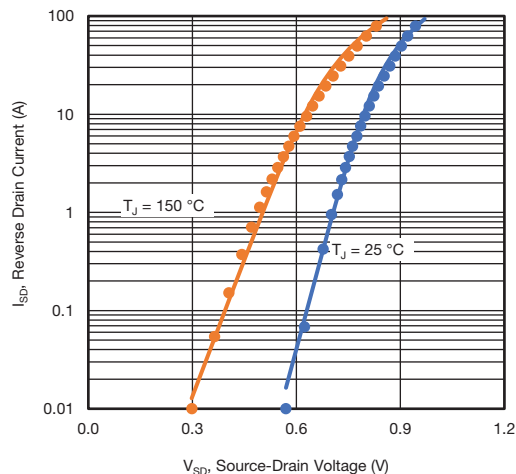
Transfer Characteristics



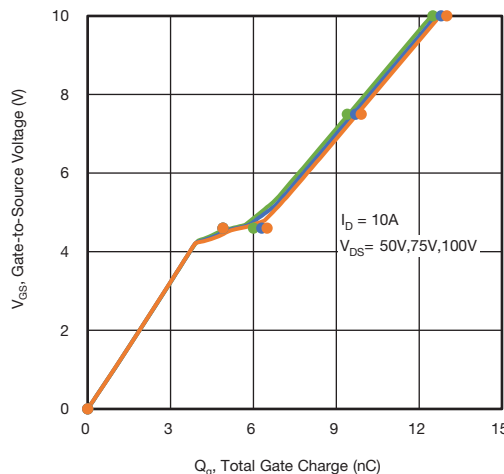
On-Resistance vs. Drain Current (A)



Capacitance



Source-Drain Diode Forward Voltage



Gate Charge