

N-Channel 100 V (D-S) MOSFET

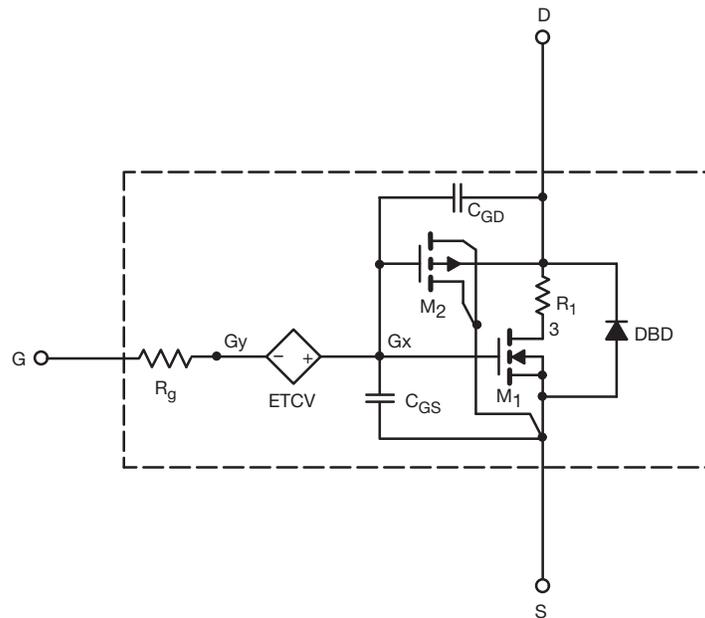
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the N-Channel vertical DMOS. The subcircuit model is extracted and optimized over the $-55\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$ temperature ranges under the pulsed -20 V to $+20\text{ V}$ gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the $-55\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$ temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



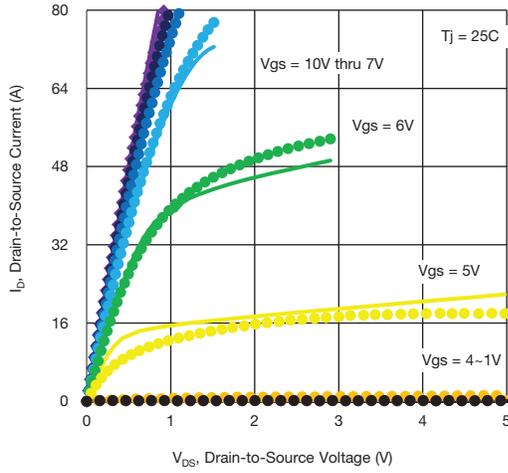
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.93	-	V
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	0.0100	0.0103	Ω
		V _{GS} = 7.5 V, I _D = 10 A	0.0120	0.0123	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A	27	25	S
Dynamic ^b					
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	964	920	pF
Output capacitance	C _{oss}		254	370	
Reverse transfer capacitance	C _{rss}		7.5	8.2	
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A	12.7	12.8	nC
			9.7	9.7	
Gate-source charge	Q _{gs}	V _{DS} = 50 V, V _{GS} = 7.5 V, I _D = 10 A	4	4.9	
Gate-drain charge	Q _{gd}		1.6	1.4	
Drain-source body diode characteristics					
Body diode voltage	V _{SD}	I _F = 5 A, V _{GS} = 0 V	0.77	0.77	V

Notes

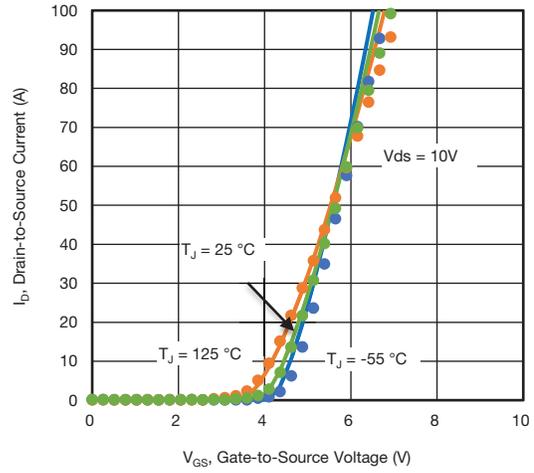
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing



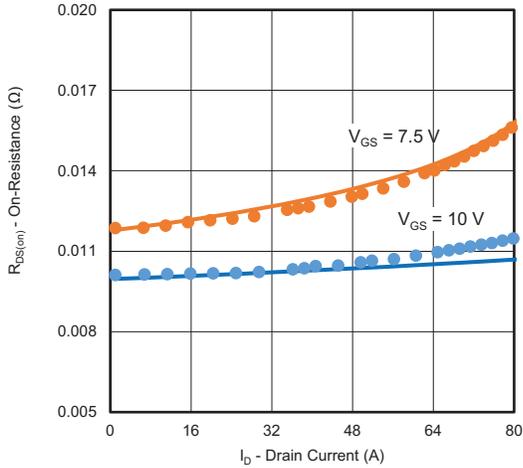
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



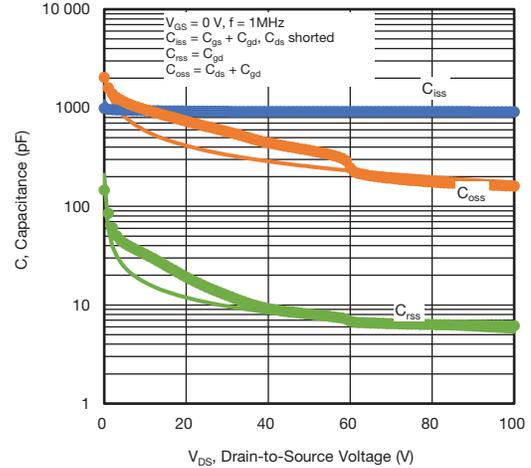
Output Characteristics



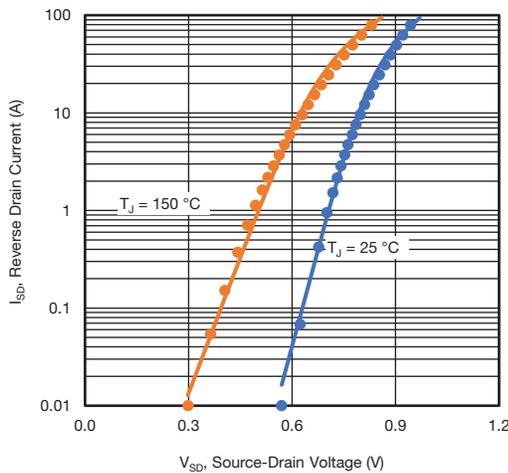
Transfer Characteristics



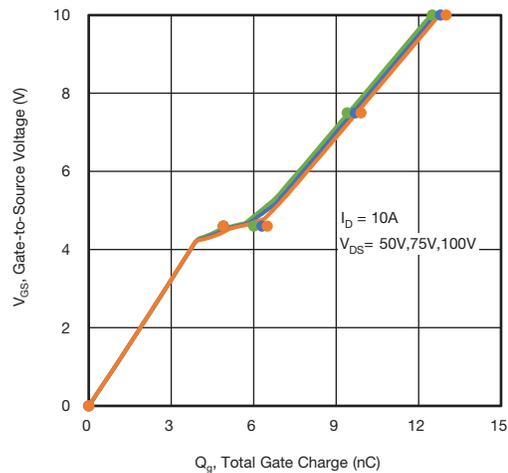
On-Resistance vs. Drain Current (A)



Capacitance



Source-Drain Diode Forward Voltage



Gate Charge

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