Dual N-Channel 30 V (D-S) MOSFET

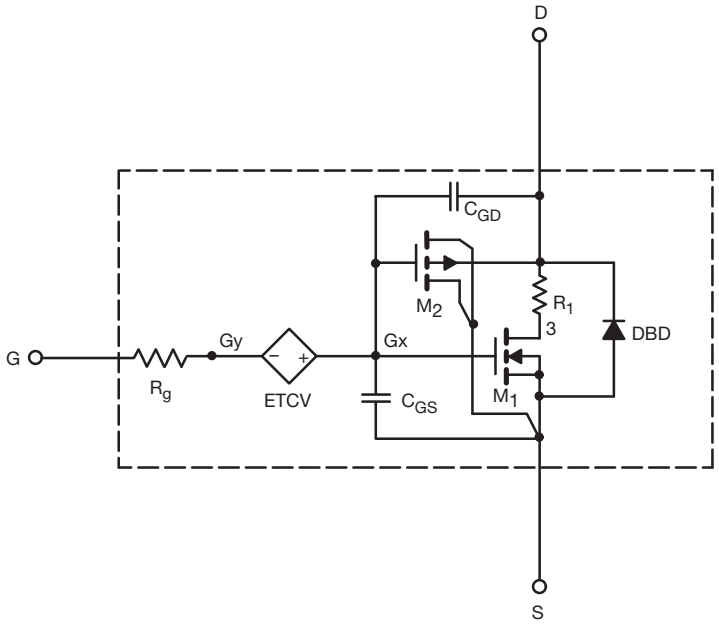
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the N-Channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +150 °C temperature ranges under the pulsed -12 V to +16 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +150 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

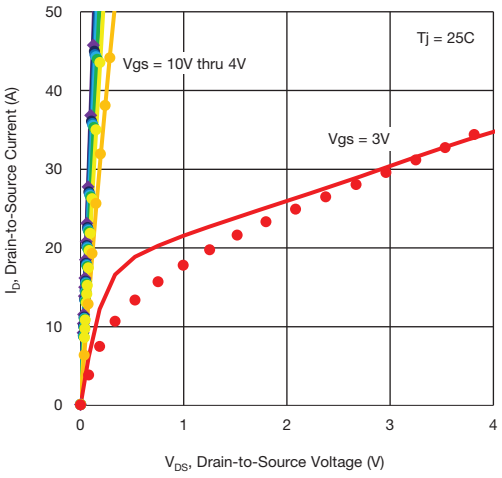
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.55	1.5	V
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	0.0026	0.0027	Ω
		V_{GS} = 4.5 V, I_D = 7 A	0.0048	0.0044	
		V_{GS} = 10 V, I_D = 10 A, T_J = 150 °C	0.0038	-	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 10 A	75	57	S
Dynamic [b]					
Input capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	975	1030	pF
Output capacitance	C_{oss}		356	340	
Reverse transfer capacitance	C_{rss}		30	30	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	14.9	14.8	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	6.9	6.7	
Gate-source charge	Q_{gs}		3.2	3.8	
Gate-drain charge	Q_{gd}		1.6	1.12	
Drain-source body diode characteristics					
Body diode voltage	V_{SD}	I_F = 15 A, V_{GS} = 0 V	0.81	0.85	V

Notes

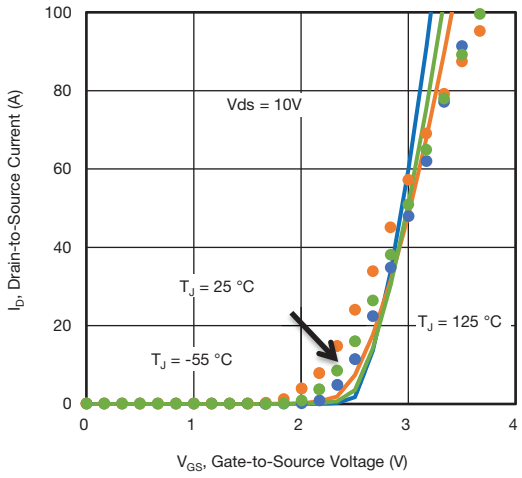
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

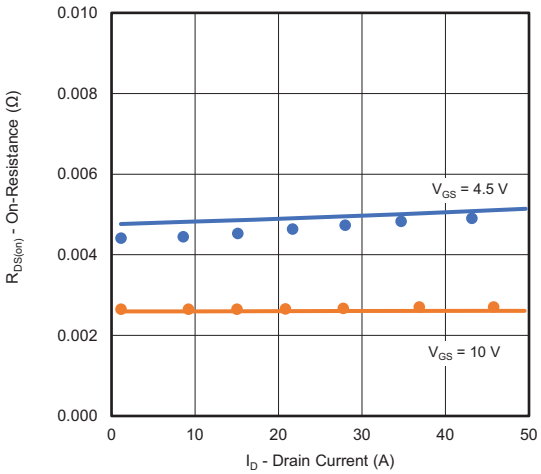
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



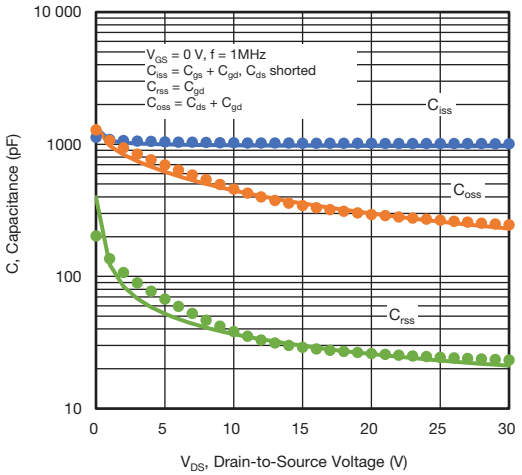
Output Characteristics



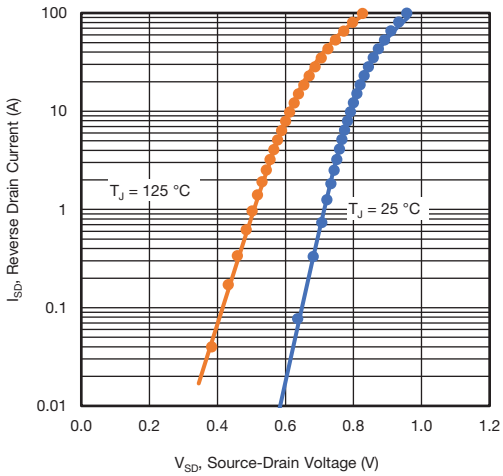
Transfer Characteristics



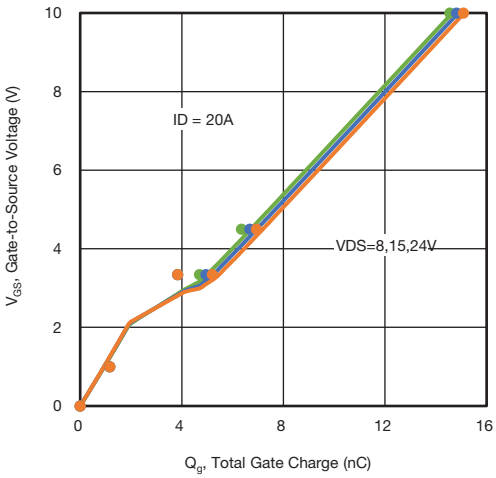
On-Resistance vs. Drain Current (A)



Capacitance



Source-Drain Diode Forward Voltage



Gate Charge