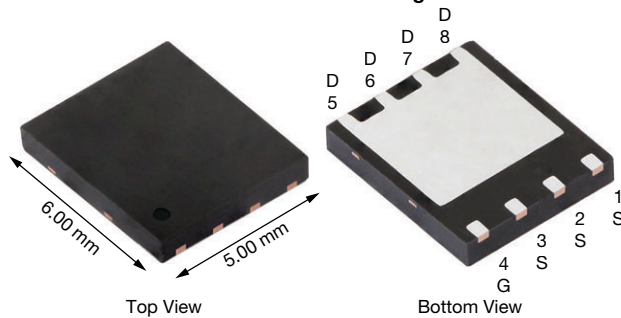


## N-Channel 150 V (D-S) MOSFET

**PowerPAK® SO-8S Single**


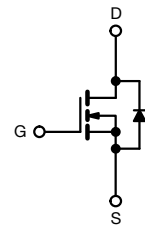
### FEATURES

- TrenchFET® Gen V power MOSFET
- Very low  $R_{DS(on)}$   $\times$   $Q_g$  figure-of-merit (FOM)
- Leadership  $R_{DS(on)}$  minimizes power loss from conduction
- 100 %  $R_g$  and UIS tested
- Enhance power dissipation and lower  $R_{thJC}$
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- DC/DC converters
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	150
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0072
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0078
$Q_g$ typ. (nC)	44
$I_D$ (A) <sup>a</sup>	119
Configuration	Single

### ORDERING INFORMATION

Package	PowerPAK SO-8S
Lead (Pb)-free and halogen-free	SiRS5702DP-T1-RE3

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	150	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	119
		$T_C = 70$ °C	95
		$T_A = 25$ °C	21 <sup>b, c</sup>
		$T_A = 70$ °C	17 <sup>b, c</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	250	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	223
		$T_A = 25$ °C	6.7 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	34	
Single pulse avalanche energy	$E_{AS}$	58	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	245
		$T_C = 70$ °C	157
		$T_A = 25$ °C	7.4 <sup>b, c</sup>
		$T_A = 70$ °C	4.7 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>		260	

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	11	17	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	0.34	0.51	

#### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 50 °C/W



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	104	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-7.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	10	
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	0.0060	0.0072	$\Omega$
		$V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$	-	0.0063	0.0078	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}$	-	111	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	4540	-	pF
Output capacitance	$C_{oss}$		-	405	-	
Reverse transfer capacitance	$C_{rss}$		-	9.1	-	
Total gate charge	$Q_g$	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	58	87	nC
		$V_{DS} = 75\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$	-	44	66	
Gate-source charge	$Q_{gs}$	$V_{DS} = 75\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$	-	22	-	
Gate-drain charge	$Q_{gd}$		-	5.1	-	
Output charge	$Q_{oss}$		$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}$	-	132	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.24	1.2	2.4	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 7.5\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	20	40	ns
Rise time	$t_r$		-	11	25	
Turn-off delay time	$t_{d(off)}$		-	35	70	
Fall time	$t_f$		-	20	40	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 7.5\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 7.5\text{ V}, R_g = 1\text{ }\Omega$	-	22	45	
Rise time	$t_r$		-	15	30	
Turn-off delay time	$t_{d(off)}$		-	31	60	
Fall time	$t_f$		-	20	40	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	223	A
Pulse diode forward current	$I_{SM}$		-	-	250	
Body diode voltage	$V_{SD}$	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$	-	0.75	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	85	170	ns
Body diode reverse recovery charge	$Q_{rr}$		-	280	560	nC
Reverse recovery fall time	$t_a$		-	61	-	ns
Reverse recovery rise time	$t_b$		-	24	-	

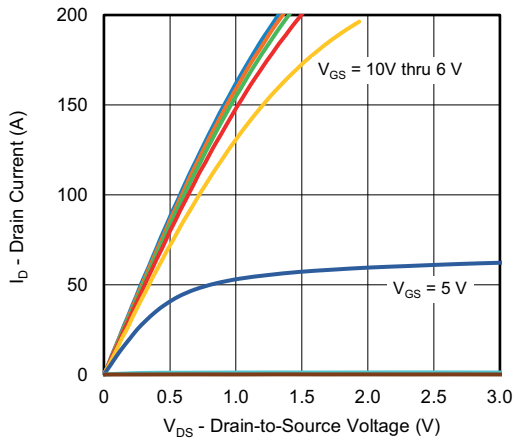
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

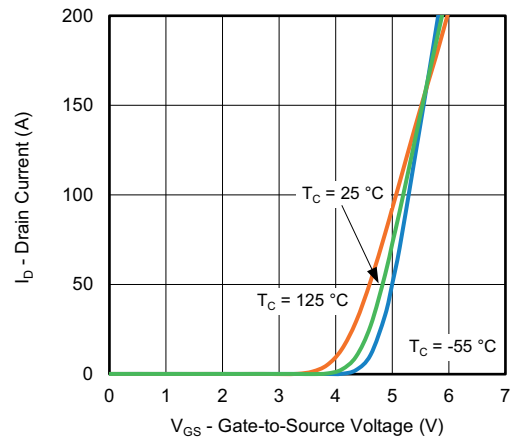
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



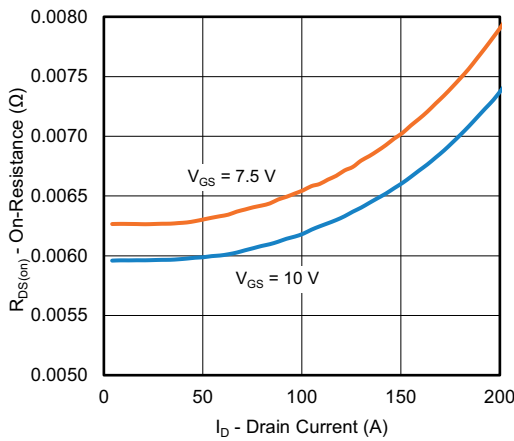
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



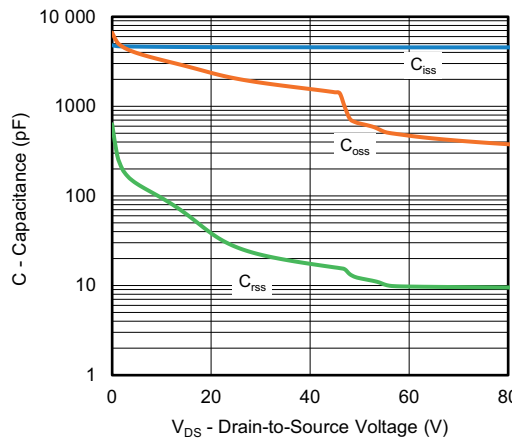
Output Characteristics



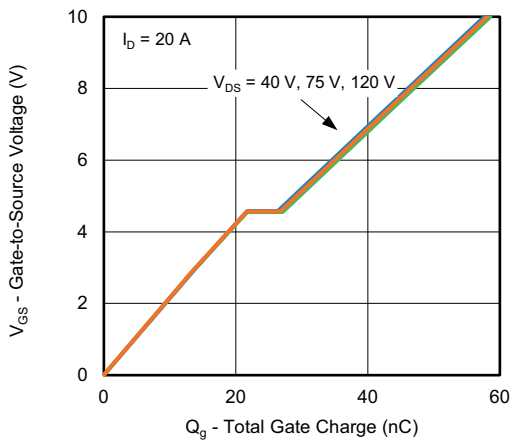
Transfer Characteristics



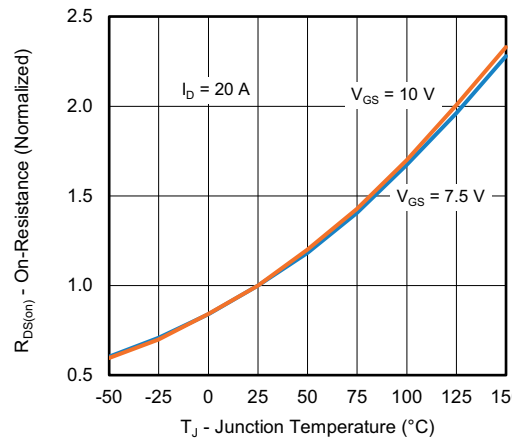
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



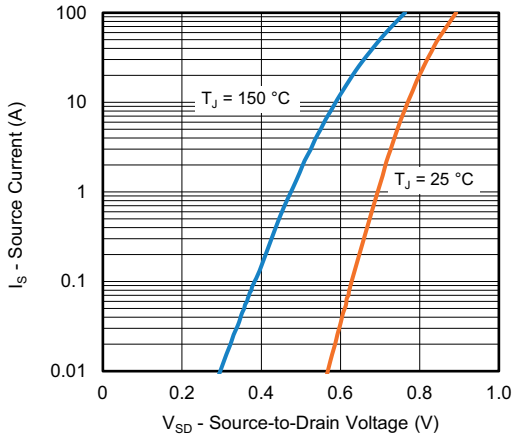
Gate Charge



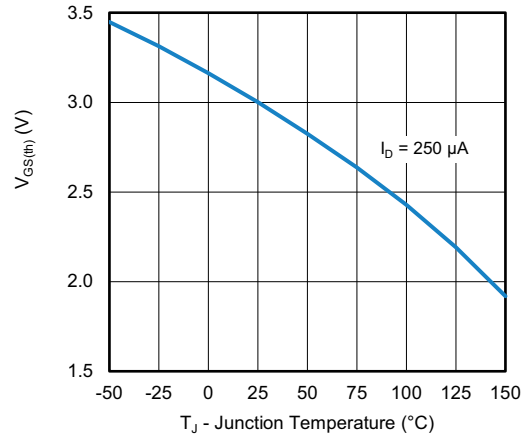
On-Resistance vs. Junction Temperature



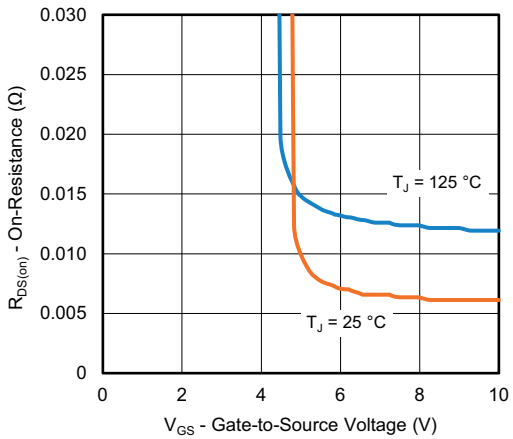
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



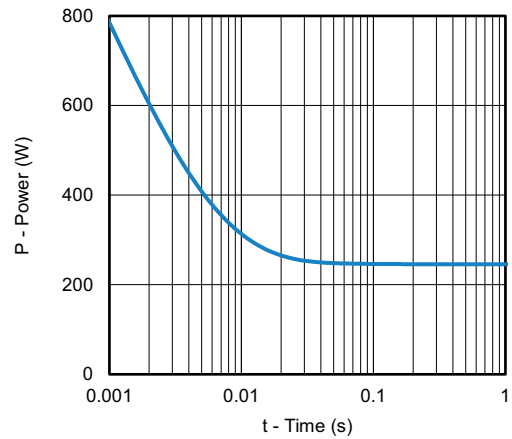
Source-Drain Diode Forward Voltage



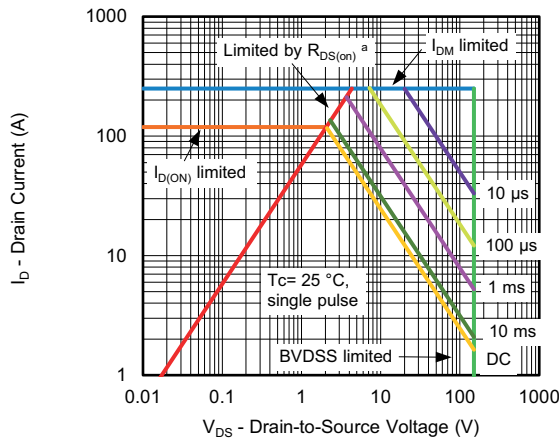
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



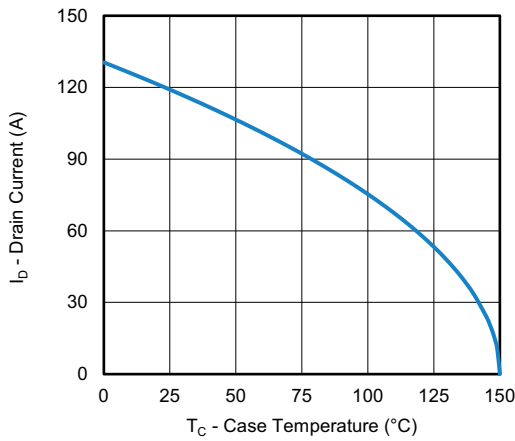
Safe Operating Area, Junction-to-Case

Note

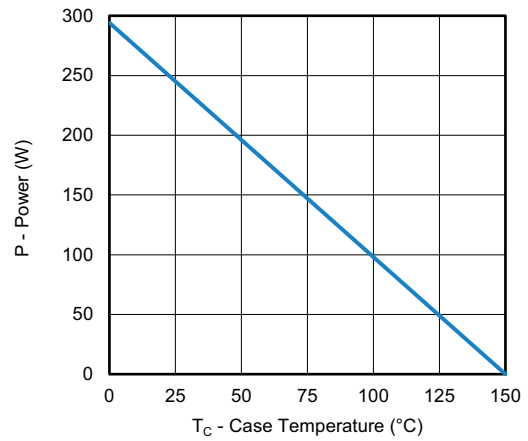
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



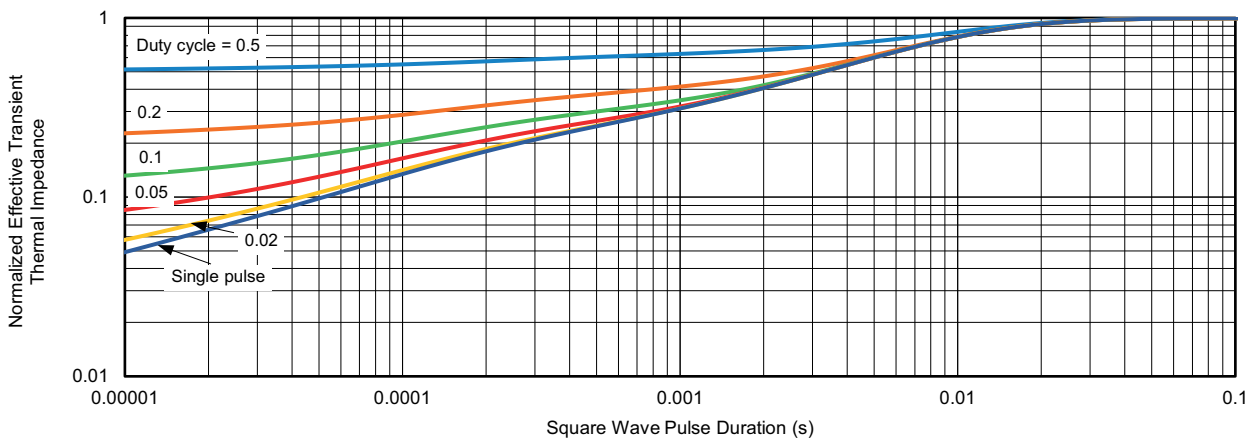
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating <sup>a</sup>



Power, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- a. The power dissipation  $P_D$  is based on  $T_J \text{ max.} = 150 \text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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