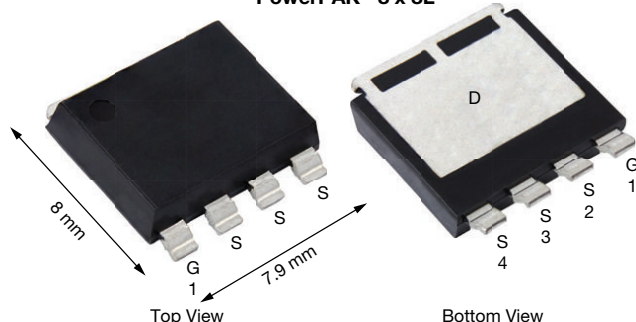


# Automotive P-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8L

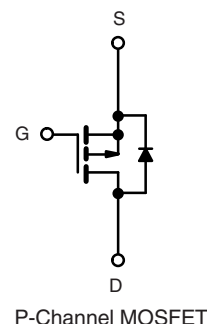


## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



PRODUCT SUMMARY	
$V_{DS}$ (V)	-80
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -10$ V	0.0055
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.0077
$I_D$ (A) <sup>g</sup>	-175
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and Halogen-free	SQJQ181EL

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	-80	V
Gate-source voltage <sup>a</sup>		$V_{GS}$	$\pm 20$	
Continuous drain current <sup>g</sup>	$T_C = 25$ °C <sup>b</sup>	$I_D$	-175	A
	$T_C = 125$ °C		-101	
Continuous source current (diode conduction) <sup>b, g</sup>		$I_S$	-317	
Pulsed drain current <sup>c, g</sup>		$I_{DM}$	-619	
Single pulse avalanche current		$I_{AS}$	-78	
Single pulse avalanche energy		$E_{AS}$	305	mJ
Maximum power dissipation <sup>c, g</sup>	$T_C = 25$ °C	$P_D$	348	W
	$T_C = 125$ °C		116	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>e</sup>	$R_{thJA}$	42	°C/W
Junction-to-case (drain) <sup>f</sup>		$R_{thJC}$	0.43	

## Notes

- Not intended for continuous use with positive gate voltage  $> 5.0$  V
- Package limited
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). For PowerPAK SO-8L, the end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- Using thermal characterization methods based on JESD51-14
- Values based on  $R_{thJC}$  and  $T_C$  of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

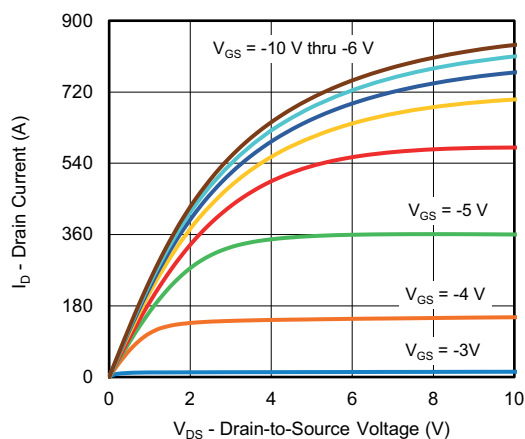
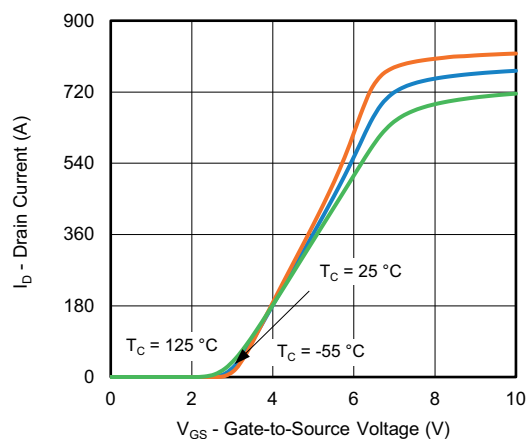
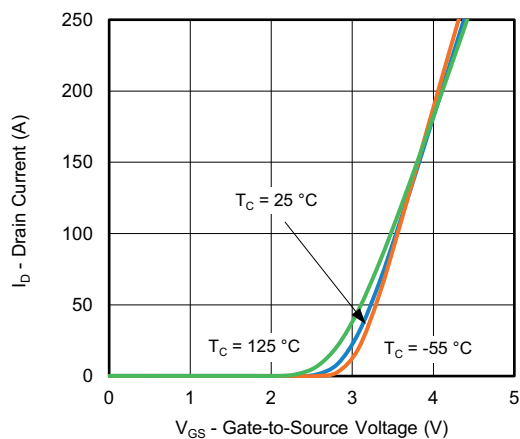
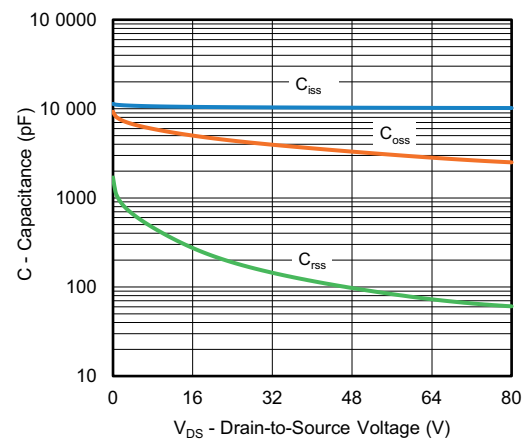
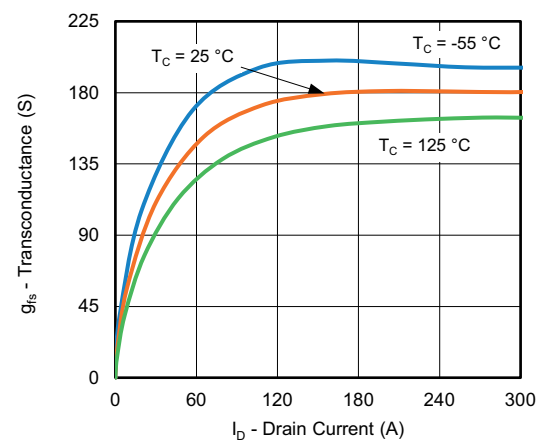
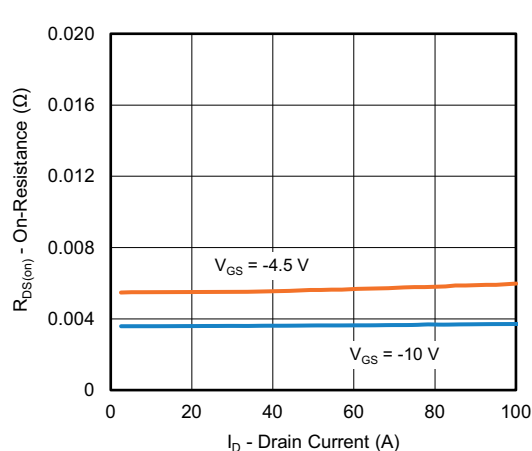


SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = -250 μA		-80	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		-1.5	-2.0	-2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -80 V	-	-	-1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -80 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -80 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> ≥ -5 V	-30	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A	-	0.0046	0.0055	Ω
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 125 °C	-	-	0.0098	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 175 °C	-	-	0.0120	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -8 A	-	0.0063	0.0075	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -30 A		-	110	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -25 V, f = 1 MHz	-	10 343	14 481	pF
Output capacitance	C <sub>oss</sub>			-	4135	4789	
Reverse transfer capacitance	C <sub>rss</sub>			-	196	275	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -40 V, I <sub>D</sub> = -50 A	-	153	230	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	39	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	20	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.8	1.8	3.2	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -40 V, R <sub>L</sub> = 4 Ω, I <sub>D</sub> ≅ -10 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω		-	19	29	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	11	17	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	80	120	
Fall time <sup>c</sup>	t <sub>f</sub>			-	21	32	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-619	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -10 A, V <sub>GS</sub> = 0 V		-	-0.76	-1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -40 A, di/dt = 100 A/μs		-	105	210	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	205	410	nC
Reverse recovery fall time	t <sub>a</sub>			-	56	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	52	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-3.1	-	A

**Notes**

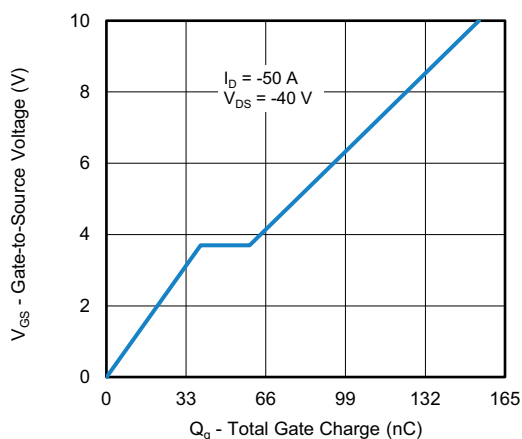
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

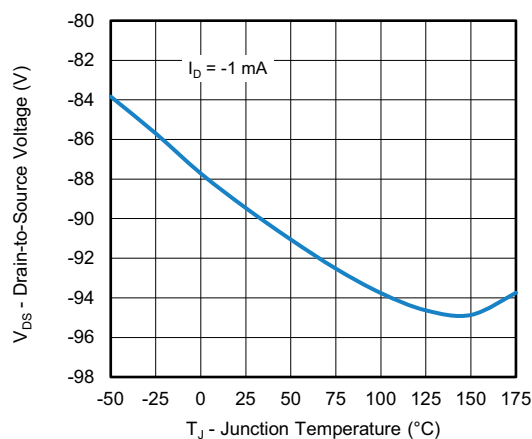
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transfer Characteristics**

**Capacitance**

**Transconductance**

**On-Resistance vs. Drain Current**



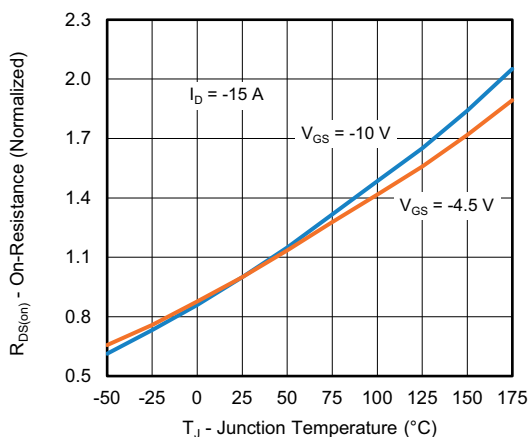
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



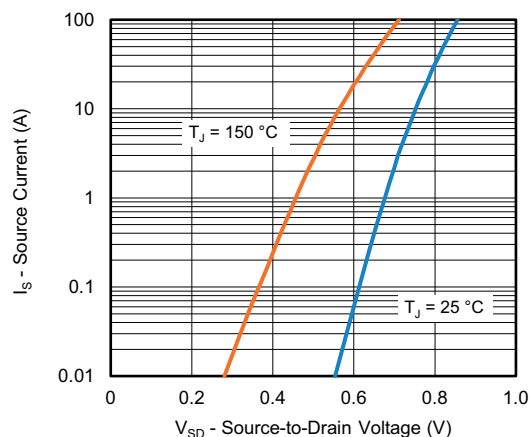
**Gate Charge**



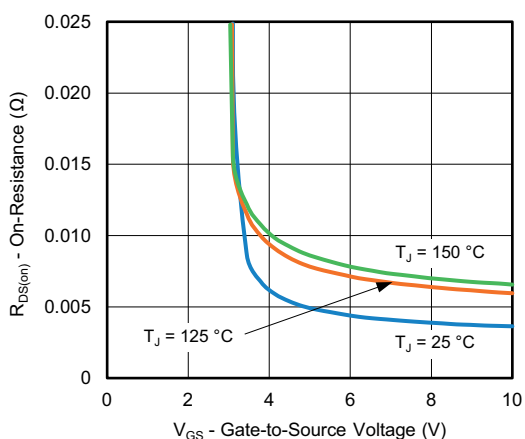
**Drain-Source Breakdown vs. Junction Temperature**



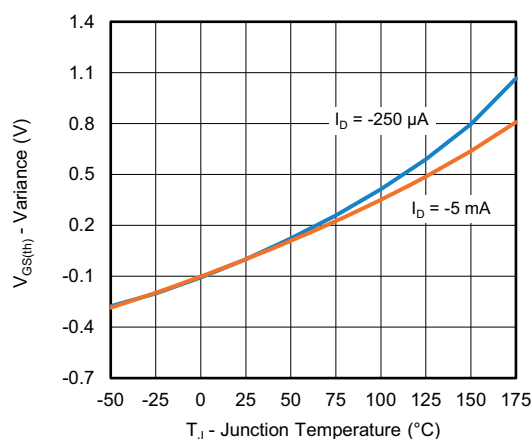
**On-Resistance vs. Junction Temperature**



**Source Drain Diode Forward Voltage**



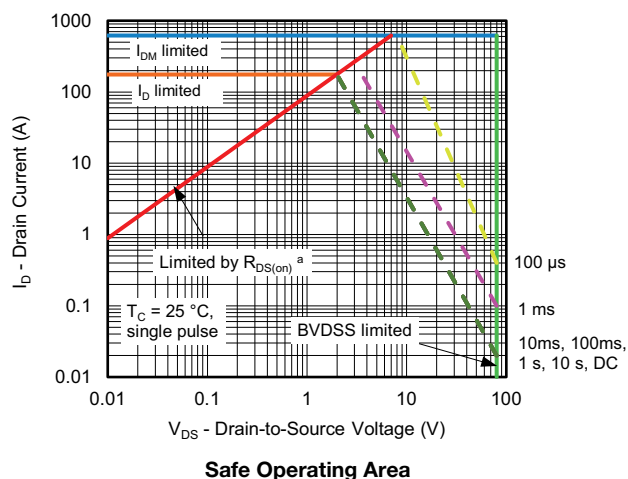
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



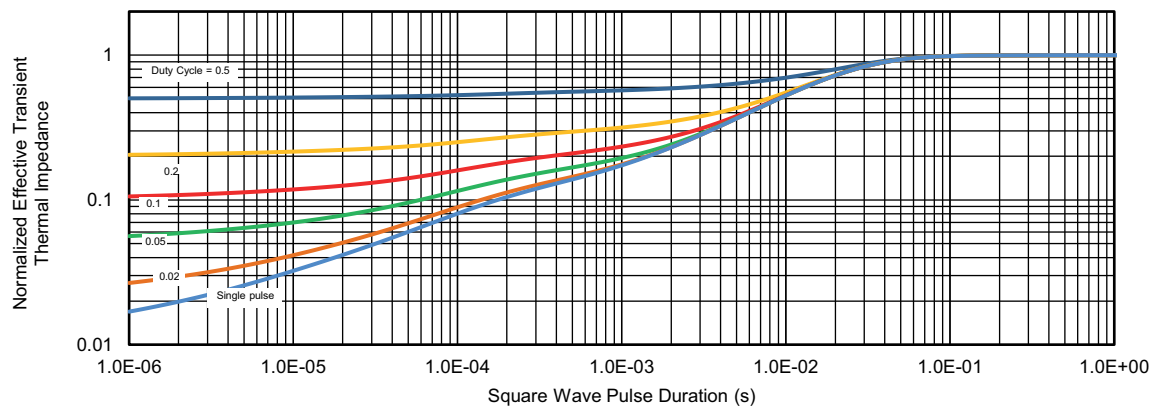
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



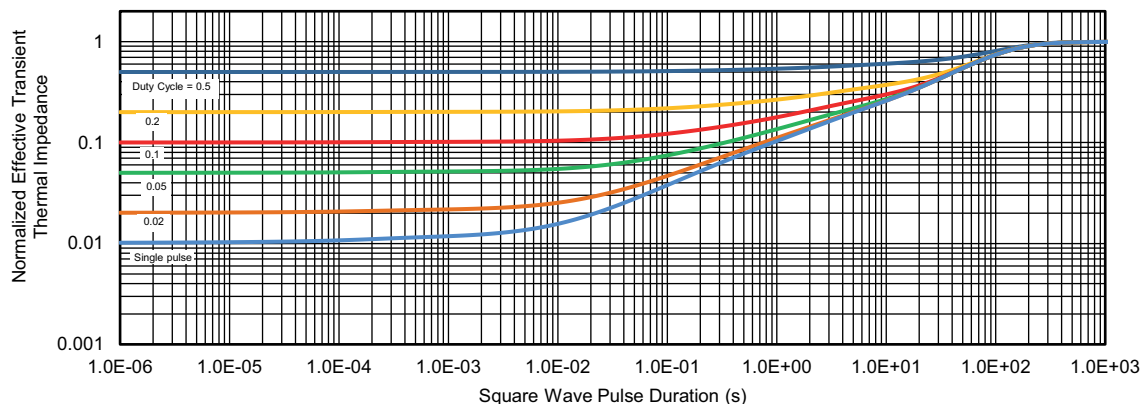
**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**THERMAL RATINGS** ( $T_C = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**



Normalized Thermal Transient Impedance, Junction-to-Ambient

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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