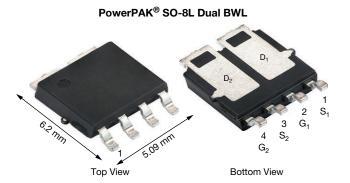
SQJ764ELP

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Vishay Siliconix

Automotive Dual N-Channel 60 V (D-S) 175 °C MOSFET

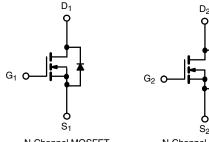


FEATURES

- TrenchFET[®] power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



PRODUCT SUMMARY V_{DS} (V) 60 $R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$ 0.0105 $R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 V$ 0.0146 I_D (A) per leg ^e 62 Configuration Dual



N-Channel MOSFET

N-Channel MOSFET

ORDERING INFORMATION				
Package	PowerPAK [®] SO-8L			
Lead (Pb)-free and halogen-free	SQJ764ELP (for detailed order number please see <u>www.vishay.com/doc?79771</u>)			

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	s ± 20		
Continuous Drain Current ^e	T _C = 25 °C a	1	62		
	T _C = 125 °C	ID	36		
Continuous Source Current (Diode conduction) ^e		IS	62	А	
Pulsed Drain Current ^{b, e}		I _{DM}	102		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	24.5		
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	30	mJ	
Maximum Power Dissipation ^{b, e}	T _C = 25 °C	$T_{\rm C} = 25 ^{\circ}{\rm C}$		W	
	T _C = 125 °C	P _D	28	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C	
Soldering Recommendations (Peak temperature)		-	260	-0	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB mount ^c	R _{thJA}	52	°C/W	
Junction-to-Case (Drain) ^d		R _{thJC}	1.74	C/W	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. When mounted on 1" square PCB (FR4 material)
c. See solder profile (www.vishay.com/doc?73257).
d. As per on JESD51-14

e. Values based on RthJC and TC of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system.

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1 For technical questions, contact: automostechsupport@vishay.com Document Number: 62453

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static					•		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = 250 \mu A$		60	-	-	v
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		1.2	2.0	2.5	v
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA
Zero Gate Voltage Drain Current		$V_{GS} = 0 V$	V _{DS} = 60 V	-	-	1	μA
	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 60 V, T _J = 125 °C	-	-	50	
		$V_{GS} = 0 V$	$V_{DS} = 60 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	150	
On-State Drain Current ^a	I _{D(on)}	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	10	-	-	Α
Drain-Source On-State Resistance ^a		$V_{GS} = 10 V$	I _D = 7 A	-	0.0088	0.0105	Ω
	P	$V_{GS} = 4.5 V$	$I_D = 7 A$	-	0.0117	0.0146	
	R _{DS(on)}	$V_{GS} = 10 V$	I _D = 7 A, T _J = 125 °C	-	-	0.0178	
		$V_{GS} = 10 V$	I _D = 7 A, T _J = 175 °C	-	-	0.0220	
Forward Transconductance b	g fs	V _{DS} = 15 V, I _D = 20 A		-	50	-	S
Dynamic ^b							
Input Capacitance	C _{iss}		V _{DS} = 25 V, f = 1 MHz	-	1275	1785	pF
Output Capacitance	Coss	$V_{GS} = 0 V$		-	486	681	
Reverse Transfer Capacitance	C _{rss}			-	15	21	
Total Gate Charge ^c	Qg		V _{DS} = 30 V, I _D = 15 A	-	17	26	nC
Gate-Source Charge ^c	Q _{gs}	$V_{GS} = 10 \text{ V}$		-	5	-	
Gate-Drain Charge ^c	Q _{gd}			-	2	-	
Gate Resistance	R _g	f = 1 MHz		1	2	3	Ω
Turn-On Delay Time ^c	t _{d(on)}	$V_{DD} = 30 \text{ V}, \text{ R}_L = 2 \Omega$ $\text{I}_D \cong 15 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		-	10	15	
Rise Time ^c	t _r			-	3	6	ns
Turn-Off Delay Time ^c	t _{d(off)}			-	20	30	
Fall Time ^c	t _f			-	2	4	
Source-Drain Diode Ratings and Chara	acteristics ^b						
Pulsed Current ^a	I _{SM}			-	-	102	Α
Forward Voltage	V _{SD}	$I_F = 7 \text{ A}, V_{GS} = 0 \text{ V}$		-	0.88	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100A/us		-	30	60	ns
Body diode reverse recovery charge	Q _{rr}			-	16	32	nC
Reverse recovery fall time	t _a			-	11	-	20
Reverse recovery rise time	t _b			-	19	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			-	-1.1	-	А

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

b. Guaranteed by design, not subject to production testing

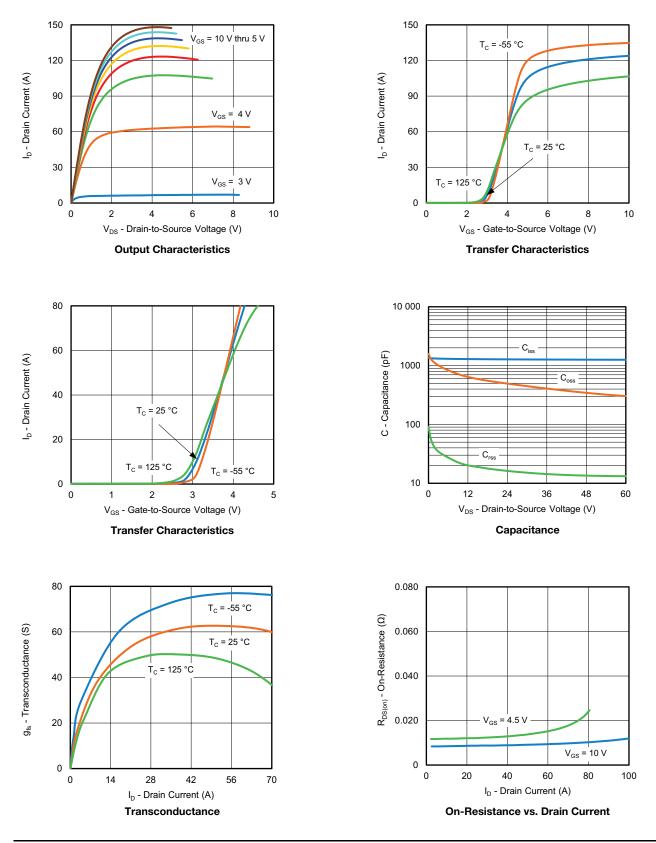
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



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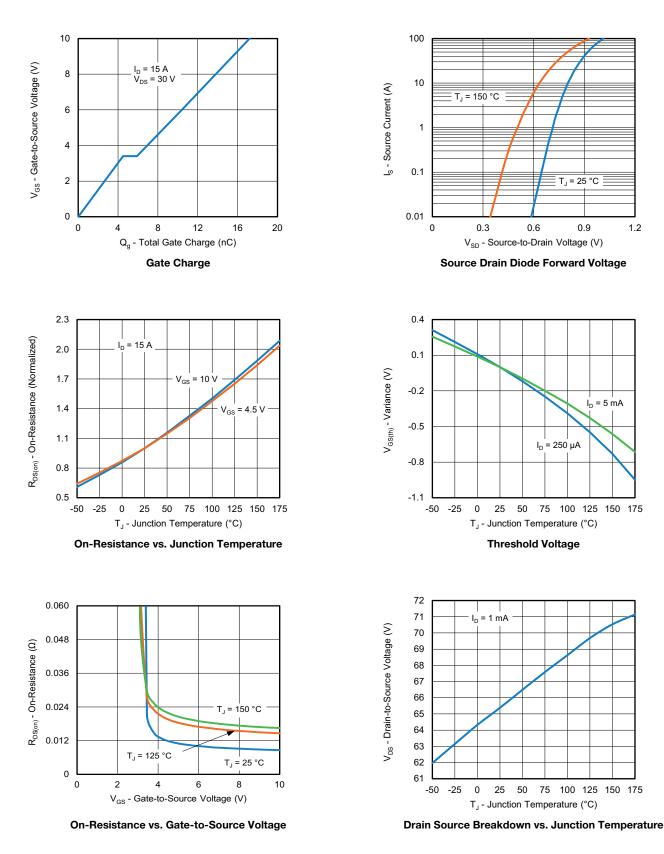
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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



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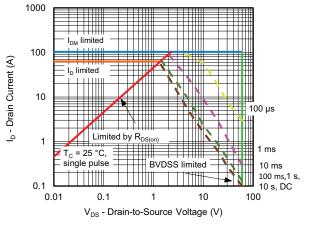
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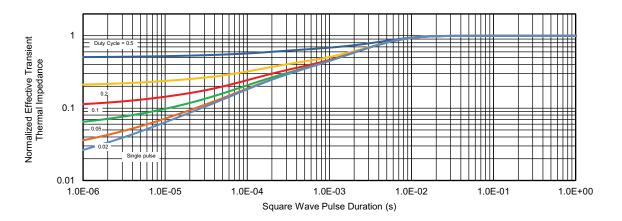
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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Safe Operating Area

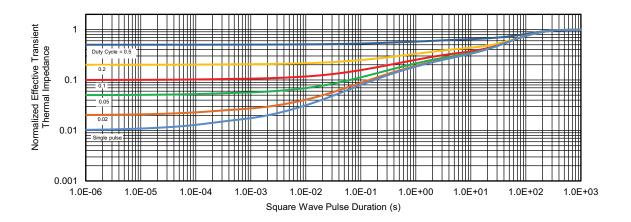


Normalized Thermal Transient Impedance, Junction-to-Case



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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

Note

The characteristics shown in the two graphs

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- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62453.



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