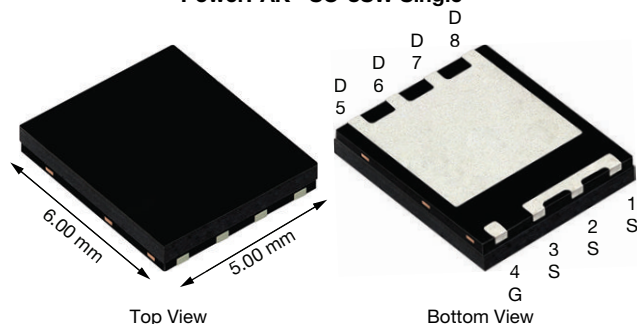


N-Channel 80 V (D-S) MOSFET

PowerPAK® SO-8SW Single


FEATURES

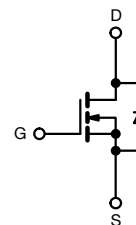
- TrenchFET® Gen V power MOSFET
- Very low $R_{DS(on)}$ x Q_g figure-of-merit (FOM)
- Leadership $R_{DS(on)}$ minimizes power loss from conduction
- 100 % R_g and UIS tested
- Enhance power dissipation and lower R_{thJC}
- Wettable flank to improved solderability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- DC/DC converters
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	80
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0025
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0032
Q_g typ. (nC)	38.5
I_D (A) ^a	190
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SO-8SW
Lead (Pb)-free and halogen-free	SiRS580DPW-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	190	A
	$T_C = 70$ °C	152	
	$T_A = 25$ °C	38 ^{b, c}	
	$T_A = 70$ °C	31 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	350	
Continuous source-drain diode current	$T_C = 25$ °C	156	
	$T_A = 25$ °C	6.3 ^{b, c}	
Single pulse avalanche current	$L = 0.1$ mH	53	
Single pulse avalanche energy	E_{AS}	143	mJ
Maximum power dissipation	$T_C = 25$ °C	171	W
	$T_C = 70$ °C	110	
	$T_A = 25$ °C	6.9 ^{b, c}	
	$T_A = 70$ °C	4.4 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	14	18	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.53	0.73	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 50 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	80	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	46	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-8.5	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 64 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 64 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.0020	0.0025	Ω
		V _{GS} = 7.5 V, I _D = 20 A	-	0.0024	0.0032	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 35 A	-	97	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	-	5045	-	pF
Output capacitance	C _{oss}		-	1580	-	
Reverse transfer capacitance	C _{rss}		-	12	-	
Total gate charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 20 A	-	51.2	77	nC
		V _{DS} = 40 V, V _{GS} = 7.5 V, I _D = 20 A	-	38.5	58	
Q _{gs}	-		20	-		
Q _{gd}	-		4.3	-		
Output charge	Q _{oss}	V _{DS} = 40 V, V _{GS} = 0 V	-	163	-	Ω
Gate resistance	R _g	f = 1 MHz	0.26	1.3	2.6	
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	18	40	ns
Rise time	t _r		-	8	15	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	13	25	
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	22	45	
Rise time	t _r		-	10	20	
Turn-off delay time	t _{d(off)}		-	28	60	
Fall time	t _f		-	14	30	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	156	A
Pulse diode forward current	I _{SM}		-	-	350	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.74	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	70	140	ns
Body diode reverse recovery charge	Q _{rr}		-	135	270	nC
Reverse recovery fall time	t _a		-	46	-	ns
Reverse recovery rise time	t _b		-	24	-	

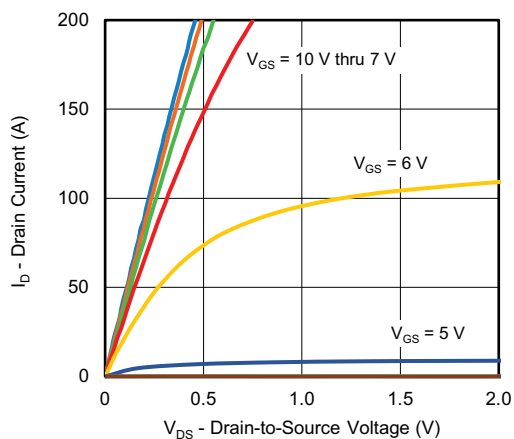
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

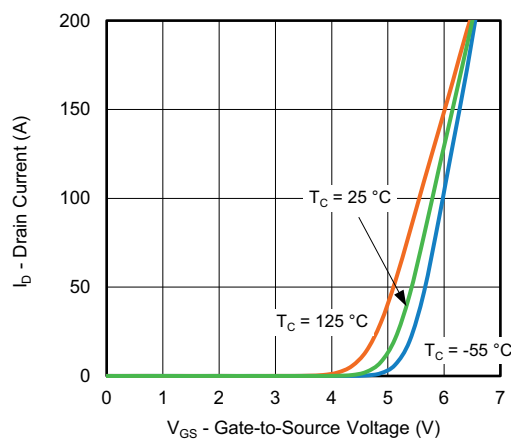
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



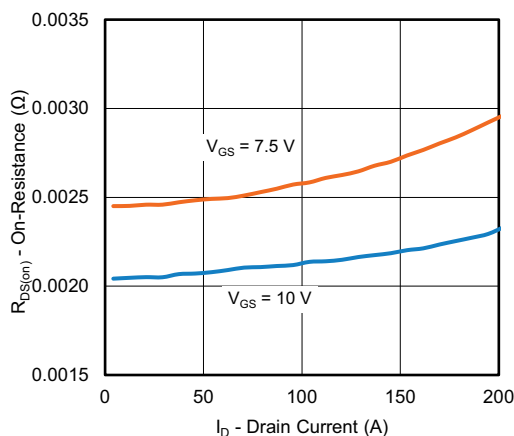
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



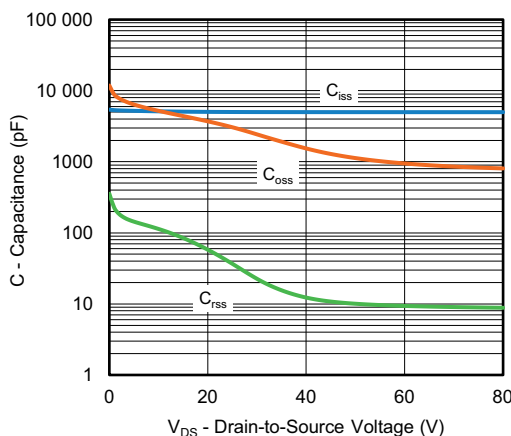
Output Characteristics



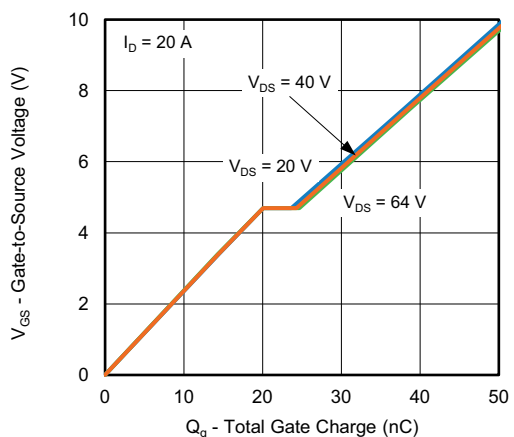
Transfer Characteristics



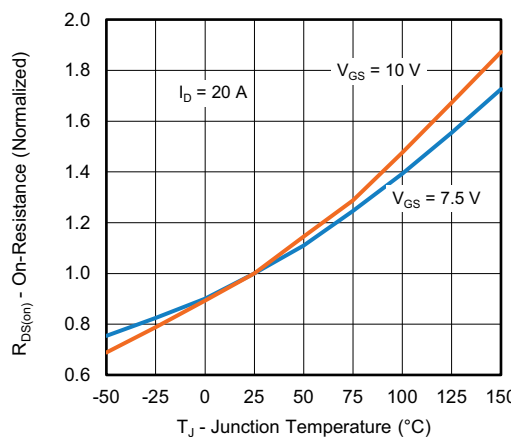
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



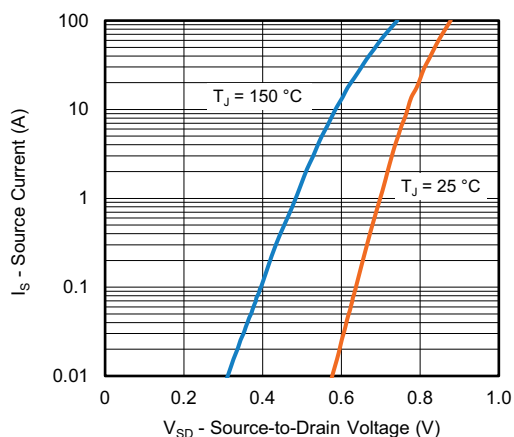
Gate Charge



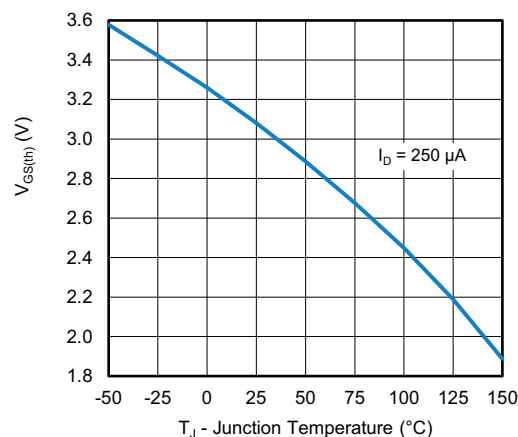
On-Resistance vs. Junction Temperature



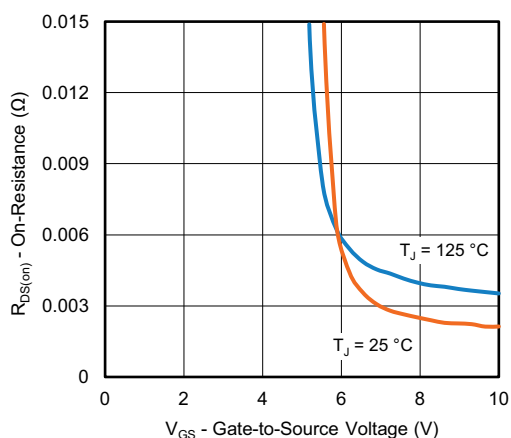
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



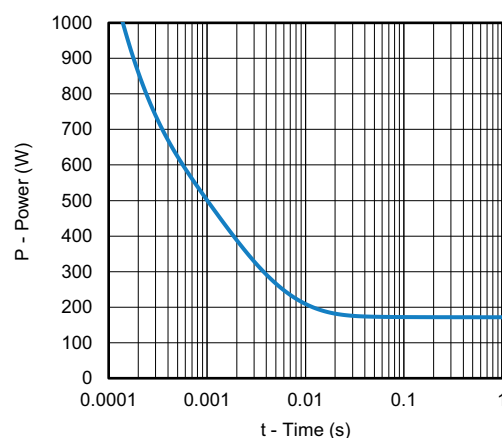
Source-Drain Diode Forward Voltage



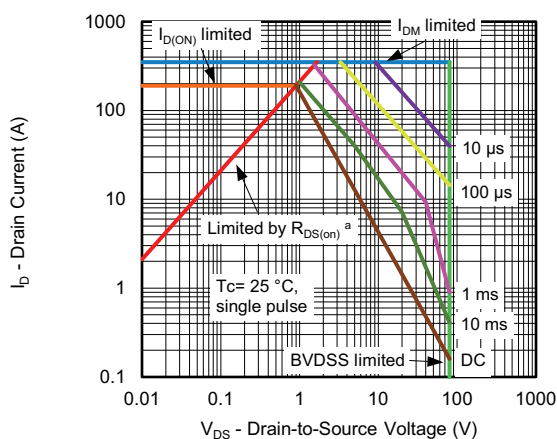
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



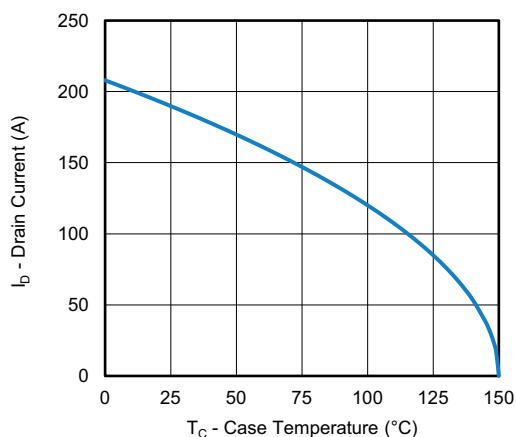
Safe Operating Area, Junction-to-Case

Note

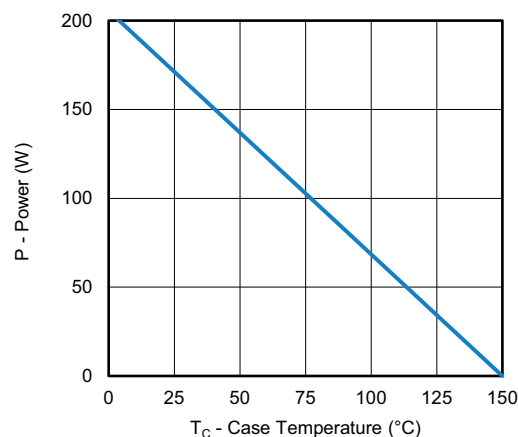
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



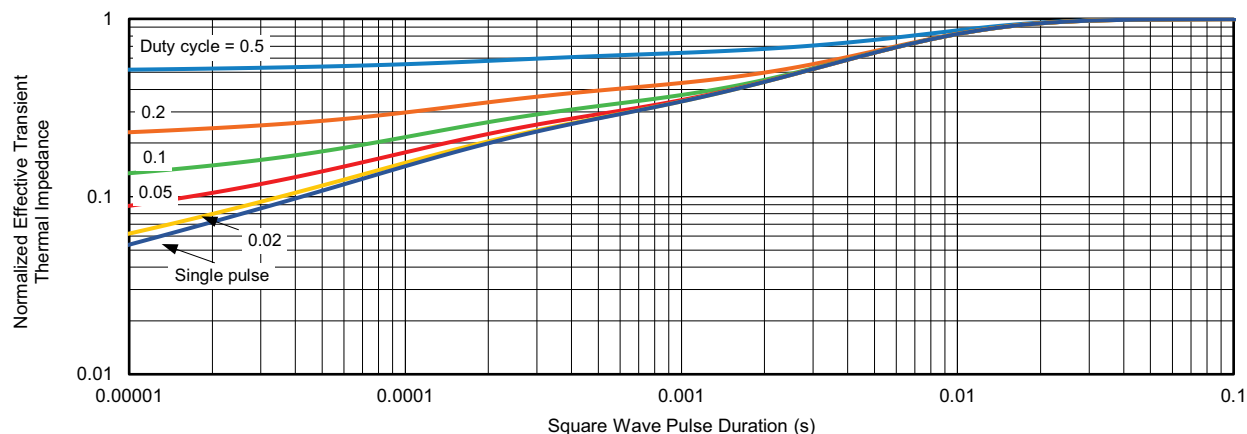
Current Derating ^a



Power, Junction-to-Case

Note

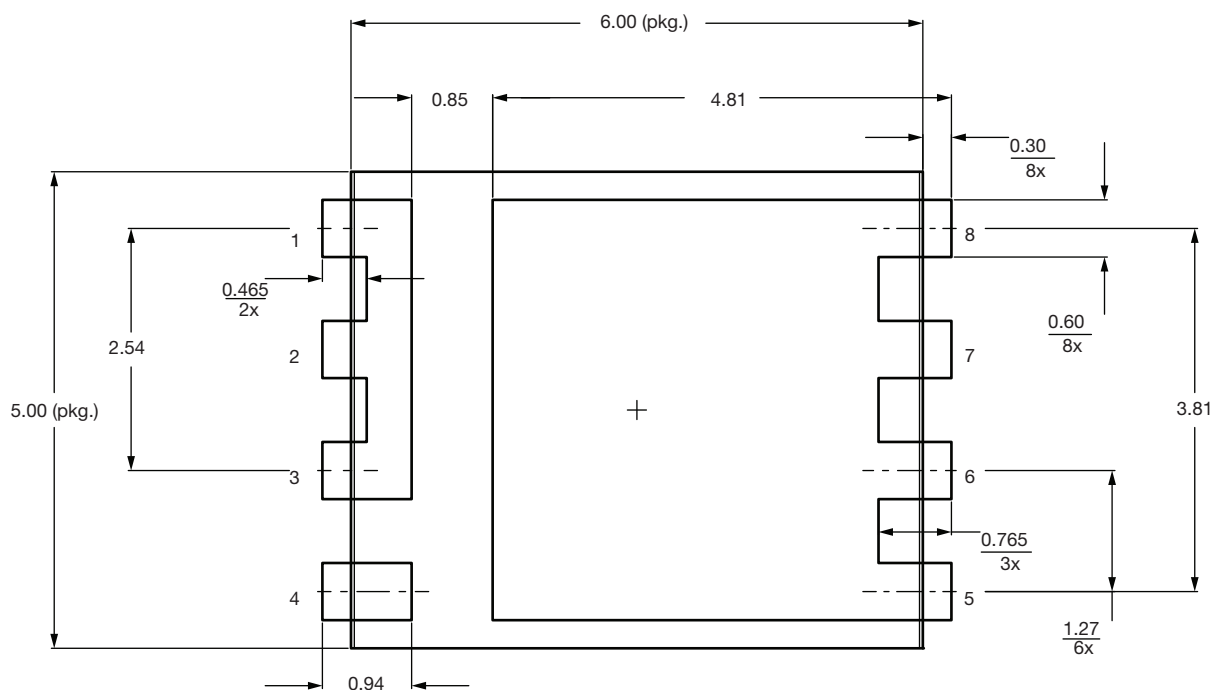
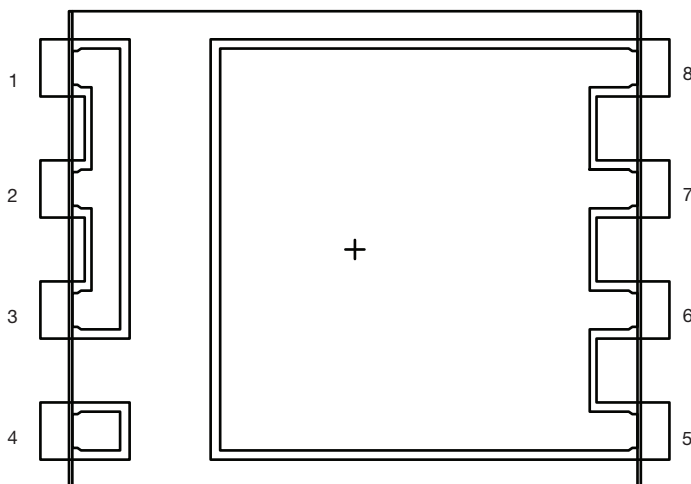
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62494.

Recommended Land Pattern PowerPAK® SO-8SW (PKSO8SWSCCL)


Note

- Dimensions in mm

ECN: C24-0483-Rev. A, 20-May-2024
DWG: 3027



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