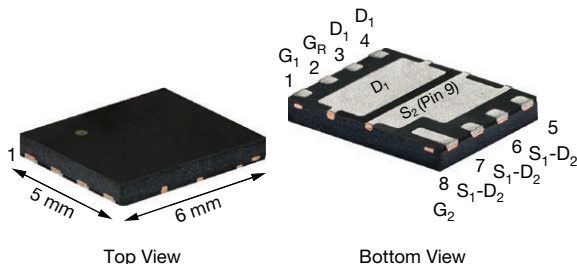


Symmetric Dual N-Channel 40 V (D-S) MOSFET

PowerPAIR® 6 x 5FSW



FEATURES

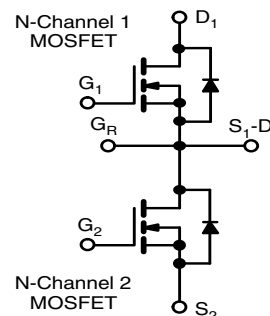
- TrenchFET® Gen IV power MOSFET
- 100 % R_g and UIS tested
- Integrated half-bridge MOSFET power stage
- Wettable flank terminals
- Internally connected switch node
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Buck-boost
- Half-bridge synchronous rectification
- Synchronous buck
- Motor drive control



PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0015
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0024
I_D (A) ^e	162
Configuration	Dual

ORDERING INFORMATION

Package	PowerPAIR 6 x 5FSW
Lead (Pb)-free and halogen-free	SQZF140ELPW-T1_GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ^e	I_D	$T_C = 25$ °C	162
		$T_C = 125$ °C	93
Pulsed drain current ^e	I_{DM}	543	A
Continuous source-drain diode current ^e	I_S	68	
Single pulse avalanche current	I_{AS}	37	
Single pulse avalanche energy	E_{AS}	68	mJ
Maximum power dissipation ^{a, e}	P_D	$T_C = 25$ °C	75
		$T_C = 125$ °C	25
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	30	°C/W
Junction-to-case (exposed pad) ^d	R_{thJC}	2.0	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per JESD51-14
- Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.2	1.7	2.2	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	100	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	500	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 15 A	-	0.00185	0.00240	Ω
		V _{GS} = 10 V	I _D = 15 A	-	0.00125	0.0015	
		V _{GS} = 10 V	I _D = 15 A, T _J = 125 °C	-	-	0.0024	
		V _{GS} = 10 V	I _D = 15 A, T _J = 175 °C	-	-	0.0030	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 70 A		-	200	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	5042	7059	pF
Output capacitance	C _{oss}			-	1096	1535	
Reverse transfer capacitance	C _{rss}			-	32	45	
Total gate charge	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 15 A	-	72	-	nC
Gate-source charge	Q _{gs}			-	15	-	
Gate-drain charge	Q _{gd}			-	12	-	
Gate resistance	R _g	f = 1 MHz		0.3	0.9	2.4	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1.33 Ω I _D ≅ 15 A, V _{GEN} = 10 V, R _g = 1 Ω		-	17	26	ns
Rise time	t _r			-	53	80	
Turn-off delay time	t _{d(off)}			-	40	60	
Fall time	t _f			-	8	12	
Source-Drain Diode Ratings and Characteristics ^b							
Body diode reverse recovery time	t _{rr}	I _F = 15 A, di/dt = 100 A/μs, T _J = 25 °C		-	42	84	ns
Body diode reverse recovery charge	Q _{rr}			-	38	76	nC
Reverse recovery fall time	t _a			-	22		A
Reverse recovery rise time	t _b			-	22		A
Pulsed current	I _{SM}			-	-	300	A
Forward voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V		-	0.75	1.1	V

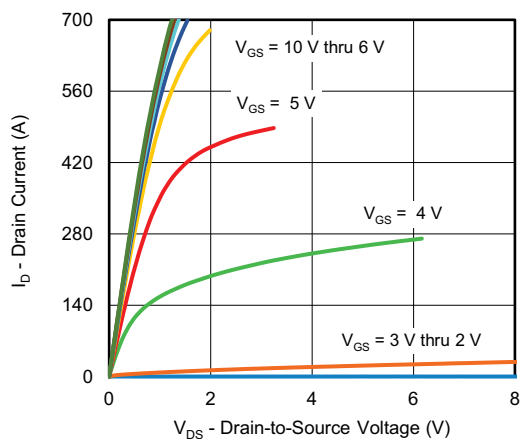
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

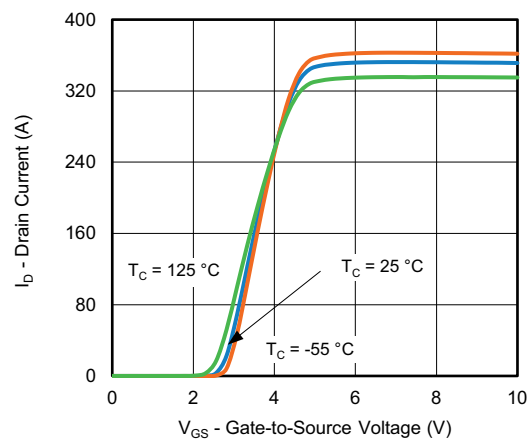
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



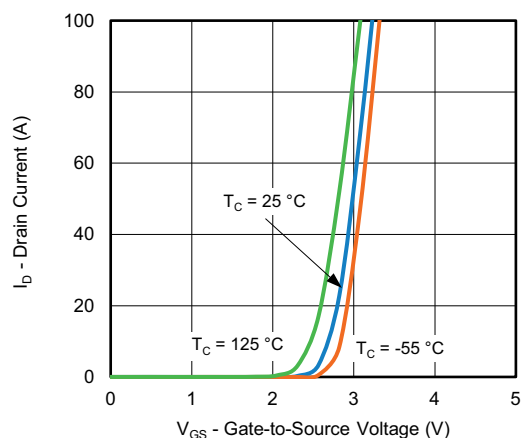
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



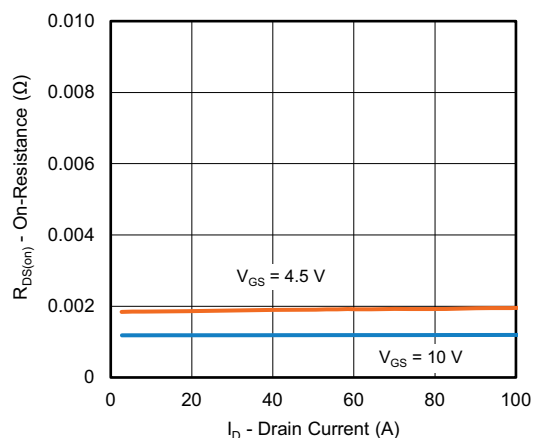
Output Characteristics



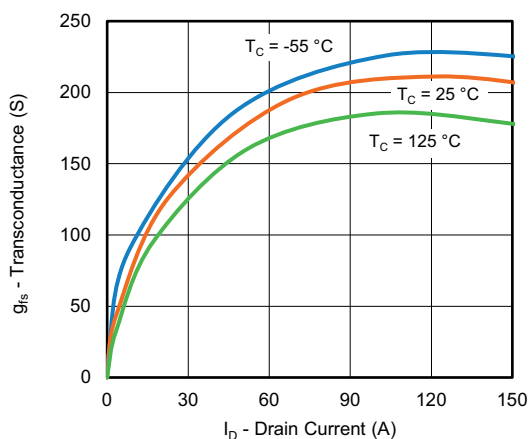
Transfer Characteristics



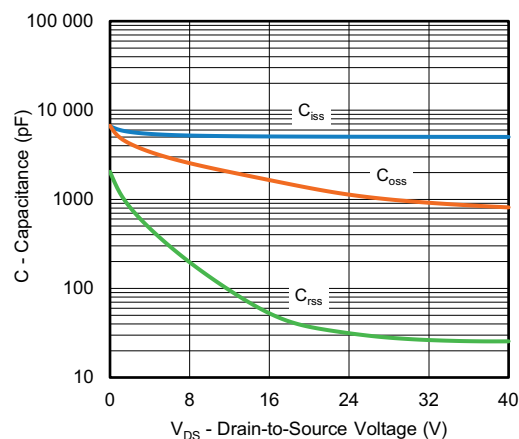
Transfer Characteristics



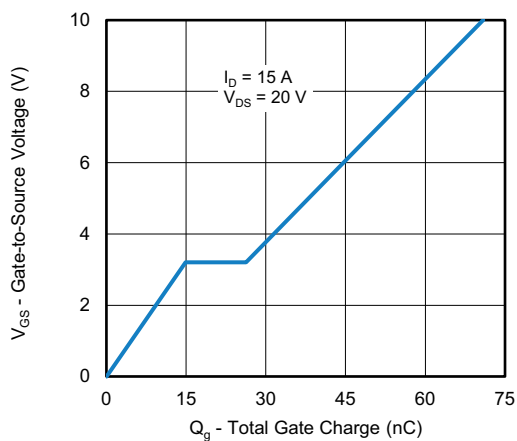
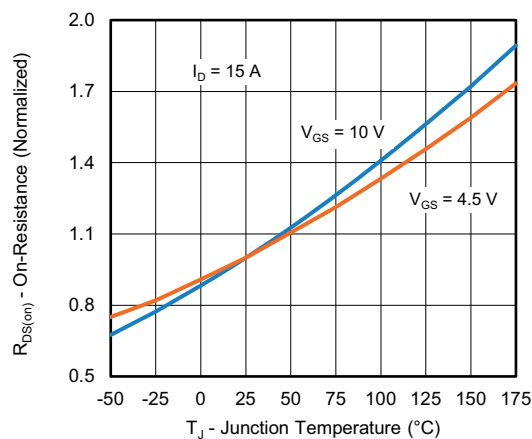
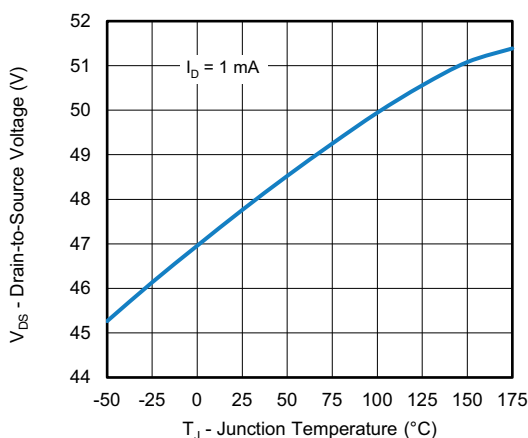
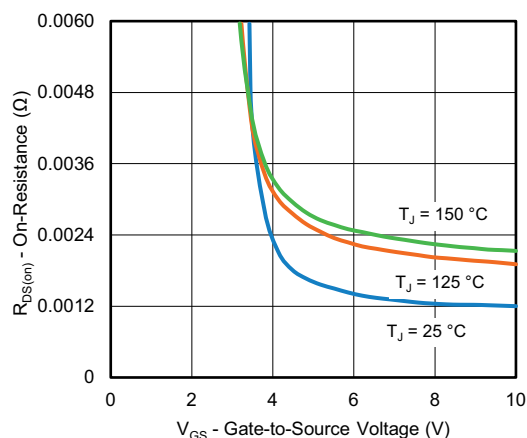
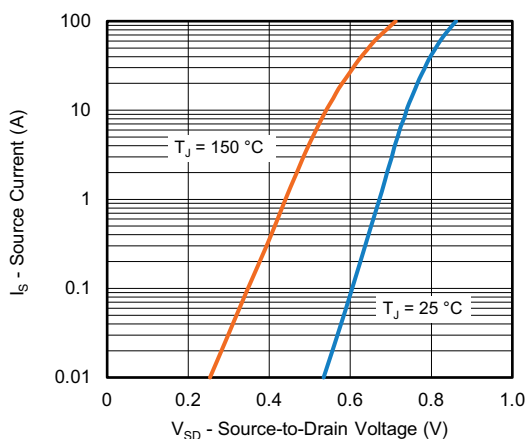
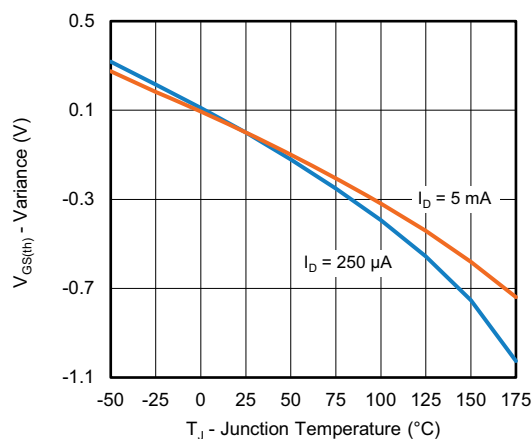
On-Resistance vs. Drain Current



Transconductance



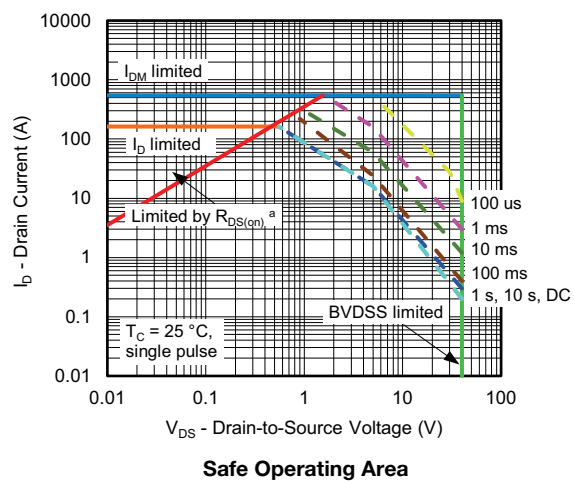
Capacitance

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Drain Source Breakdown vs. Junction Temperature

On-Resistance vs. Gate-to-Source Voltage

Source-Drain Diode Forward Voltage

Threshold Voltage
Note

- $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

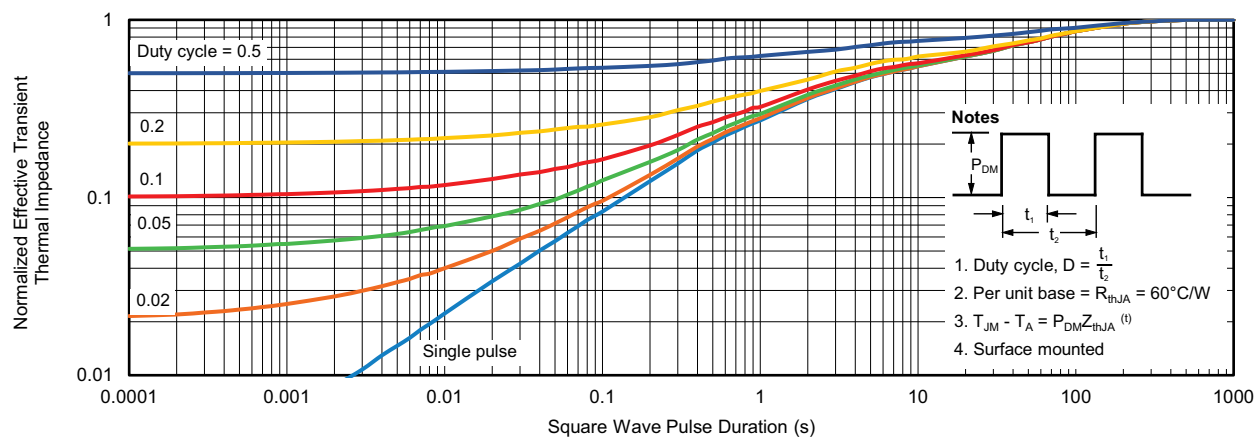


Note

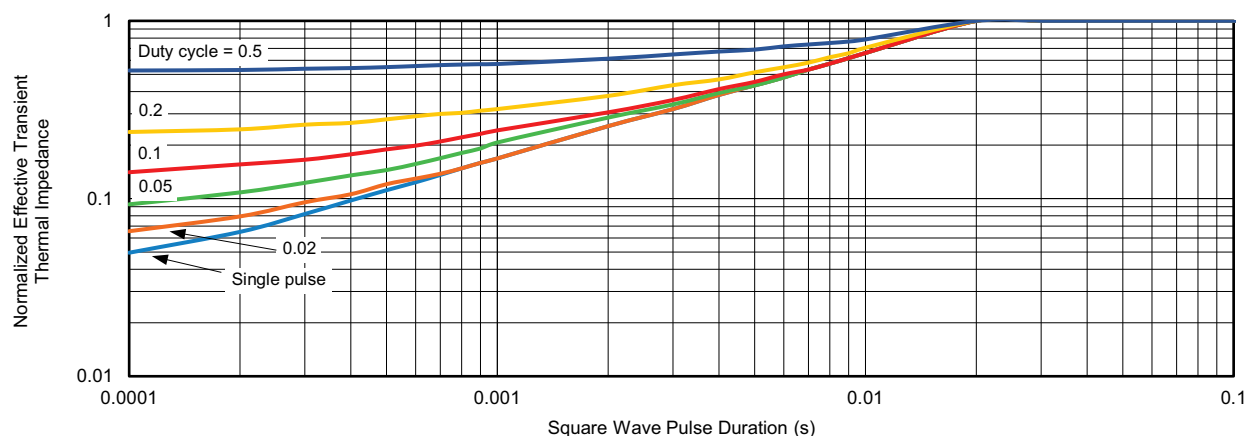
b. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



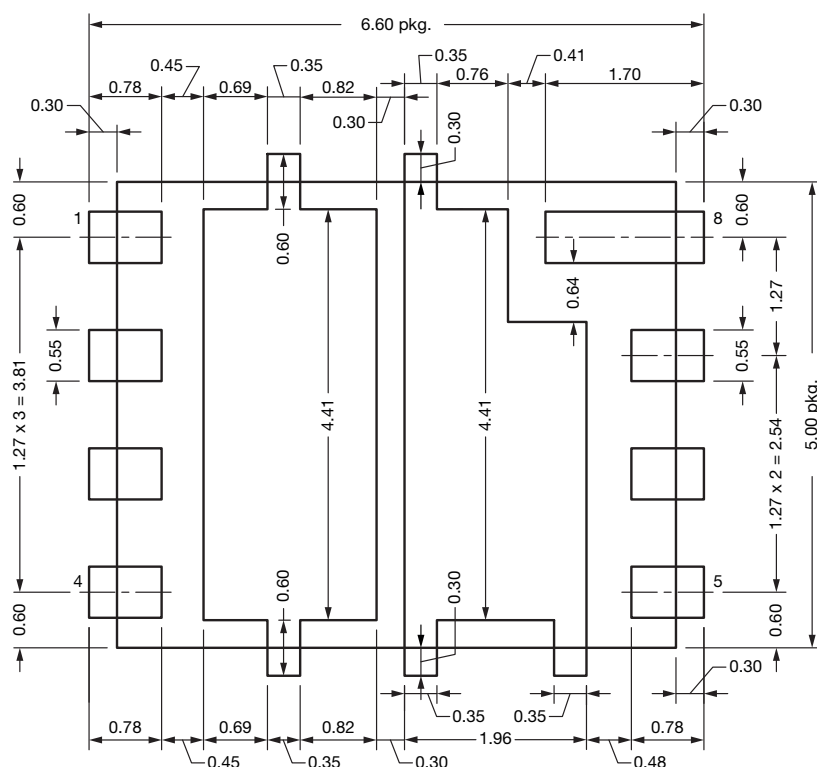
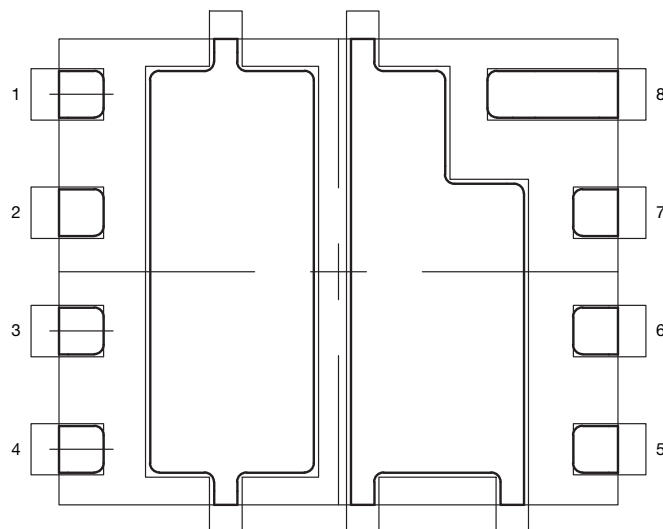
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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Recommended Land Pattern PowerPAIR® 6 x 5 FS and PowerPAIR® 6 x 5 FSW



Note

- Dimensions in mm

T24-0311-Rev. A, 09-Sep-2024
DWG: 3030



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