Dual N-Channel 30 V (D-S) MOSFETs

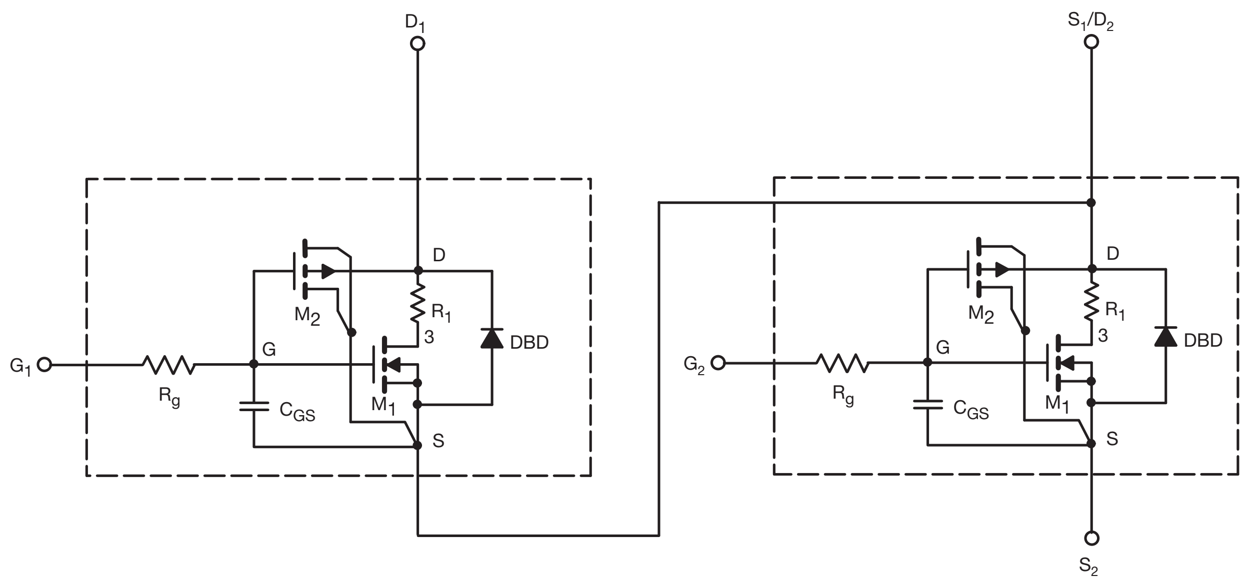
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	Ch-1	1.3	-	V
			Ch-2	1.3	-	
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 13.8 A	Ch-1	0.009	0.010	Ω
		V_{GS} = 10 V, I_D = 20 A	Ch-2	0.003	0.003	
		V_{GS} = 4.5 V, I_D = 12.6 A	Ch-1	0.010	0.012	
		V_{GS} = 4.5 V, I_D = 20 A	Ch-2	0.0035	0.0035	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 13.8 A	Ch-1	43	47	S
		V_{DS} = 10 V, I_D = 20 A	Ch-2	132	116	
Diode Forward Voltage[a]	V_{SD}	I_S = 10 A, V_{GS} = 0 V	Ch-1	0.82	0.85	V
		I_S = 10 A, V_{GS} = 0 V	Ch-2	0.80	0.80	
Dynamic[a]						
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	766	790	pF
			Ch-2	3800	3830	
Output Capacitance	C_{oss}		Ch-1	192	190	
			Ch-2	684	670	
Reverse Transfer Capacitance	C_{rss}		Ch-1	78	76	
			Ch-2	321	315	
Total Gate Charge	Q_g	Channel-1 V_{DS} = 15 V, V_{GS} = 10 V, I_D = 13.8 A	Ch-1	14	14	nC
		Channel-2 V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	Ch-2	64	67.3	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 13.8 A Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	Ch-1	7	6.8	
			Ch-2	32	32	
Gate-Source Charge	Q_{gs}		Ch-1	2.6	2.6	
			Ch-2	10.8	10.8	
Gate-Drain Charge	Q_{gd}		Ch-1	1.9	1.9	
			Ch-2	9.3	9.3	

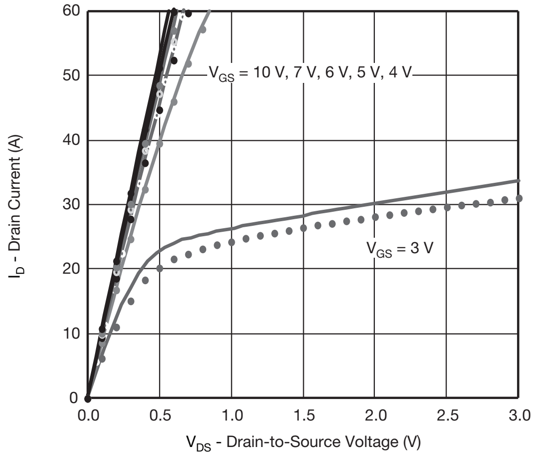
Notes

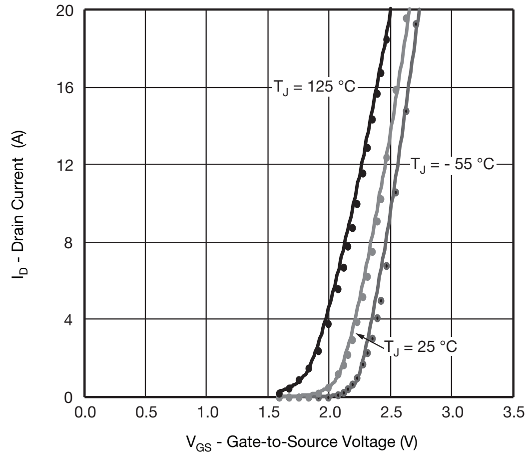
a. Guaranteed by design, not subject to production testing.

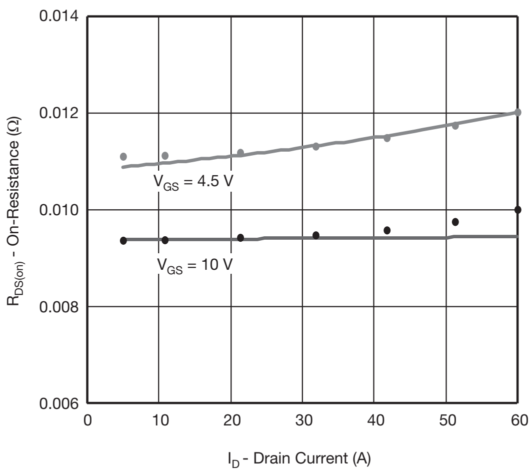
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

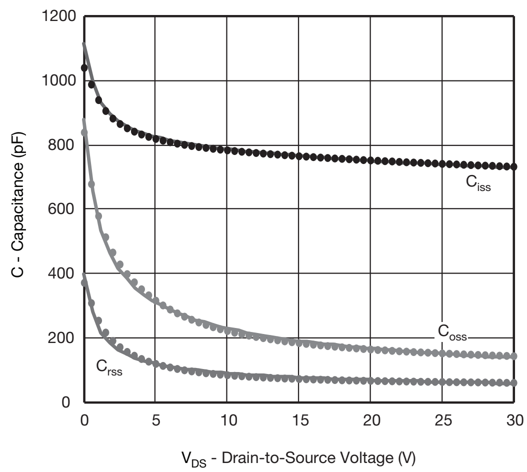
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

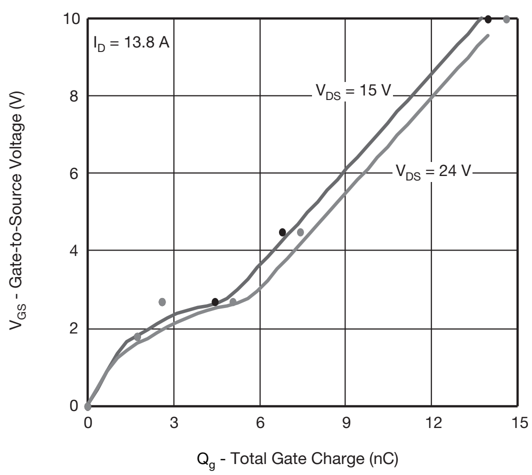
Channel 1 MOSFET

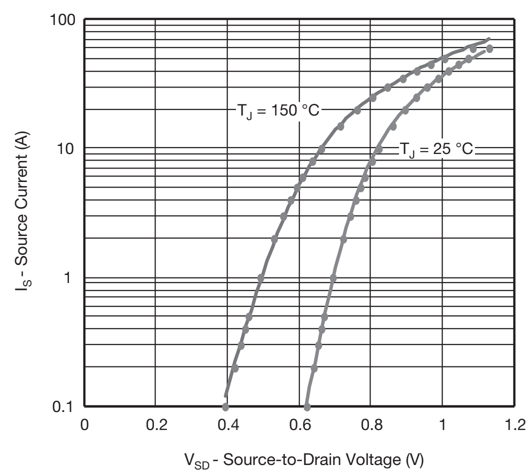










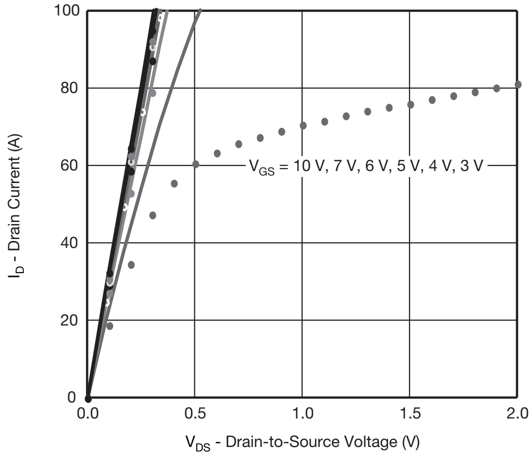


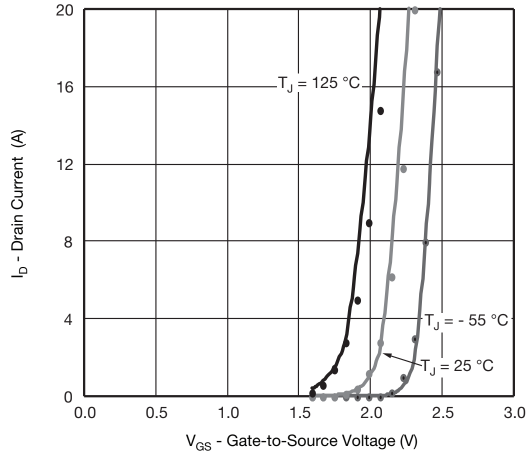
Note

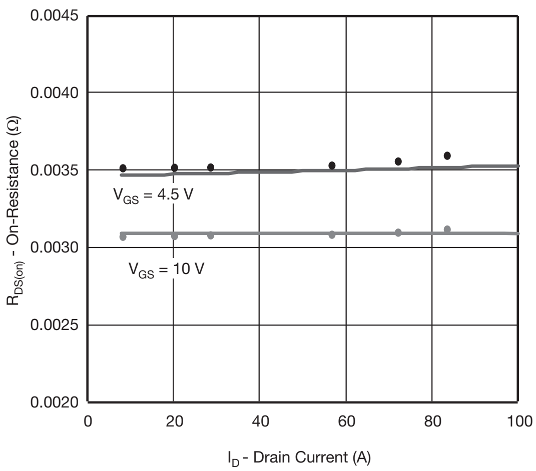
- Dots and squares represent measured data.

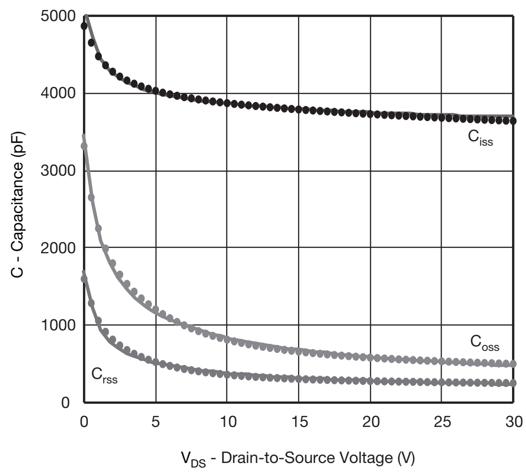
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

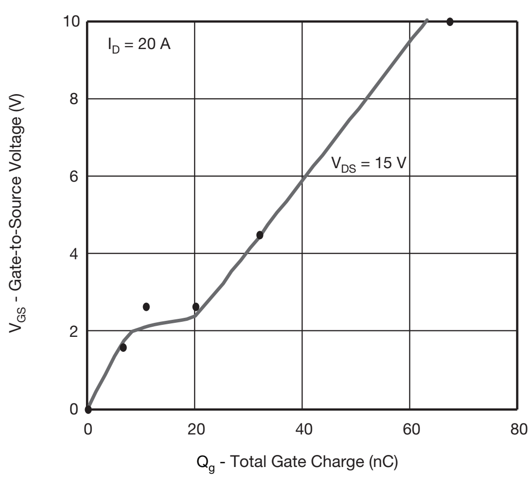
Channel 2 MOSFET

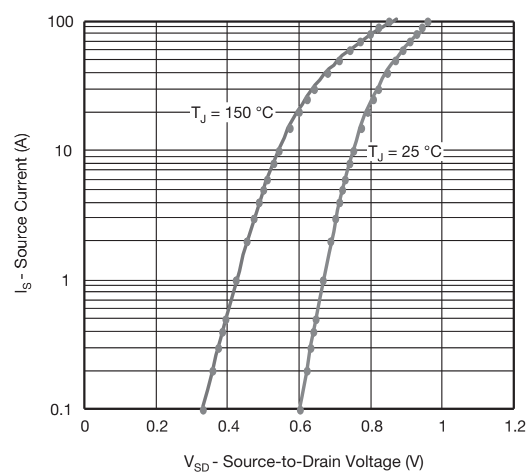












Note

- Dots and squares represent measured data.

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