

Vishay Siliconix

# **Dual N-Channel 8 V (D-S) MOSFET**

#### **DESCRIPTION**

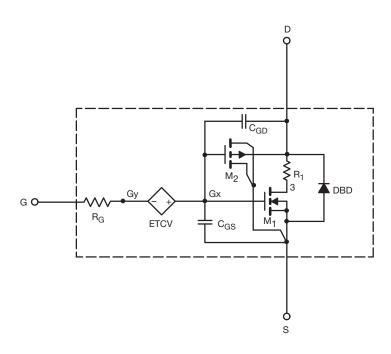
The attached spice model describes the typical electrical characteristics of the N-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### SUBCIRCUIT MODEL SCHEMATIC



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



# **SPICE Device Model SiA920DJ**

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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6	-	V
Drain-Source On-State Resistance <sup>a</sup>	Б	$V_{GS} = 4.5 \text{ V}, I_D = 5.3 \text{ A}$	0.022	0.022	Ω
	R <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 4.9 \text{ A}$	0.025	0.025	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 5.3 \text{ A}$	25	28	S
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5.5 A	0.75	0.80	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 0 V, f = 1 MHz	466	470	pF
Output Capacitance	C <sub>oss</sub>		174	175	
Reverse Transfer Capacitance	C <sub>rss</sub>		83	85	
Total Gate Charge	Qg	V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.9 A	4	4.8	nC
Gate-Source Charge	Q <sub>gs</sub>		0.63	0.63	
Gate-Drain Charge	$Q_{qd}$		0.60	0.60	

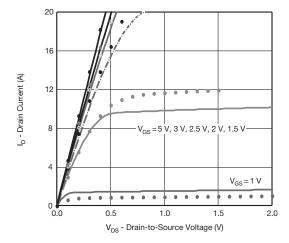
#### **Notes**

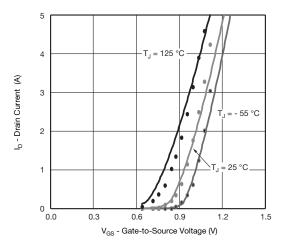
- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

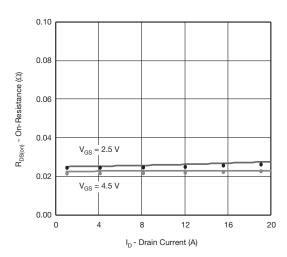
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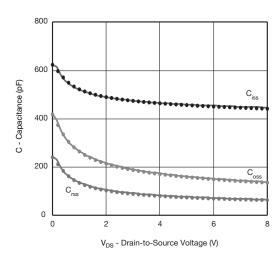
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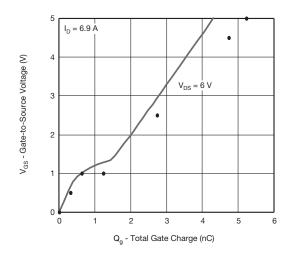
## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25~^{\circ}C$ , unless otherwise noted)

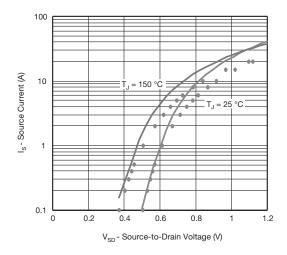












#### Note

• Dots and squares represent measured data.



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