FPGA Power Supply Considerations

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ABSTRACT

An FPGA is a device that offers many logic elements - up to 1 million gates in a single device at this writing - as well as other functionality such as transceivers, PLLs, and MAC units for complex processing. FPGAs are becoming very powerful, and the need to power the devices effectively is a key, if often underestimated, part of the design. A straightforward power supply design process can significantly reduce the number of required design iterations for the OEM designer.

This application note looks at the various types of voltage regulators used to power FPGAs, offers guidance on how and where to place them on the PCB, and takes the reader step-by-step through a design example involving an FPGA that needs to operate in a system supplied by a 12 V bus which is the main output from a mains-supplied SMPS.

VOLTAGE REGULATORS

There are two popular types of regulator that can be used to power the FPGA. These will receive an input voltage which is usually supplied by an off-line SMPS and can typically be between 5 V and 24 V. The regulators step the input voltage down to the required output voltage which may power the core, the I/O, or the auxiliary circuitry.

The action of stepping down a voltage can be carried out using a pass transistor as used in linear regulators. However, this has the effect of wasting a large proportion of the power across the transistor as heat, especially for larger input/output voltage ratios where efficiency can be as low as 50 %. The advantage of the linear regulator is the low noise output and straightforward design process.

It is common practice when powering more powerful FPGAs to use a buck regulator. The buck regulator samples the input voltage and this pulse waveform is then integrated using an inductor and capacitor filter. The accuracy of this sampling is determined by the control technique used, the layout of the system, and also the effect of the devices employed to achieve the required output.

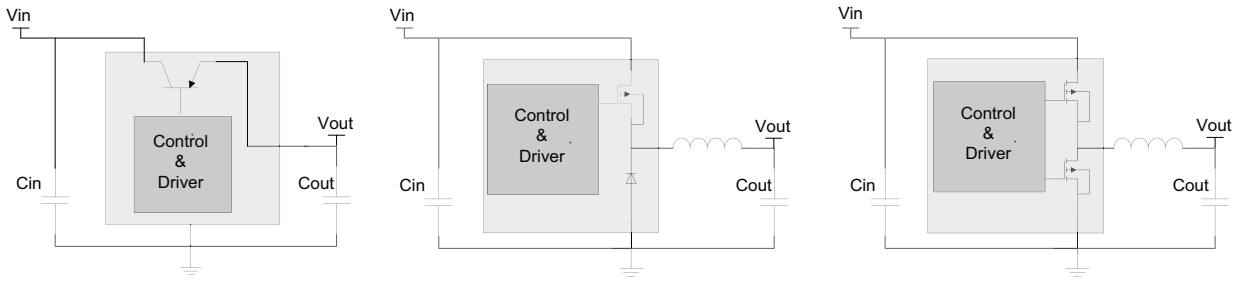

Fig. 1 - a) Linear Regulator b) Asynchronous Buck c) Synchronous Buck

The buck regulator can be implemented in asynchronous operation whereby the low-side freewheel action is achieved using a diode, or in synchronous operation where the low-side freewheel action is achieved using a second MOSFET. Synchronous buck regulators achieve higher efficiencies due to the lower $R_{DS(ON)}$ of the low-side MOSFET compared to the diode forward voltage and series resistance of the diode. The synchronous buck regulator is useful when current increases past that of an amp or when there is a large voltage to be stepped down. This involves a small duty cycle and hence the low side is on for a large percentage of the duty cycle.

APPLICATION NOTE

FPGA Power Supply Considerations

Integrated switching regulators such as the Vishay microBUCK® synchronous buck regulator series are a popular choice for this application. microBUCK benefits include an advanced constant-on-time (COT) topology offering fast transient response and allowing a reduction in output component sizes. This allows designers to achieve the levels of ripple voltage, transient response, and efficiency their designs require.

POWER ESTIMATORS AND VOLTAGE REQUIREMENTS

The key part of the design is to determine the voltage requirements needed and the current requirements of each voltage rail. The major FPGA vendors offer software to provide an estimation of the power supply requirements at a suitable stage in the design process. For instance, Altera offers the PowerPlay Early Power Estimator (1) and Xilinx offers the XPower Analyser (2). These are comprehensive calculators that take into account the frequency that the part operates at, the number of gates used, as well as the toggle rate of the gates.

Table 1 contains some of the typical voltage rails required by Altera and Xilinx devices. They are broken down into the core voltage, the I/O voltages, and the transceiver and auxiliary voltages. The main power requirement will be for the core, followed by that of the I/Os, and then the auxiliary needs.

POL AND POWER DISTRIBUTION SYSTEM

TABLE 1 - VOLTAGE REQUIREMENTS OF A SELECTION OF ALTERA AND XILINX FPGAS

	PART NUMBER	LOGIC (Ks)	CORE VOLTAGE (V)	CORE TOL. (mV)	AUILLIARY VOLTAGES		I/O VOLTAGES (V)	I/O TOL. (%)
					(V)			
Altera								
Stratix V	5SEBA	1087	0.85	30	2.5	(VCCA_PLL)	1.2 - 3	5
					1.5	(VCCD_PLL)		5
Cyclone IV GX	EP4CGX150	150	1.2	40	2.5	(VCCA, VCCA_GXB, VCCH_GXB)	1.2 - 3	5
					1.2	(VCCD_PLL, VCC_CLKIN)		5
Arria V	5AGXB7	503	1.1	30	2.5	(VCC_AUX, VCCA_FPLL,VCCPD)	1.2 - 3.3	5
Xilinx								
Virtex 6	XC6VLX760	760	1	50	2.5	(VCC_AUX)	1.2 - 2.5	5
Virtex 6	XC7V2000T	2000	1	30	1	(MGTAVCC, VCCBRAM)	1.2 - 1.8	5
					1.2	(MGTAVTT)	-	-
					1.8	(MGTVCCAUX, VCCAUX, VCCAUX_IO)	-	-
					4.5	(VCCBRAM)	-	-
Spartan 6	XC6SLS150T	147	1.2	60	1.2	(MGTAVCC, MGTAVCCPLL, MGTAVTTRX, MGTAVTTTX)	1.2 - 3.3	5
					2.5	(VCCAUX)	-	-
					3.3		-	-
Artix 7	XC7A350T	360	1	30	1	(MGTAVCC, VCCBRAM, VCCINT)	1.2 - 3.3	5
					1.2	(MGTAVTT)		-
					1.8	(MGTVCCAUX, VCCAUX, VCCAUX_IO)		-

FPGAs with lower core voltage needs will require a large amount of current, which has to be supplied with a reasonably low noise floor and a minimum amount of ripple voltage. In order to achieve this the standard decoupling method is to place the capacitance as close as possible to the FPGA with minimal ESR and ESL in the decoupling path; any vias and traces used must be scrutinized to reduce the possibility of transients because of the tuned circuit that may be accidentally created.

Another useful method to achieve a more effective power design is to place the POL regulators as near to the part as possible without affecting routing in and out of the FPGA. This will reduce the trace lengths and consequently the effective ESR and ESL. In general the shorter the path length with this type of converter the better. Vishay's microBUCK series offers very high operating

FPGA Power Supply Considerations

frequencies from advanced device packaging with integrated control, drivers and MOSFETs, enabling a compact layout and small solution footprint. The small size allows for relatively close placement of the regulators to the FPGA while the higher frequency allows for smaller external passives without compromising transient response.

Fig. 2 - Step Response of SiP12107.
V_{IN} = 5 V, V_{OUT} = 1.2 V, F_{SW} = 2 MHz; Load step at 20 kHz = 0 A to 3 A; L = 330 nH, C_{IN} = 22 µF, C_{OUT} = 22 µF; Yellow = V_{OUT}, Blue = current.

Figure 2 provides a snapshot of the voltage step seen in the SiP12107 current mode constant-on-time (CM-COT) topology regulator. The load is a stepped 20 kHz, 0 A to 3 A load with a 50 % duty cycle. The step response, with minimal input and output capacitance of 22 µF (0805) and a relatively small 330 nH inductor (IHLP2020) can be observed as 37 mV Pk-Pk (the load has some capacitance also).

In using the current mode constant-on-time (CM-COT), the controller is free from the limitations of external voltage ripple (which was used to improve stability) thanks to the internal current ramp sensing scheme eliminating the need for significant ESR in the output capacitors or an ESR network. This allows for improved efficiency, reduced component count, and an excellent transient response.

Figure 3 represents a typical power architecture for an FPGA power delivery system. The input voltage will be sourced from a mains SMPS, a battery, or DC/DC converter. This voltage can be in the region of 5 V to upwards of 24 V depending on the application area; for example, a telecoms application may be 48 V. The efficiency and voltage requirements of the system will need to be understood and this will determine whether an intermediate step down conversion is needed. From this point the architecture that feeds the FPGA, the POL system, is worked on.

FPGA Power Supply Considerations

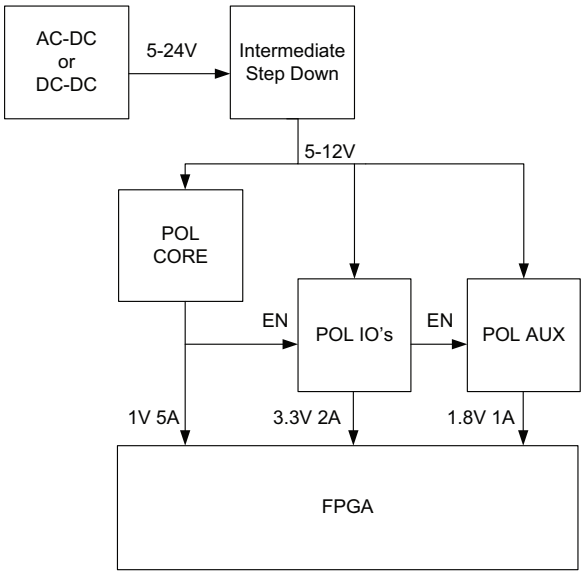

Fig. 3 - Typical Power Architecture and Start Up Control

POWER-UP SEQUENCING

Power-up sequencing is not a requirement stated by some of the FPGA vendors for the newer devices, but a sensible approach is to power up the core voltage first and then the I/Os followed by the auxiliary supplies. Scrutinizing the datasheet should reveal any device requirements. Power-up sequencing can be achieved by allowing the enable pins to be controlled by the previous stage that has powered up; an extra delay can be added with an external RC circuit as well. This a basic and straightforward method, but if more intelligence is required a small micro-controller may be employed to control the startup routine. This also has the benefit of being deterministic with no RC variables to be concerned about.

CHOOSING THE RIGHT REGULATOR

There are a number of regulators in the microBUCK range that are summarized in table 2. The applications for these devices are varied but in general they are suitable in any POL application that requires tight regulation with high efficiency. A linear regulator is also included in the list for low current, low dropout applications.

TABLE 2 - VISHAY LINEAR AND BUCK REGULATORS

PART NUMBER	$V_{IN(min.)}$ (V)	$V_{IN(max.)}$ (V)	F_{SW} (min.) (kHZ)	F_{SW} (max.) (kHZ)	$I_{OUT(max.)}$ (A)	En	START UP (ms)	POWER SAVE MODE	LDO VOLTAGE (V)	LDO CURRENT (A)
SiP21106	2.2	6	Linear	Linear	0.15	Y	-	-	-	-
SiP12107	2.7	5.5	200	4000	3	Y	1.5	Y	-	-
SiP12108	2.7	5.5	200	4000	5	Y	1.5	Y	-	-
SiP12109	4.5	16	400	1500	4	Y	User	Y		-
SiC401A/B	3	17	200	1000	15	Y	12	Y	5	0.2
SiC402A/B	3	28	200	1000	10	Y	12	Y	5	0.2
SiC403A/B	3	28	200	1000	6	Y	12	Y	5	0.2
SiC413	4.5	26	500	500	4	Y	5	N	-	-
SiC414/424	3	28	200	1000	6	Y	1.7	Y	-	-

FPGA Power Supply Considerations

Table 2 also contains several features of each of the devices. Of key importance and the first reference should be the operating voltage; this will be the first decision that is made regarding the device. Next the current requirements should be checked. Once the device list is narrowed down then a further inspection of features such as operating frequency range, low current power mode savings, and so on should enable the designer to hone in on the part that best fits the application.

The initial understanding of what the device can offer will lead to a more detailed look at the datasheet.

Vishay regulators are supported with the online simulation tool, PowerCAD (3). This allows users to quickly develop a design. Once this is complete, the operational waveforms such as start-up, step response, and steady-state operation can be inspected for current and voltage magnitudes. Efficiency and a breakdown of all component losses as well as a BOM generator are also features of this simulator. The simulation schematic additionally allows users to alter the part parameters and arrive at a quick understanding of the effect that substituting parts has on the circuit. A snapshot of the simulation schematic can be seen in Figure 4.

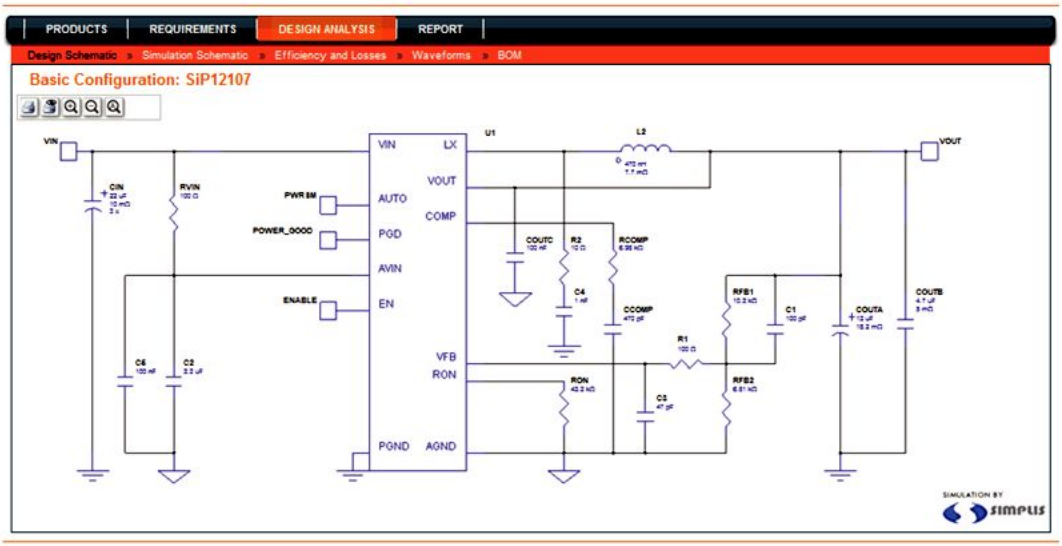

Fig. 4 - Vishay PowerCAD Software Simulation Schematic

EXAMPLE OF INITIAL DESIGN PROCEDURE

An FPGA is required to operate in a system supplied by a 12 V bus, which is the main output from a mains-supplied SMPS. There are no requirements for frequency of operation although an efficiency of greater than 80 % is required. The design specification has resulted in the choice of a Cyclone IV EP4CGX75 running at a clock speed of 362 MHz.

1 - Using PowerPlay (1) a current requirement for each rail is determined. At this point the FPGA design will allow the designer to extract the number of logic gates being used, PLLs, transceivers, and any other functionality such as toggle rate of components and frequency of operation. An understanding of the interface circuitry is useful also as it provides the load requirements placed upon the FPGA I/Os. The extra circuitry can be added to the power supply requirements, but we will look at powering the FPGA only with worst-case loads on the outputs. Table 3 captures the design specification that was provided by the early estimator software (1).

FPGA Power Supply Considerations

TABLE 4 - DESIGN SPECIFICATIONS DERIVED FROM ALTERA POWERPLAY					
	PART NUMBER	DESCRIPTION	VOLTAGE (V)	V_{RIPPLE} (mV)	CURRENT (A)
Altera					
Cyclone IV GX	EPC4CGX75	VCORE	1.2	30	5
		VCCL_GXB	1.2	30	1
		VCCA	2.5	125	0.5
		VCCA_GXB	2.5	125	0.1
		VCC_CLKIN	3.3	165	0.1
		VCCIO_1-11	3.3	165	4.4

2 - Selection of devices can now take place. From table 3 the core voltage of the device is 1.2 V at 5 A. There is also another requirement from this rail of 1 A, making a total of 6 A from the voltage rail. In fact this is true for the other two voltages. With adequate holdup capacitance and effective placement of capacitors, these voltages can be supplied by the same regulator. Table 3 can be updated as seen in table 4.

TABLE 5 - REQUIREMENTS SPECIFICATION										
	RAIL NUMBER	VOLTAGE (V)	V_{RIPPLE} (mV)	CURRENT (A)	HEADROOM + 10 % (A)	POWER (W)	η min. (%)	PIN (W)	V_{IN} (V)	I_{IN}(A)
Altera										
EPC4CGX75	1	1.2	30	6	6.6	7.94	80 %	9.9	12	1.21
	2	2.5	125	0.6	0.66	1.65	80 %	2.1	3.3	0.63
	3	3.3	165	4.95	4.95	16.34	80 %	21	12	2.27

Table 4 reveals the voltages that require a regulator choice. A headroom has also been given as there is a possibility that the power requirement may increase with design progress. While this will have the effect of initially designing with a slightly larger inductor and capacitance, it will reduce the risk of a design update at a later date.

There are no switching frequency requirements, so these will be kept to within 500 kHz. The switching frequency will, however, affect the transient response. Also, since the energy stored in the inductor is transferred to the output capacitor at higher frequency, both inductor and the capacitor size can be reduced. With an initial specification table 2 reveals that the design requires two SiC40X devices powered from the 12 V input voltage along with an SiP12108 powered from the 3.3 V rail.

FPGA Power Supply Considerations

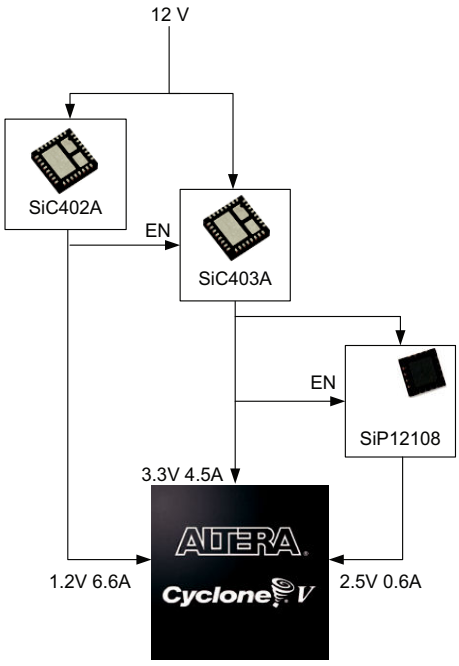

Fig. 5 - Example Solution

3 - Efficiency and the overall design can now be inspected. This can be achieved easily using Vishay PowerCAD simulation tools, which provide a first insight into the circuit that will be required. Running the simulator provides the results found in table 5.

TABLE 6 - RESULTS FROM POWERCAD SIMULATION

PART NUMBER	V_{IN} (V)	V_{OUT} (V)	F_{SW} (kHZ)	V_{RIPPLE} (mV)	I_{OUT} (A)	En	C_{OUT} (µF)	L_{BUCK} (µH)	LOAD STEP (mV)	η (%)
SiC402A	12	1.2	300	< 30	6	Y	330	2.2	< 50	88
SiC403A	12	3.3	500	< 30	5.1	Y	82	4.7	< 50	94
SiP12108	3.3	2.5	300	< 30	0.6	Y	6.8	6.8	< 50	96

These simulations are within 1 % to 2 % of the final design in terms of efficiency. Although they do not replace the need for a thorough design process they allow a quick look at the result that may be achieved using Vishay regulators.

REFERENCES

(1) Altera PowerPlay Early Estimator - www.altera.co.uk/support/devices/estimator/pow-powerplay.jsp
(2) Xilinx XPower Analyser - www.xilinx.com/products/technology/power/index.htm
(3) Vishay PowerCAD - vishay.transim.com/power/Products.aspx
(4) SiC401A/B Datasheet - www.vishay.com/doc?/63835
(5) SiC402A/B Datasheet - www.vishay.com/doc?/63729
(6) SiC403A/B Datasheet - www.vishay.com/doc?/62768
(7) SiP12107 Datasheet - www.vishay.com/doc?/63395

APPLICATION NOTE