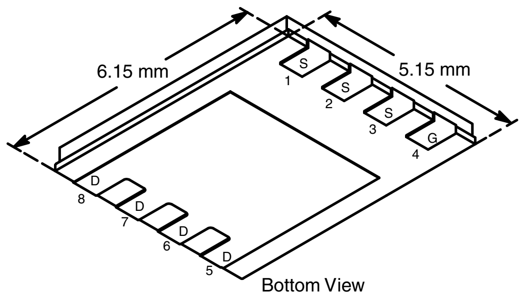
N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)[a,g]	Q_g (Typ.)
30	0.0068 at V_{GS} = 10 V	16	13.2 nC
	0.0097at V_{GS} = 4.5 V	16	

PowerPAK® SO-8



Ordering Information:
SiRA16DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

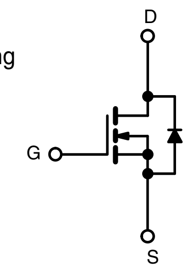
FEATURES

- TrenchFET® Gen IV Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- DC/DC Conversion
- High Current Power Rails in Computing
- Load Switching
- Battery Protection
- DC/AC Inverters



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	+ 20, - 16	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	16[g]	A
	T_C = 70 °C		16[g]	
	T_A = 25 °C		16[b, c]	
	T_A = 70 °C		14.2[b, c]	
Pulsed Drain Current (t = 100 µs)		I_{DM}	70	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	16[g]	
	T_A = 25 °C		3.5[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	15	
Single Pulse Avalanche Energy		E_{AS}	11.25	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	29.7	W
	T_C = 70 °C		19	
	T_A = 25 °C		3.9[b, c]	
	T_A = 70 °C		25[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	27	32	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3.5	4.2	

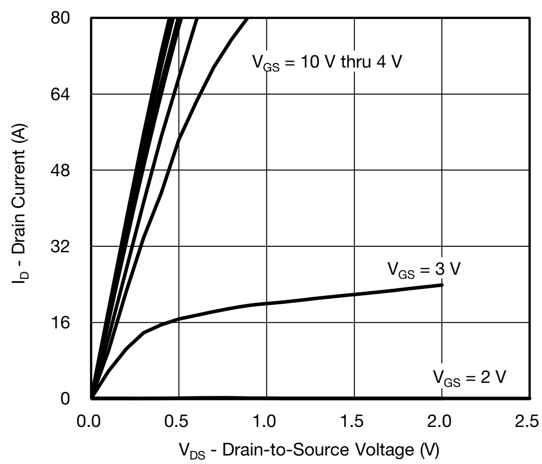
Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 70 °C/W.
g. Package limited.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		18		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1		2.3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = + 20, - 16 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.0056	0.0068	Ω
		V_{GS} = 4.5 V, I_D = 10 A		0.0077	0.0097	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 15 A		60		S
Dynamic[b, d]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		2060		pF
Output Capacitance	C_{oss}			543		
Reverse Transfer Capacitance	C_{rss}			47		
C_{rss}/C_{iss} Ratio				0.023	0.046	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A		31	47	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A		13.2	20	
Gate-Source Charge	Q_{gs}			5.7		
Gate-Drain Charge	Q_{gd}			2.2		
Output Charge	Q_{oss}	V_{DS} = 15 V, V_{GS} = 0 V		15.4		
Gate Resistance	R_g	f = 1 MHz	0.4	1.0	1.7	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		21	42	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			19	38	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		10	20	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			19	38	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			16	A
Pulse Diode Forward Current (t = 100 µs)	I_{SM}				70	
Body Diode Voltage	V_{SD}	I_S = 5 A		0.78	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 5 A, dI/dt = 100 A/µs, T_J = 25 °C		28	55	ns
Body Diode Reverse Recovery Charge	Q_{rr}			20	40	nC
Reverse Recovery Fall Time	t_a			14		ns
Reverse Recovery Rise Time	t_b			14		

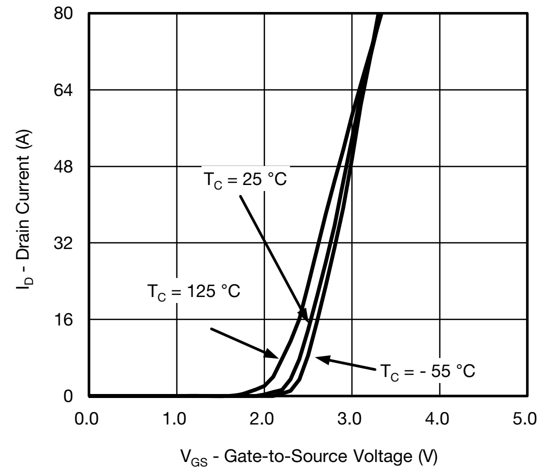
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

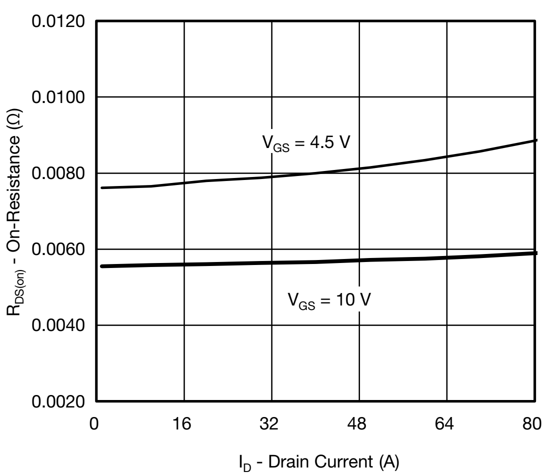
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



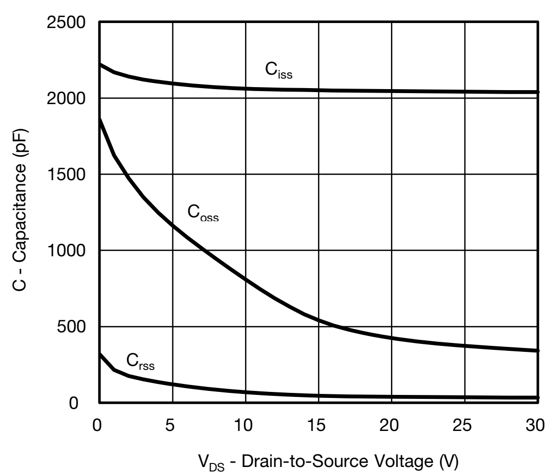
Output Characteristics



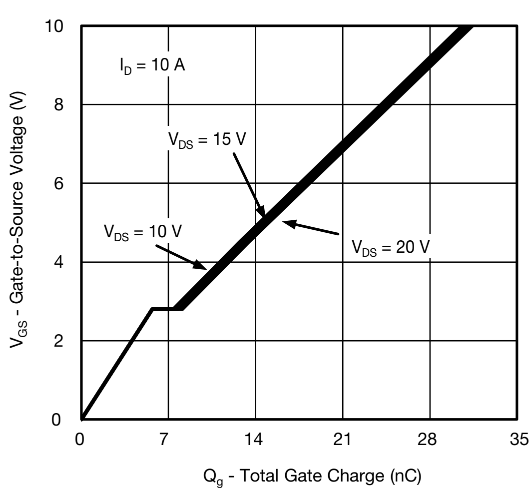
Transfer Characteristics



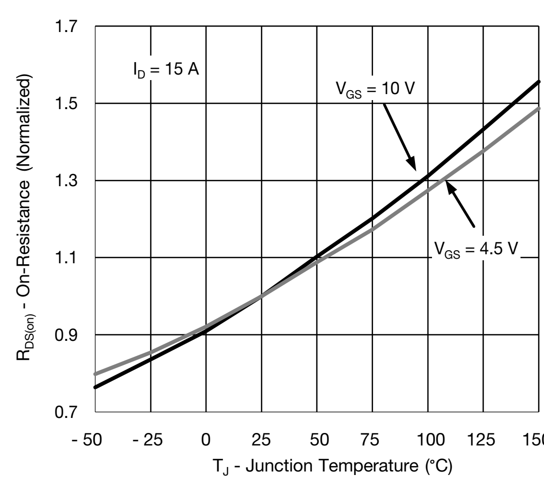
On-Resistance vs. Drain Current



Capacitance

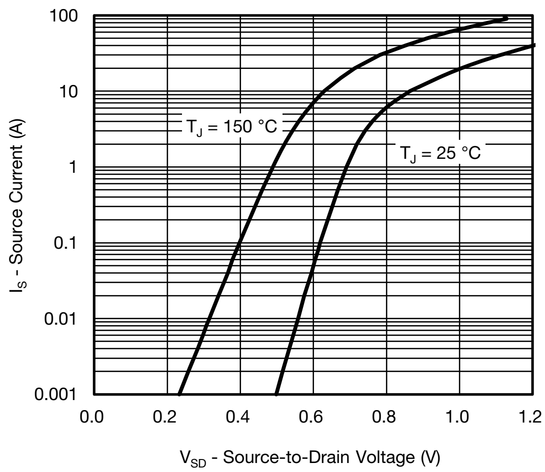


Gate Charge

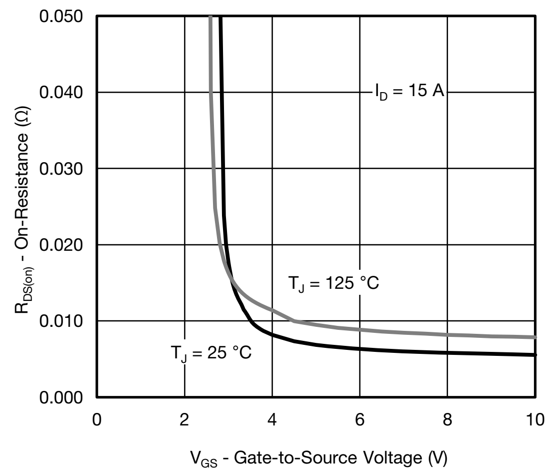


On-Resistance vs. Junction Temperature

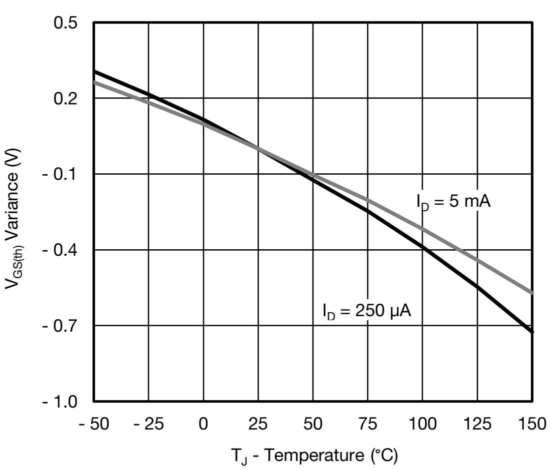
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



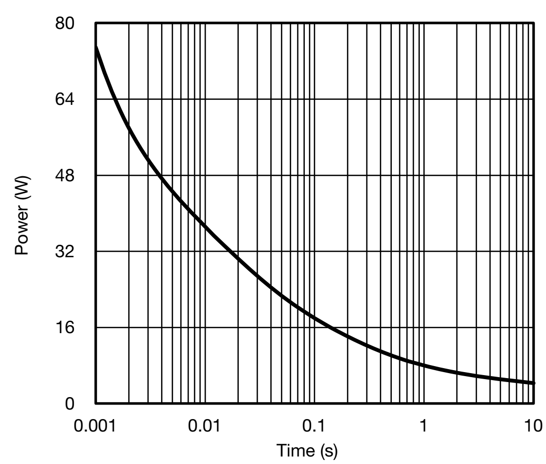
Source-Drain Diode Forward Voltage



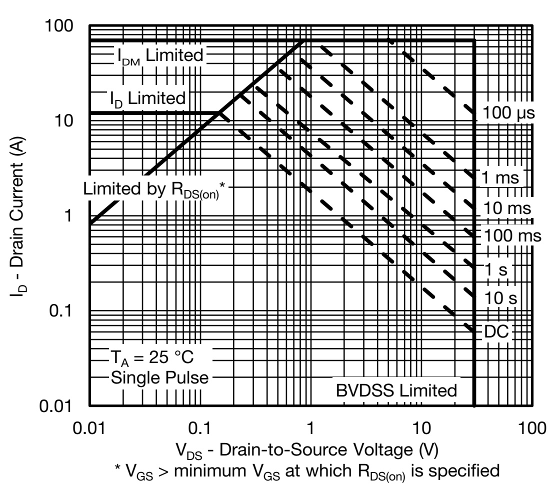
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

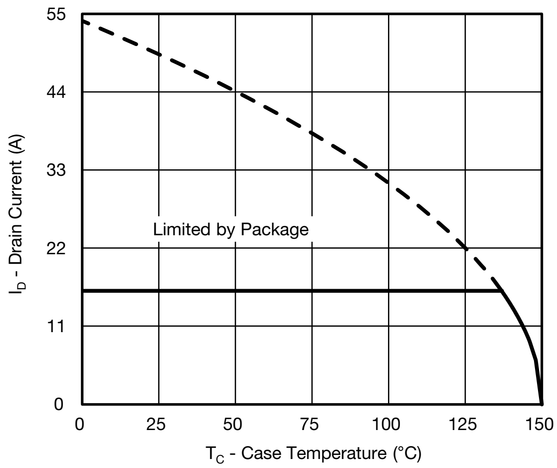


Single Pulse Power, Junction-to-Ambient

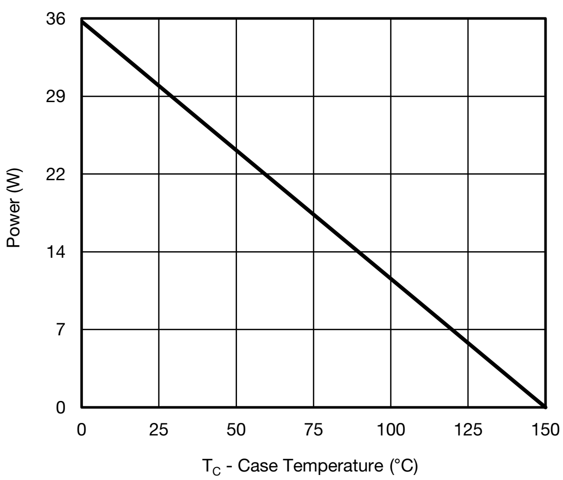


Safe Operating Area

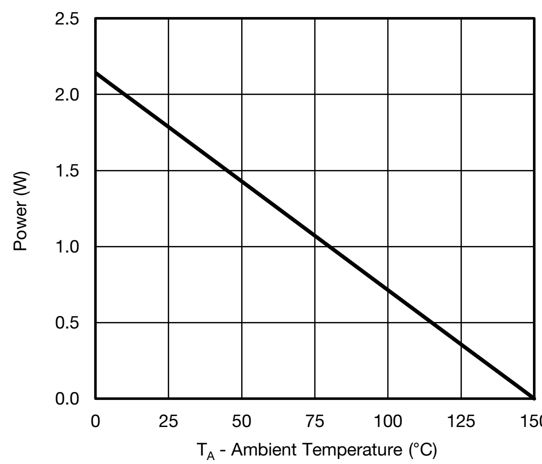
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



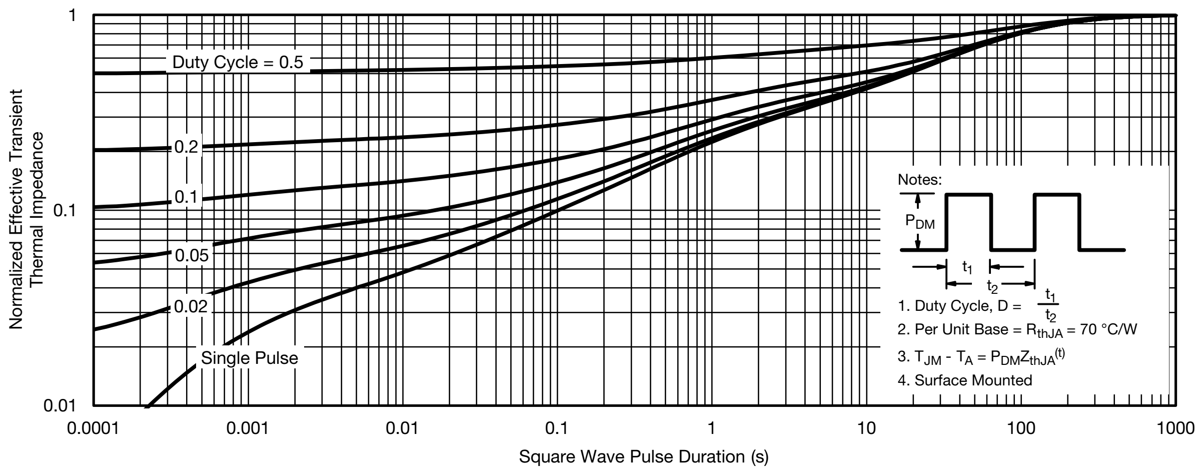
Power, Junction-to-Case



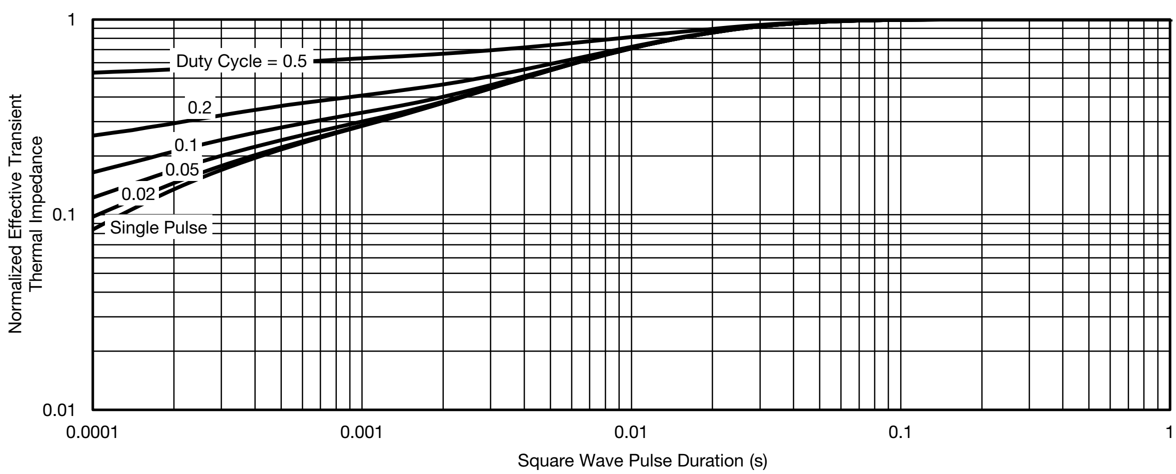
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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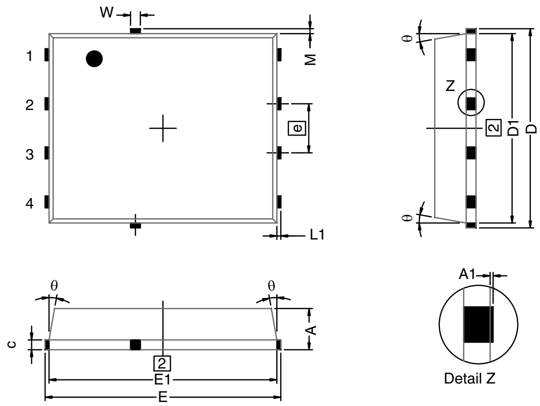
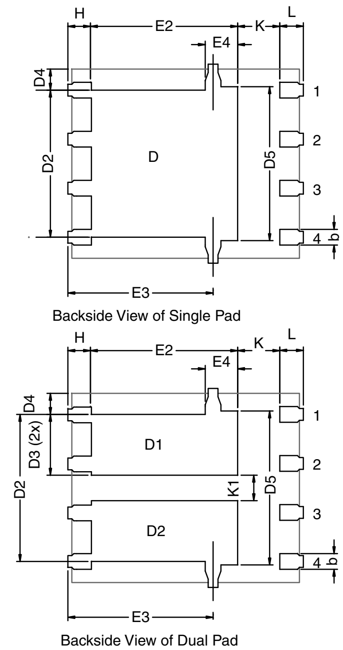
PowerPAK® SO-8, (Single/Dual)



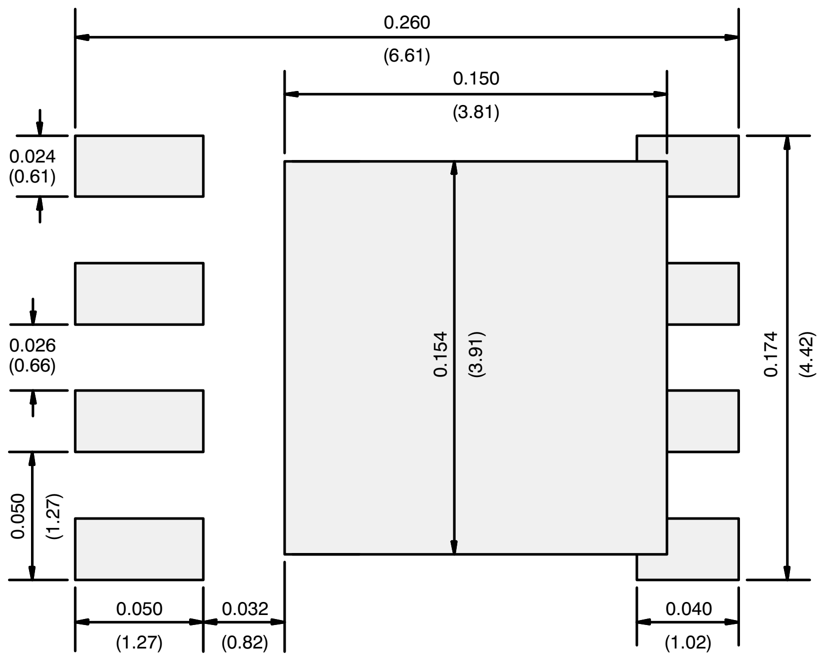


Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S17-0173-Rev. L, 13-Feb-17 DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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